

LMx31x Precision Voltage-to-Frequency Converters

1 Features

- Ensured Linearity 0.01% Maximum
- Improved Performance in Existing Voltage-to-Frequency Conversion Applications
- Split or Single-Supply Operation
- Operates on Single 5-V Supply
- Pulse Output Compatible With All Logic Forms
- Excellent Temperature Stability: ± 50 ppm/ $^{\circ}\text{C}$ Maximum
- Low Power Consumption: 15 mW Typical at 5 V
- Wide Dynamic Range, 100 dB Minimum at 10-kHz Full Scale Frequency
- Wide Range of Full Scale Frequency: 1 Hz to 100 kHz
- Low-Cost

2 Applications

- Voltage to Frequency Conversions
- Frequency to Voltage Conversions
- Remote-Sensor Monitoring
- Tachometers

3 Description

The LMx31 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM231	PDIP (8)	9.81 mm x 6.35 mm
LM331		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic Diagram

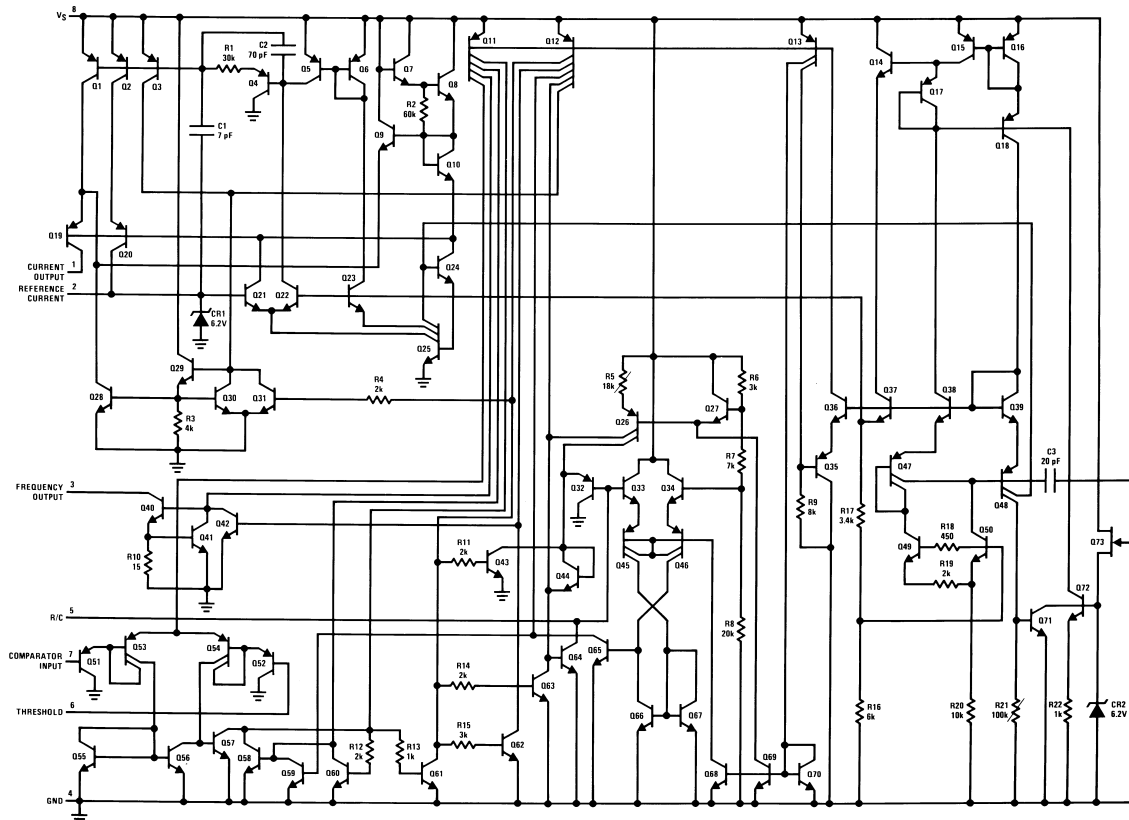


Table of Contents

1 Features	1	8.3 Feature Description.....	10
2 Applications	1	8.4 Device Functional Modes.....	10
3 Description	1	9 Application and Implementation	11
4 Revision History	2	9.1 Application Information.....	11
5 Description continued	3	9.2 Typical Applications	12
6 Pin Configuration and Functions	4	9.3 System Examples	15
7 Specifications	4	10 Power Supply Recommendations	18
7.1 Absolute Maximum Ratings	4	11 Layout	18
7.2 ESD Ratings.....	4	11.1 Layout Guidelines	18
7.3 Recommended Operating Conditions.....	5	11.2 Layout Example	18
7.4 Thermal Information	5	12 Device and Documentation Support	19
7.5 Electrical Characteristics.....	5	12.1 Related Links	19
7.6 Dissipation Ratings	6	12.2 Community Resources.....	19
7.7 Typical Characteristics	7	12.3 Trademarks	19
8 Detailed Description	9	12.4 Electrostatic Discharge Caution.....	19
8.1 Overview	9	12.5 Glossary	19
8.2 Functional Block Diagram	9	13 Mechanical, Packaging, and Orderable Information	19

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C	Page
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

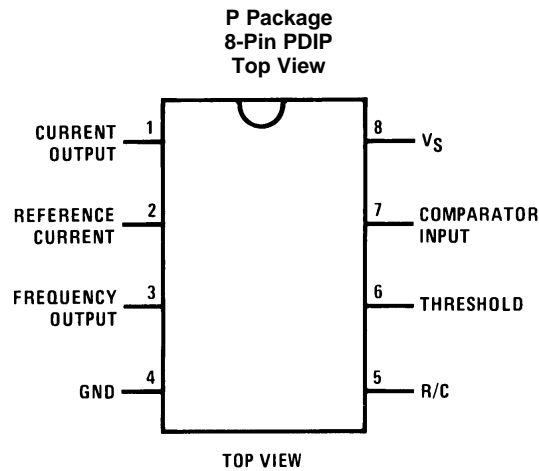
Changes from Revision A (March 2013) to Revision B	Page
<ul style="list-style-type: none"> Changed layout of National Data Sheet to TI format 	1

5 Description continued

Further, the LMx31A attain a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LMx31 are ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery-powered voltage-to-frequency converter can be easily channeled through a simple photo isolator to provide isolation against high common-mode levels.

The LMx31 uses a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4 V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100-kHz voltage-to-frequency conversion. And the output are capable of driving 3 TTL loads, or a high-voltage output up to 40 V, yet is short-circuit-proof against V_{CC} .

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IOUT	1	O	Current Output
IREF	2	I	Reference Current
FOUT	3	O	Frequency Output. This output is an open-collector output and requires a pullup resistor.
GND	4	G	Ground
RC	5	I	R-C filter input
THRESH	6	I	Threshold input
COMPIN	7	I	Comparator Input
VS	8	P	Supply Voltage

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
Supply Voltage, V_S			40	V
Output Short Circuit to Ground		Continuous		
Output Short Circuit to V_{CC}		Continuous		
Input Voltage		-0.2	+ V_S	V
Lead Temperature (Soldering, 10 sec.)	PDIP		260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are measured with respect to GND = 0 V, unless otherwise noted.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾⁽²⁾	±500 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) Human body model, 100 pF discharged through a 1.5-kΩ resistor.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Operating Ambient Temperature	LM231, LM231A	-25	85	°C
	LM331, LM331A	0	70	°C
Supply Voltage, V_S ⁽¹⁾		4	40	V

(1) All voltages are measured with respect to GND = 0 V, unless otherwise noted.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM312, LM331	UNIT
		P (PDIP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

All specifications apply in the circuit of [Figure 16](#), with $4.0\text{ V} \leq V_S \leq 40\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VFC Non-Linearity ⁽¹⁾		$4.5\text{ V} \leq V_S \leq 20\text{ V}$		±0.003	±0.01	% Full-Scale
		$T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$		±0.006	±0.02	% Full-Scale
VFC Non-Linearity in Circuit of Figure 14		$V_S = 15\text{ V}$, $f = 10\text{ Hz to } 11\text{ kHz}$		±0.024	±0.14	% Full-Scale
Conversion Accuracy Scale Factor (Gain)	LM231, LM231A	$V_{\text{IN}} = -10\text{ V}$, $R_S = 14\text{ k}\Omega$	0.95	1	1.05	kHz/V
	LM331, LM331A		0.9	1	1.1	kHz/V
Temperature Stability of Gain	LMx31	$T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$ $4.5\text{ V} \leq V_S \leq 20\text{ V}$		±30	±150	ppm/°C
	LMx31A			±20	±50	ppm/°C
Change of Gain with V_S		$4.5\text{ V} \leq V_S \leq 10\text{ V}$		0.01	0.1	%/V
		$10\text{ V} \leq V_S \leq 40\text{ V}$		0.006	0.06	%/V
Rated Full-Scale Frequency		$V_{\text{IN}} = -10\text{ V}$	10.0			kHz
Gain Stability vs. Time (1000 Hours)		$T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$		±0.02		% Full-Scale
Over Range (Beyond Full-Scale) Frequency		$V_{\text{IN}} = -11\text{ V}$	10%			
INPUT COMPARATOR						
Offset Voltage				±3	±10	mV
	LM231/LM331	$T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$		±4	±14	mV
	LM231A/LM331A	$T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$		±3	±10	mV
Bias Current				-80	-300	nA
Offset Current				±8	±100	nA
Common-Mode Range		$T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$	-0.2		$V_{\text{CC}} - 2$	V
TIMER						
Timer Threshold Voltage, Pin 5			$0.63 \times V_S$	$0.667 \times V_S$	$0.7 \times V_S$	
Input Bias Current, Pin 5		$V_S = 15\text{ V}$				
	All Devices	$0\text{ V} \leq V_{\text{PIN } 5} \leq 9.9\text{ V}$		±10	±100	nA
	LM231/LM331	$V_{\text{PIN } 5} = 10\text{ V}$		200	1000	nA
	LM231A/LM331A	$V_{\text{PIN } 5} = 10\text{ V}$		200	500	nA
$V_{\text{SAT PIN } 5}$ (Reset)		$I = 5\text{ mA}$		0.22	0.5	V

(1) Non-linearity is defined as the deviation of f_{OUT} from $V_{\text{IN}} \times (10\text{ kHz}/-10\text{ V}_{\text{DC}})$ when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T , use NPO ceramic, Teflon®, or polystyrene.

Electrical Characteristics (continued)

All specifications apply in the circuit of [Figure 16](#), with $4.0\text{ V} \leq V_S \leq 40\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SOURCE (PIN 1)						
Output Current	LM231, LM231A	$R_S = 14\text{ k}\Omega$, $V_{\text{PIN } 1} = 0$	126	135	144	μA
	LM331, LM331A		116	136	156	μA
Change with Voltage		$0\text{V} \leq V_{\text{PIN } 1} \leq 10\text{ V}$		0.2	1	μA
Current Source OFF Leakage	LM231, LM231A, LM331, LM331A			0.02	10	nA
	All Devices	$T_A = T_{\text{MAX}}$		2	50	nA
Operating Range of Current (Typical)			(10 to 500)			μA
REFERENCE VOLTAGE (PIN 2)						
LM231, LM231A			1.76	1.89	2.02	V_{DC}
LM331, LM331A			1.7	1.89	2.08	V_{DC}
Stability vs. Temperature				± 60		ppm/ $^\circ\text{C}$
Stability vs. Time, 1000 Hours				$\pm 0.1\%$		
LOGIC OUTPUT (PIN 3)						
V_{SAT}	$I = 5\text{ mA}$			0.15	0.5	V
	$I = 3.2\text{ mA}$ (2 TTL Loads), $T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$			0.1	0.4	V
OFF Leakage				± 0.05	1	μA
SUPPLY CURRENT						
LM231, LM231A	$V_S = 5\text{ V}$		2	3	4	mA
	$V_S = 40\text{ V}$		2.5	4	6	mA
LM331, LM331A	$V_S = 5\text{ V}$		1.5	3	6	mA
	$V_S = 40\text{ V}$		2	4	8	mA

7.6 Dissipation Ratings

	VALUE	UNIT
Package Dissipation at 25°C ⁽¹⁾	1.25	W

- (1) The absolute maximum junction temperature (T_{Jmax}) for this device is 150°C . The maximum allowable power dissipation is dictated by T_{Jmax} , the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature T_A , and can be calculated using the formula $P_{\text{Dmax}} = (T_{\text{Jmax}} - T_A) / \theta_{\text{JA}}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

7.7 Typical Characteristics

(All electrical characteristics apply for the circuit of Figure 16, unless otherwise noted.)

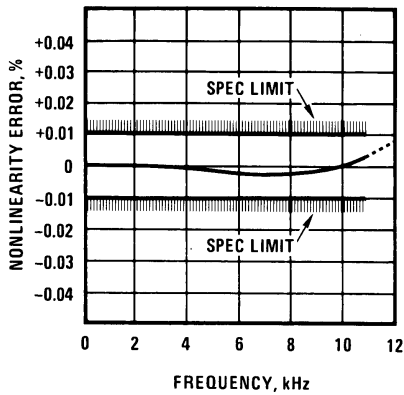


Figure 1. Non-Linearity Error as Precision V-to-F Converter (Figure 16)

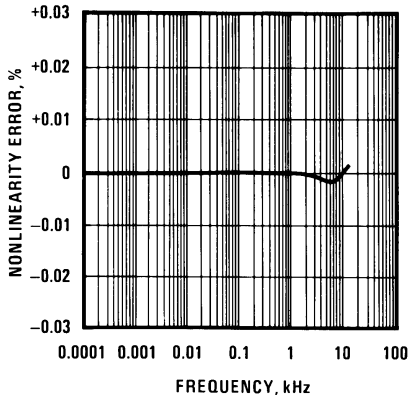


Figure 2. Non-Linearity Error

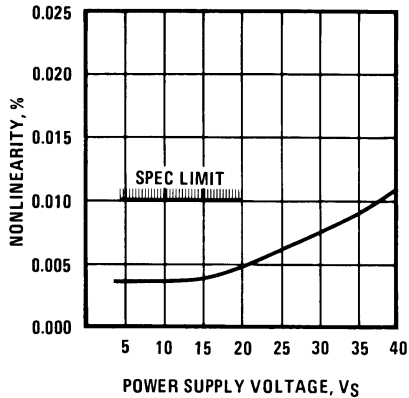


Figure 3. Non-Linearity Error vs. Power Supply Voltage

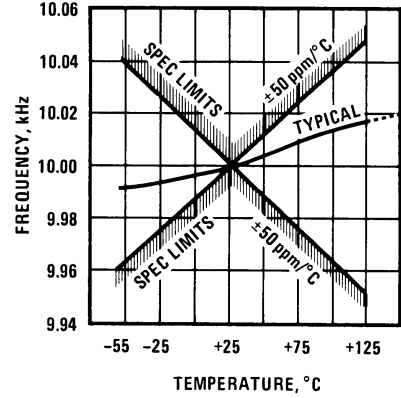


Figure 4. Frequency vs. Temperature

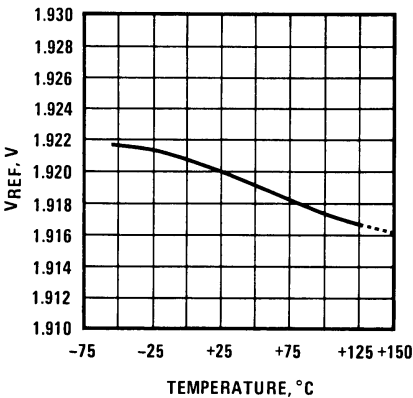


Figure 5. VREF vs. Temperature

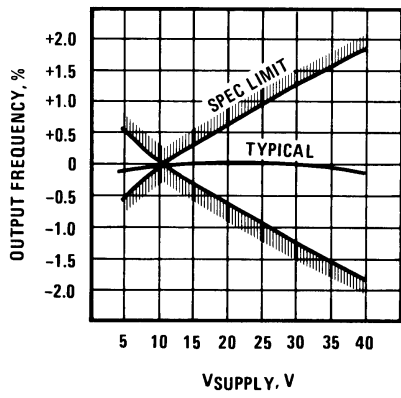


Figure 6. Output Frequency vs. V_SUPPLY

Typical Characteristics (continued)

(All electrical characteristics apply for the circuit of [Figure 16](#), unless otherwise noted.)

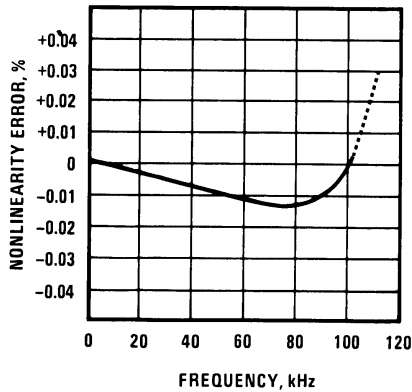


Figure 7. 100 kHz Non-Linearity Error ([Figure 17](#))

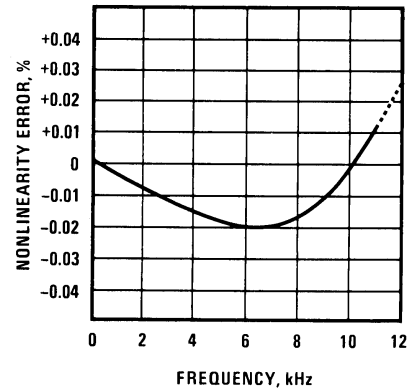


Figure 8. Non-Linearity Error ([Figure 14](#))

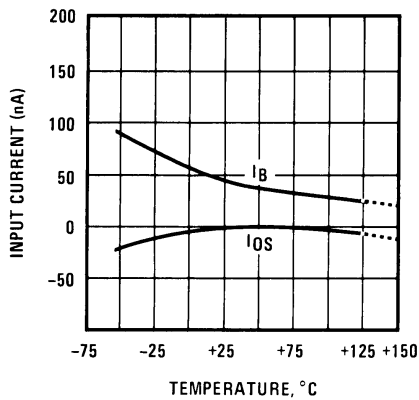


Figure 9. Input Current (Pins 6,7) vs. Temperature

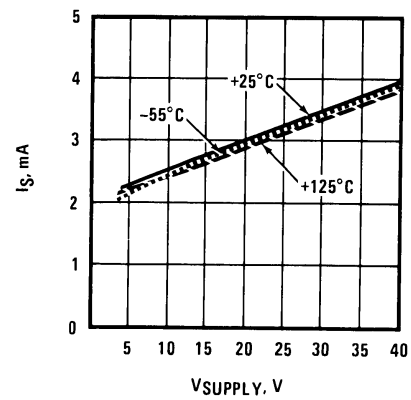


Figure 10. Power Drain vs. V_{SUPPLY}

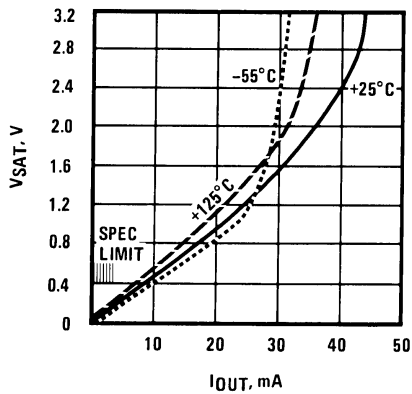


Figure 11. Output Saturation Voltage vs. I_{OUT} (Pin 3)

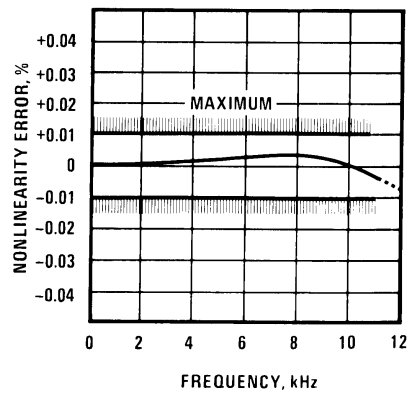


Figure 12. Non-Linearity Error, Precision F-to-V Converter ([Figure 19](#))

8 Detailed Description

8.1 Overview

8.1.1 Detail of Operation, Functional Block Diagram

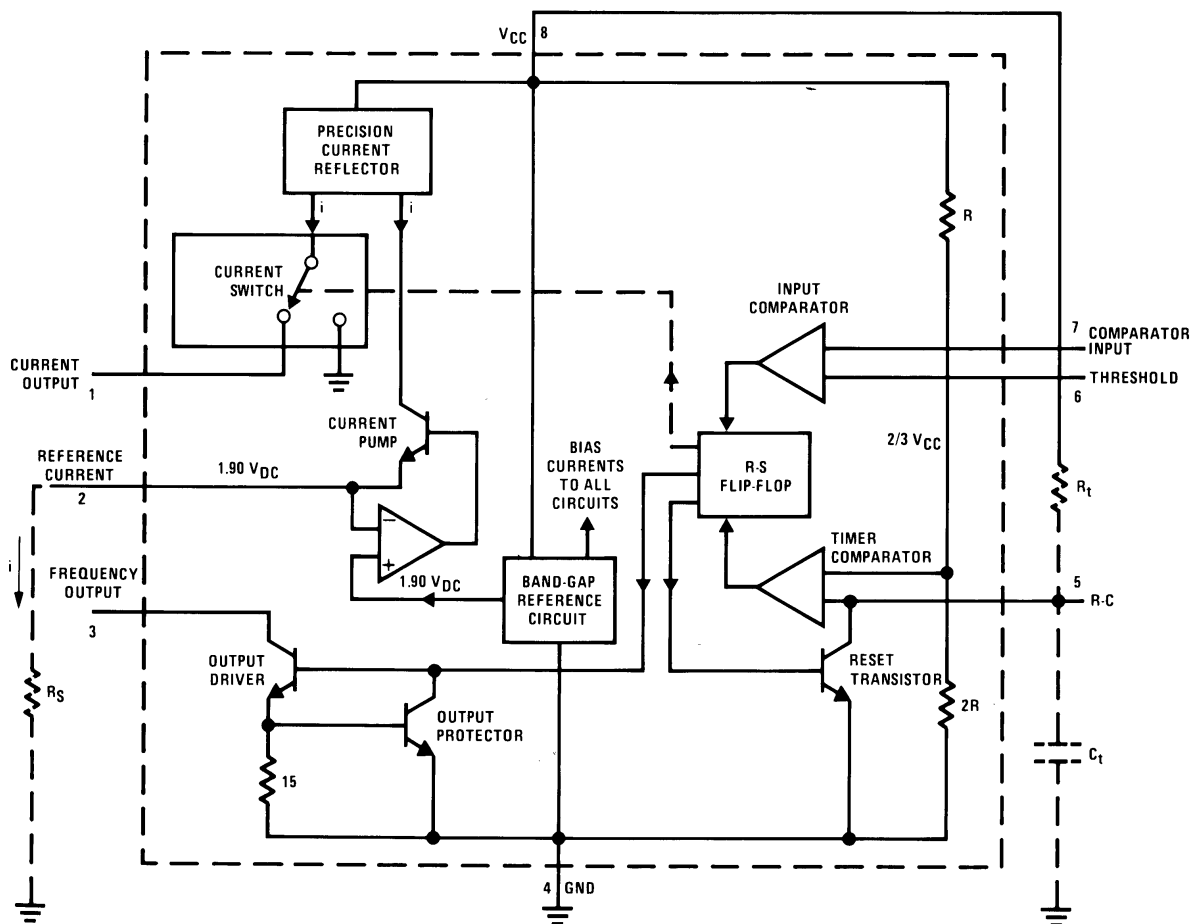
The *Functional Block Diagram* shows a band gap reference which provides a stable 1.9-V_{DC} output. This 1.9 V_{DC} is well regulated over a V_S range of 3.9 V to 40 V. It also has a flat, low temperature coefficient, and typically changes less than ½% over a 100°C temperature change.

The current pump circuit forces the voltage at pin 2 to be at 1.9 V, and causes a current $i = 1.90 \text{ V}/R_S$ to flow. For $R_S=14 \text{ k}$, $i=135 \mu\text{A}$. The precision current reflector provides a current equal to i to the current switch. The current switch switches the current to pin 1 or to ground, depending upon the state of the R-S flip-flop.

The timing function consists of an R-S flip-flop and a timer comparator connected to the external R_tC_t network. When the input comparator detects a voltage at pin 7 higher than pin 6, it sets the R-S flip-flop which turns ON the current switch and the output driver transistor. When the voltage at pin 5 rises to ⅔ V_{CC}, the timer comparator causes the R-S flip-flop to reset. The reset transistor is then turned ON and the current switch is turned OFF.

However, if the input comparator still detects the voltage on pin 7 as higher than pin 6 when pin 5 crosses ⅔ V_{CC}, the flip-flop will not be reset, and the current at pin 1 will continue to flow, trying to make the voltage at pin 6 higher than pin 7. This condition will usually apply under start-up conditions or in the case of an overload voltage at signal input. During this sort of overload the output frequency will be 0. As soon as the signal is restored to the working range, the output frequency will be resumed.

8.2 Functional Block Diagram



8.3 Feature Description

The LMx31 operate over a wide voltage range of 4 V to 40 V.

The voltage at pin 2 is regulated at $1.90 V_{DC}$ for all values of i between $10 \mu A$ to $500 \mu A$. It can be used as a voltage reference for other components, but take care to ensure that current is not taken from it which could reduce the accuracy of the converter.

8.4 Device Functional Modes

The output driver transistor acts to saturate pin 3 with an ON resistance of about 50Ω . In case of overvoltage, the output current is actively limited to less than 50 mA.

If the voltage on pin 7 is higher than pin 6 when pin 5 crosses $\frac{2}{3} V_{CC}$, the LMx31 internal flip-flop will not be reset, and the current at pin 1 will continue to flow, trying to make the voltage at pin 6 higher than pin 7. This condition will usually apply under start-up conditions or in the case of an overload voltage at signal input. During this sort of overload the output frequency will be 0. As soon as the signal is restored to the working range, the output frequency will be resumed.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Simplified Voltage-to-Frequency Converter

The operation of these blocks is best understood by going through the operating cycle of the basic V-to-F converter, [Figure 13](#), which consists of the simplified block diagram of the LMx31 and the various resistors and capacitors connected to it.

The voltage comparator compares a positive input voltage, V_1 , at pin 7 to the voltage, V_x , at pin 6. If V_1 is greater, the comparator will trigger the 1-shot timer. The output of the timer will turn ON both the frequency output transistor and the switched current source for a period $t = 1.1 R_t C_t$. During this period, the current i will flow out of the switched current source and provide a fixed amount of charge, $Q = i \times t$, into the capacitor, C_L . This will normally charge V_x up to a higher level than V_1 . At the end of the timing period, the current i will turn OFF, and the timer will reset itself.

Now there is no current flowing from pin 1, and the capacitor C_L will be gradually discharged by R_L until V_x falls to the level of V_1 . Then the comparator will trigger the timer and start another cycle.

The current flowing into C_L is exactly $I_{AVE} = i \times (1.1 \times R_t C_t) \times f$, and the current flowing out of C_L is exactly $V_x / R_L \approx V_{IN} / R_L$. If V_{IN} is doubled, the frequency will double to maintain this balance. Even a simple V-to-F converter can provide a frequency precisely proportional to its input voltage over a wide range of frequencies.

9.1.2 Principles of Operation

The LMx31 are monolithic circuits designed for accuracy and versatile operation when applied as voltage-to-frequency (V-to-F) converters or as frequency-to-voltage (F-to-V) converters. A simplified block diagram of the LMx31 is shown in [Figure 13](#) and consists of a switched current source, input comparator, and 1-shot timer.

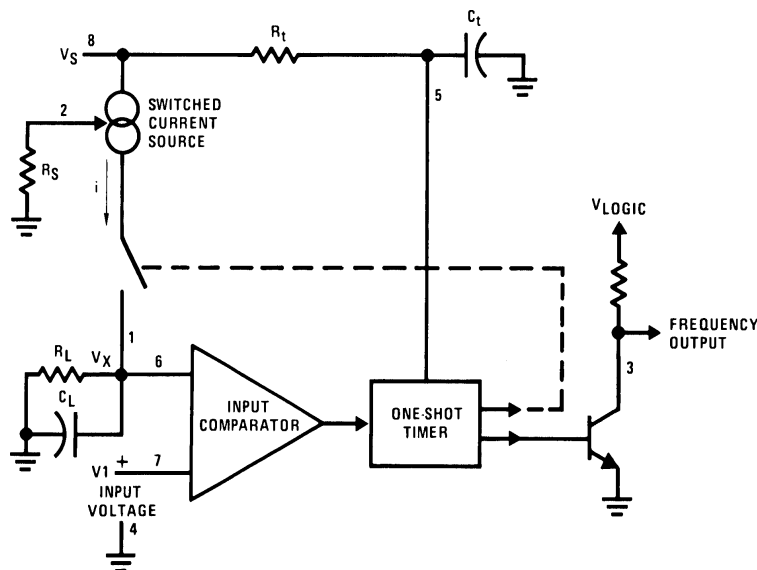
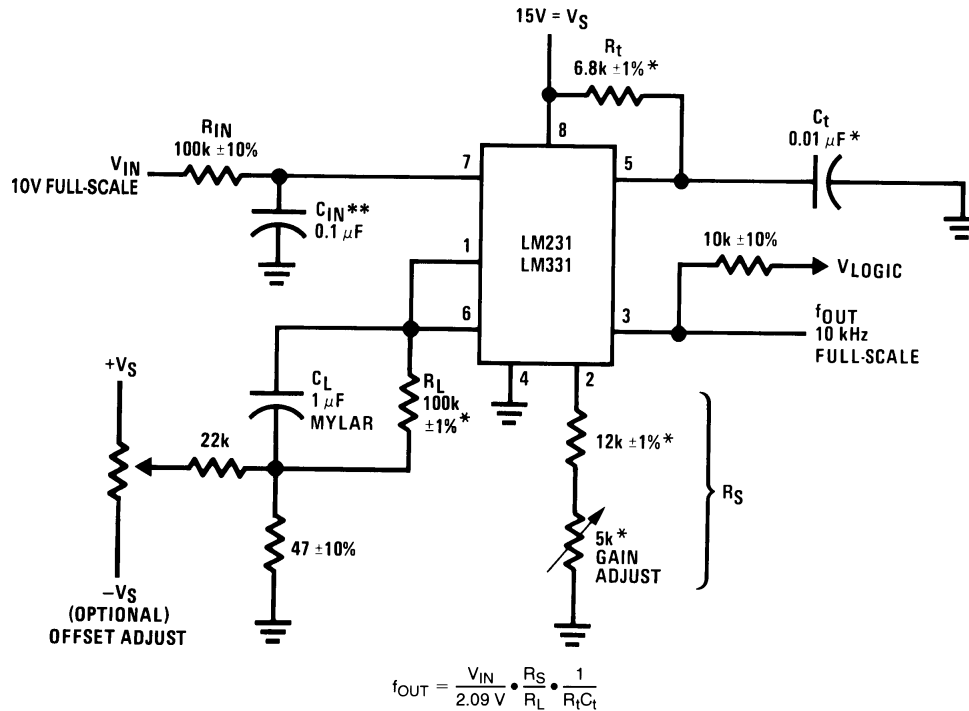


Figure 13. Simplified Block Diagram of Stand-Alone Voltage-to-Frequency Converter and External Components

9.2 Typical Applications

9.2.1 Basic Voltage-to-Frequency Converter

The simple stand-alone V-to-F converter shown in Figure 14 includes all the basic circuitry of Figure 13 plus a few components for improved performance.



*Use stable components with low temperature coefficients. See [Application Information](#).

**0.1 μF or 1 μF, See [Typical Applications](#).

Figure 14. Simple Stand-Alone V-to-F Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

9.2.1.1 Design Requirements

For this example, the system requirements are 0.05% linearity over an output frequency range of 10 Hz to 4 kHz with an input voltage range of 25 mV to 12.5 V. The available supply voltage is 15.0 V.

9.2.1.2 Detailed Design Procedure

A capacitor C_{IN} is added from pin 7 to ground to act as a filter for V_{IN} , use of a 0.1 μF is appropriate for this application. A value of 0.01 μF to 0.1 μF will be adequate in most cases; however, in cases where better filtering is required, a 1-μF capacitor can be used. When the RC time constants are matched at pin 6 and pin 7, a voltage step at V_{IN} will cause a step change in f_{OUT} . If C_{IN} is much less than C_L , a step at V_{IN} may cause f_{OUT} to stop momentarily.

Next, we cancel the comparator bias current by setting R_{IN} to 100 kΩ to match R_L . This will help to minimize any frequency offset.

For best results, all the components should be stable low-temperature-coefficient components, such as metal-film resistors. The capacitor should have low dielectric absorption; depending on the temperature characteristics desired, NPO ceramic, polystyrene, Teflon or polypropylene are best suited.

The resistance R_S at pin 2 is made up of a 12-kΩ fixed resistor plus a 5-kΩ (cermet, preferably) gain adjust rheostat. The function of this adjustment is to trim out the gain tolerance of the LMx31, and the tolerance of R_t , R_L and C_t .

Typical Applications (continued)

A 47-Ω resistor in series with the 1-μF capacitor (CL) provides hysteresis, which helps the input comparator provide the excellent linearity.

This results in the transfer function of $f_{OUT} = (V_{IN} / 2.09 V) \times (R_S / R_L) \times (1 / R_t C_t)$.

9.2.1.3 Application Curve

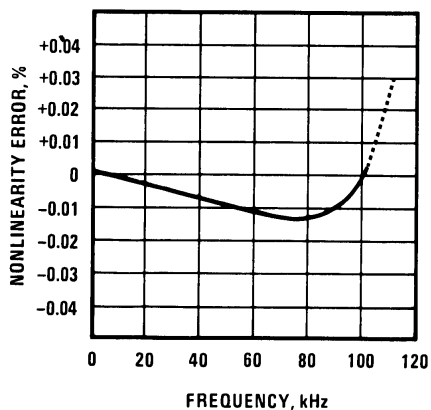


Figure 15. Output Non-Linearity Error vs. Frequency

Typical Applications (continued)

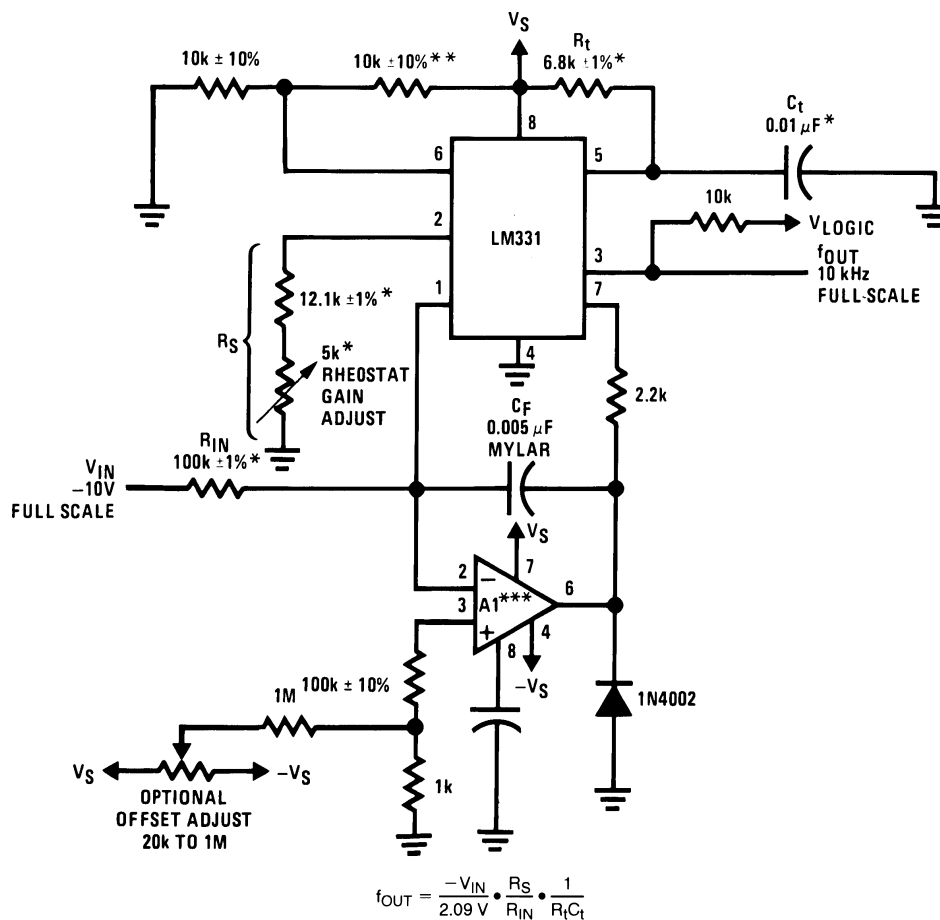
9.2.2 Precision V-To-F Converter

In this circuit, integration is performed by using a conventional operational amplifier and feedback capacitor, C_F . When the integrator's output crosses the nominal threshold level at pin 6 of the LMx31, the timing cycle is initiated.

The average current fed into the summing point of the op-amp (pin 2) is $i \times (1.1 R_t C_t) \times f$ which is perfectly balanced with $-V_{IN}/R_{IN}$. In this circuit, the voltage offset of the LMx31 input comparator does not affect the offset or accuracy of the V-to-F converter as it does in the stand-alone V-to-F converter; nor does the LM231/331 bias current or offset current. Instead, the offset voltage and offset current of the operational amplifier are the only limits on how small the signal can be accurately converted. Since op-amps with voltage offset well below 1 mV and offset currents well below 2 nA are available at low cost, this circuit is recommended for best accuracy for small signals. This circuit also responds immediately to any change of input signal (which a stand-alone circuit does not) so that the output frequency will be an accurate representation of V_{IN} , as quickly as the spacing of the 2 output pulses can be measured.

In the precision mode, excellent linearity is obtained because the current source (pin 1) is always at ground potential and that voltage does not vary with V_{IN} or f_{OUT} . (In the stand-alone V-to-F converter, a major cause of non-linearity is the output impedance at pin 1 which causes i to change as a function of V_{IN}).

The circuit of [Figure 17](#) operates in the same way as [Figure 16](#), but with the necessary changes for high-speed operation.



*Use stable components with low temperature coefficients.

**This resistor can be 5 kΩ or 10 kΩ for $V_S = 8 V$ to 22 V, but must be 10 kΩ for $V_S = 4.5 V$ to 8 V.

***Use low offset voltage and low offset current op-amps for A1: recommended type LF411A

Figure 16. Standard Test Circuit and Applications Circuit, Precision Voltage-to-Frequency Converter

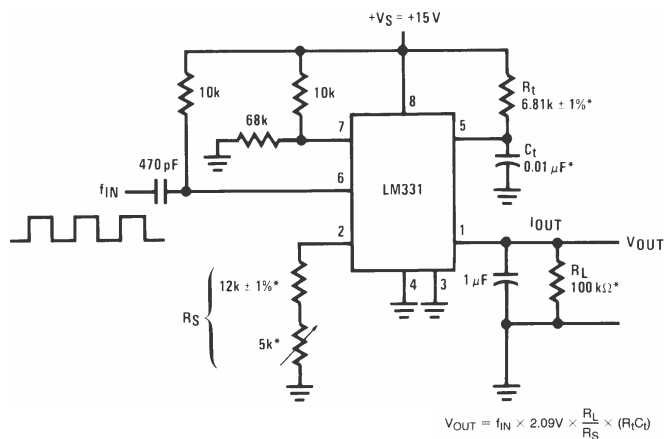
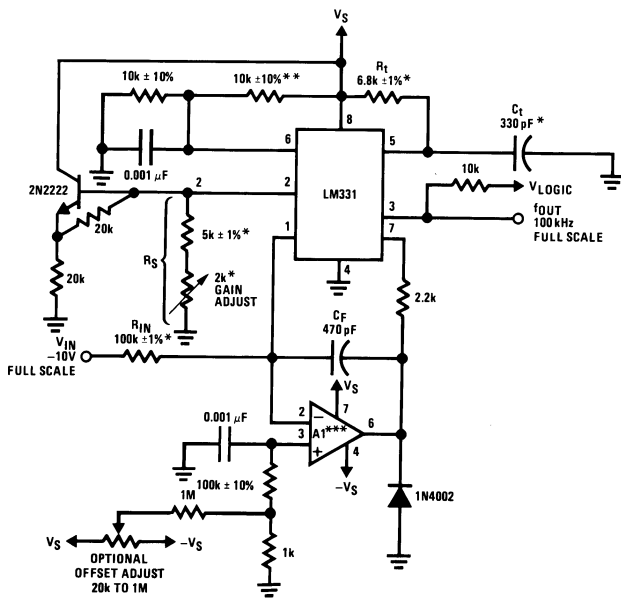
9.3 System Examples

9.3.1 F-to-V Converters

In these applications, a pulse input at f_{IN} is differentiated by a C-R network and the negative-going edge at pin 6 causes the input comparator to trigger the timer circuit. Just as with a V-to-F converter, the average current flowing out of pin 1 is $I_{AVERAGE} = i \times (1.1 R_t C_t) \times f$.

In the simple circuit of Figure 18, this current is filtered in the network $R_L = 100\text{ k}\Omega$ and $1\text{ }\mu\text{F}$. The ripple will be less than 10-mV peak, but the response will be slow, with a 0.1 second time constant, and settling of 0.7 second to 0.1% accuracy.

In the precision circuit, an operational amplifier provides a buffered output and also acts as a 2-pole filter. The ripple will be less than 5-mV peak for all frequencies above 1 kHz, and the response time will be much quicker than in Figure 18. However, for input frequencies below 200 Hz, this circuit will have worse ripple than Figure 18. The engineering of the filter time-constants to get adequate response and small enough ripple simply requires a study of the compromises to be made. Inherently, V-to-F converter response can be fast, but F-to-V response can not.



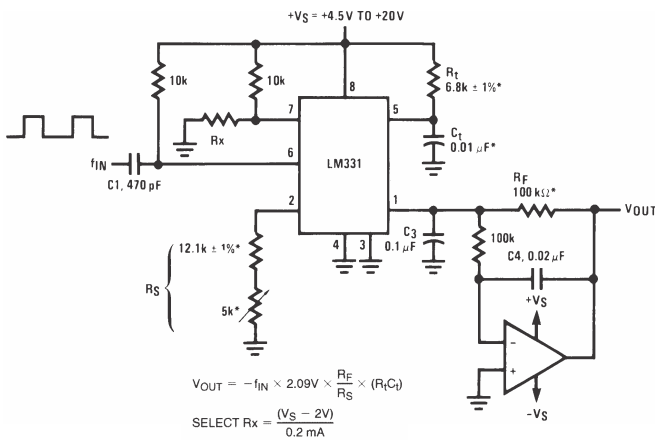
10 kHz Full-Scale, ±0.06% Non-Linearity
*Use stable components with low temperature coefficients.

100 kHz Full-Scale, ±0.03% Non-Linearity
*Use stable components with low temperature coefficients.
**This resistor can be 5 kΩ or 10 kΩ for $V_S=8\text{V}$ to 22V , but must be 10 kΩ for $V_S=4.5\text{V}$ to 8V .
***Use low offset voltage and low offset current op-amps for A1: recommended types LF411A or LF356.

Figure 17. Precision Voltage-to-Frequency Converter

Figure 18. Simple Frequency-to-Voltage Converter

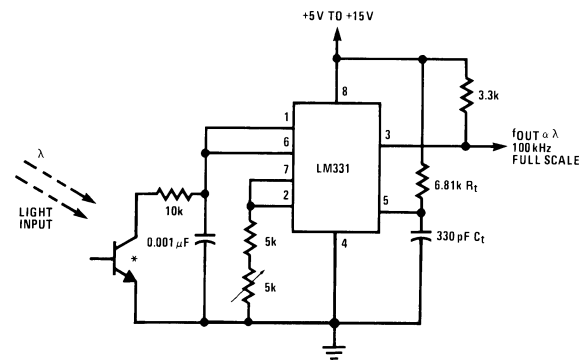
System Examples (continued)



10 kHz Full-Scale With 2-Pole Filter, $\pm 0.01\%$ Non-Linearity Maximum

*Use stable components with low temperature coefficients.

Figure 19. Precision Frequency-to-Voltage Converter,



*L14F-1, L14G-1 or L14H-1, photo transistor (General Electric Co.) or similar

Figure 20. Light Intensity to Frequency Converter

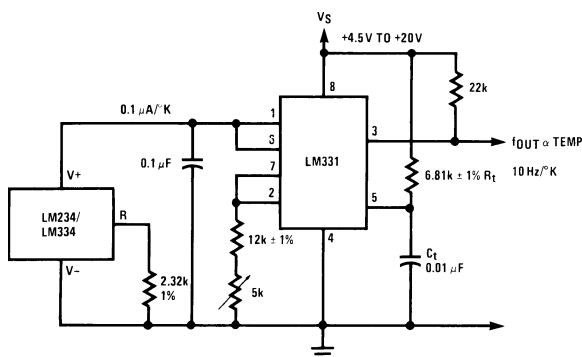


Figure 21. Temperature to Frequency Converter

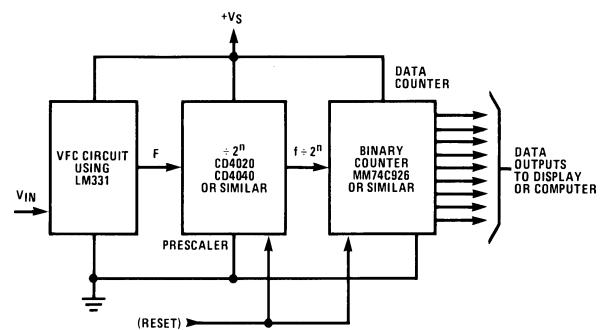


Figure 22. Long-Term Digital Integrator Using VFC

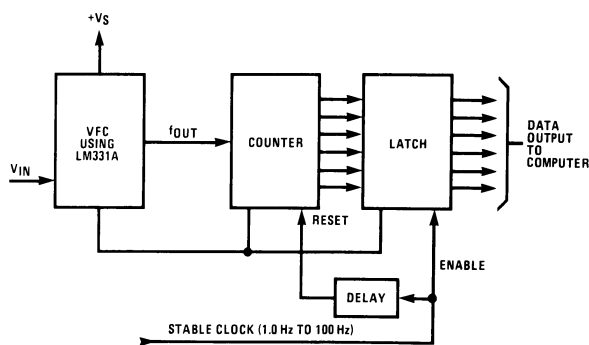


Figure 23. Basic Analog-to-Digital Converter Using Voltage-to-Frequency Converter

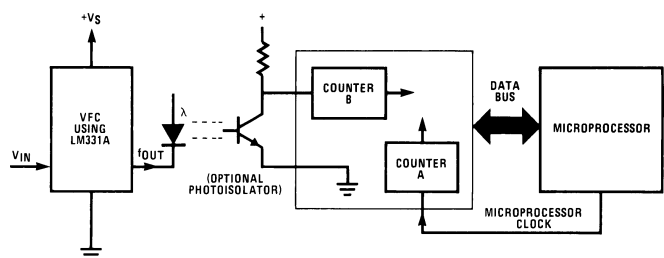


Figure 24. Analog-to-Digital Converter With Microprocessor

System Examples (continued)

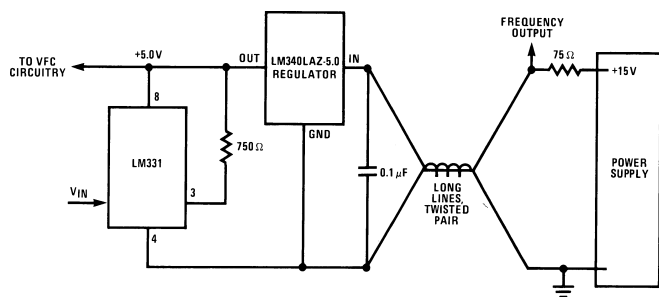


Figure 25. Remote Voltage-to-Frequency Converter With 2-Wire Transmitter and Receiver

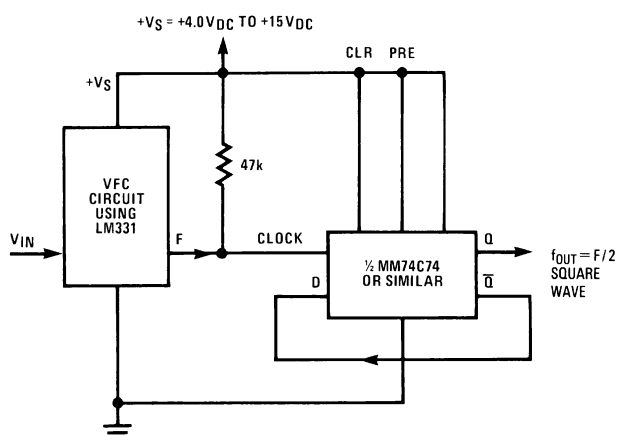


Figure 26. Voltage-to-Frequency Converter With Square-Wave Output Using ÷ 2 Flip-Flop

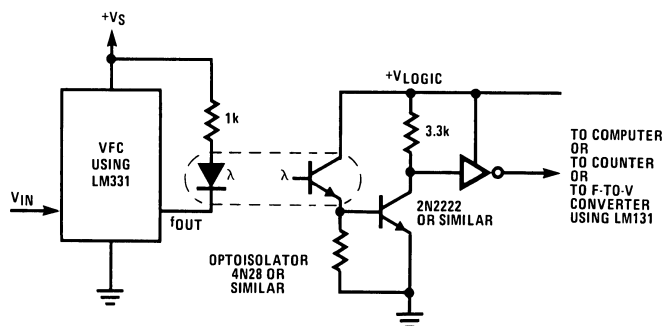


Figure 27. Voltage-to-Frequency Converter With Isolators

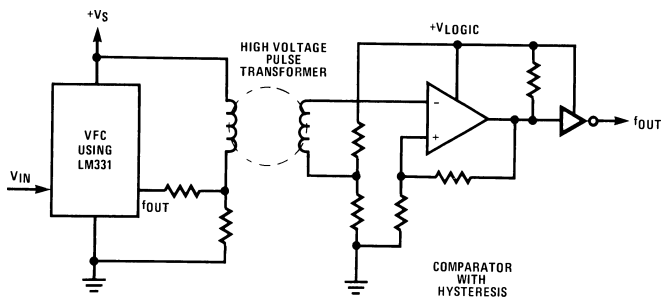


Figure 28. Voltage-to-Frequency Converter With Isolators

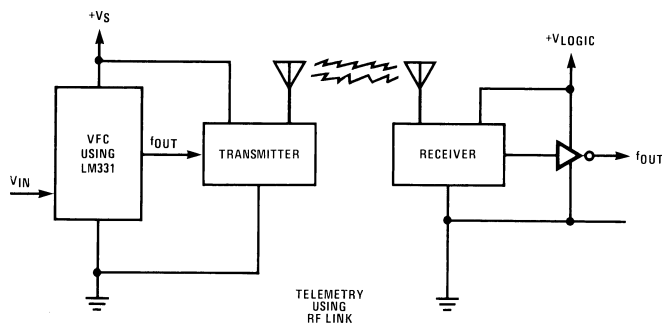


Figure 29. Voltage-to-Frequency Converter With Isolators

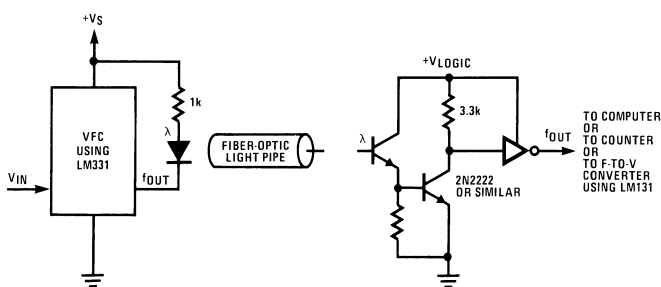


Figure 30. Voltage-to-Frequency Converter With Isolators

10 Power Supply Recommendations

The LMx31 can operate over a wide supply voltage range of 4 V to 40 V. For proper operation, the supply pin should be bypassing to ground with a low-ESR, 1- μ F capacitor. It is acceptable to use X7R capacitors for this. For systems using higher supply voltages, ensure that the voltage rating for the bypass caps is sufficient.

11 Layout

11.1 Layout Guidelines

Bypass capacitors must be placed as close as possible to the supply pin. As the LM331 is a through-hole device, it is acceptable to place the bypass capacitor on the bottom layer.

If an input capacitor to ground is used to clean the input signal, the capacitor should be placed close to the supply pin.

Use of a ground plane is recommended to provide a low-impedance ground across the circuit.

11.2 Layout Example

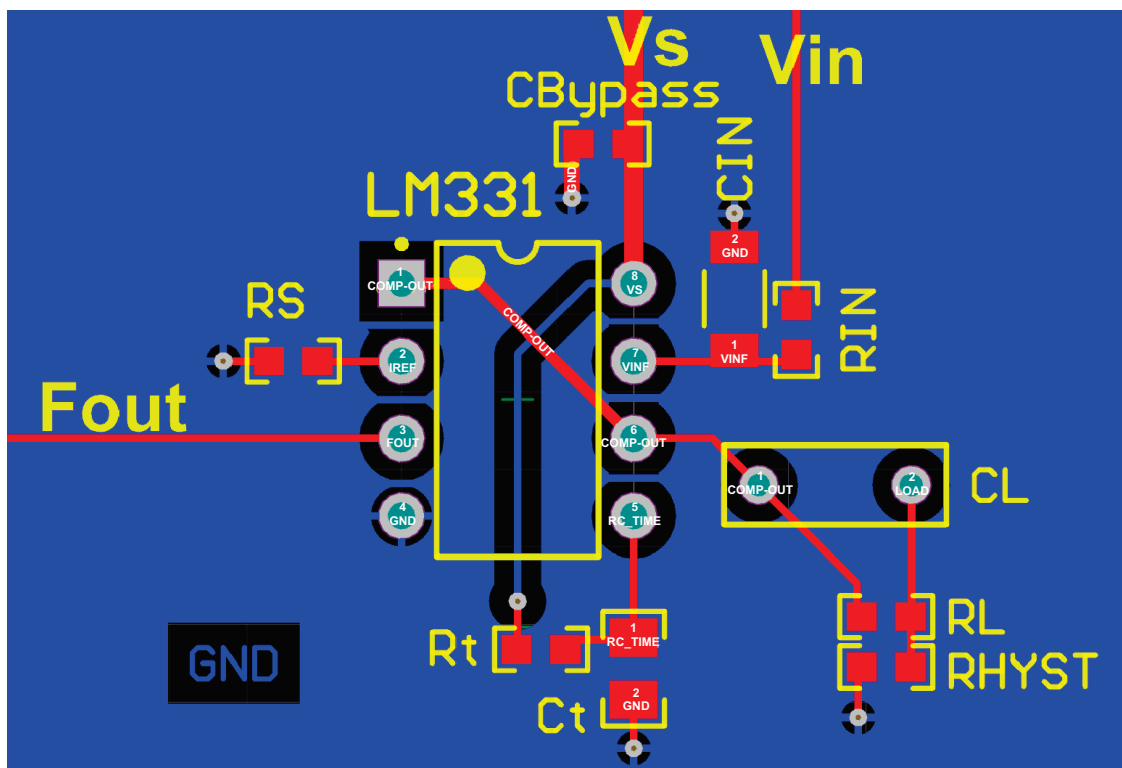


Figure 31. Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM231	Click here	Click here	Click here	Click here	Click here
LM331	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

Teflon is a registered trademark of E.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM231AN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-25 to 85	LM 231AN	Samples
LM231N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-25 to 85	LM 231N	Samples
LM331AN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM 331AN	Samples
LM331N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM 331N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.