裕太微电子
MotorComm

Motorcomm YT8614Q

Datasheet

QSGMII TO QUAD 1000BASE-X/100BASE-FX TRANSCEIVER

VERSION V1.0
DATE 2021-07-26

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Revision History

Revision	Release Date	Summary
1.0	2021/07/26	Release version

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1. Overview

The YT8614Q is used for converting QSGMII interface to four 1000BASE-X/100BASE-FX ports. It's managemet interface comply with IEEE 802.3,Cluase 22, thus the switch controller can access the related register to get the status and set configuration.

1.1. Features

- 5Gbps QSGMII to x4 100BASE-FX/1000Base-X port conversion and each port can also be separately set to SGMII_MAC
- 5Gbps QSGMII to x4 SGMII_PHY port conversion
- 5Gbps QSGMII to x4 SGMII_MAC port conversion
- Supports unidirection in 1000BASE-X/100Base-FX
- SerDes Test pattern
  - PRBS-7/10/31
  - IDLE /K28.5 /D5.6
  - Customized define by user
  - SerDes BIST
- Packet Generator and Checker
- Low power consumption
- Easy layout, good EMI/EMS, and good thermal performance
- Supports 25MHz or 50MHz reference clock input
- 3.3V and 1.2V power supply
- Sync-E clock output
- QFN-88 E-PAD package

1.2. Target Applications

- High Port Density Switch
- QSGMII TO 4*1000BASE-X/100BASE-FX Bridge
- QSGMII TO 4*SGMAC Bridge
- QSGMII TO 4*SGPHY Bridge

1.3. System Application

- 5Gbps QSGMII to four 1000BASE-X/100BASE-FX conversion

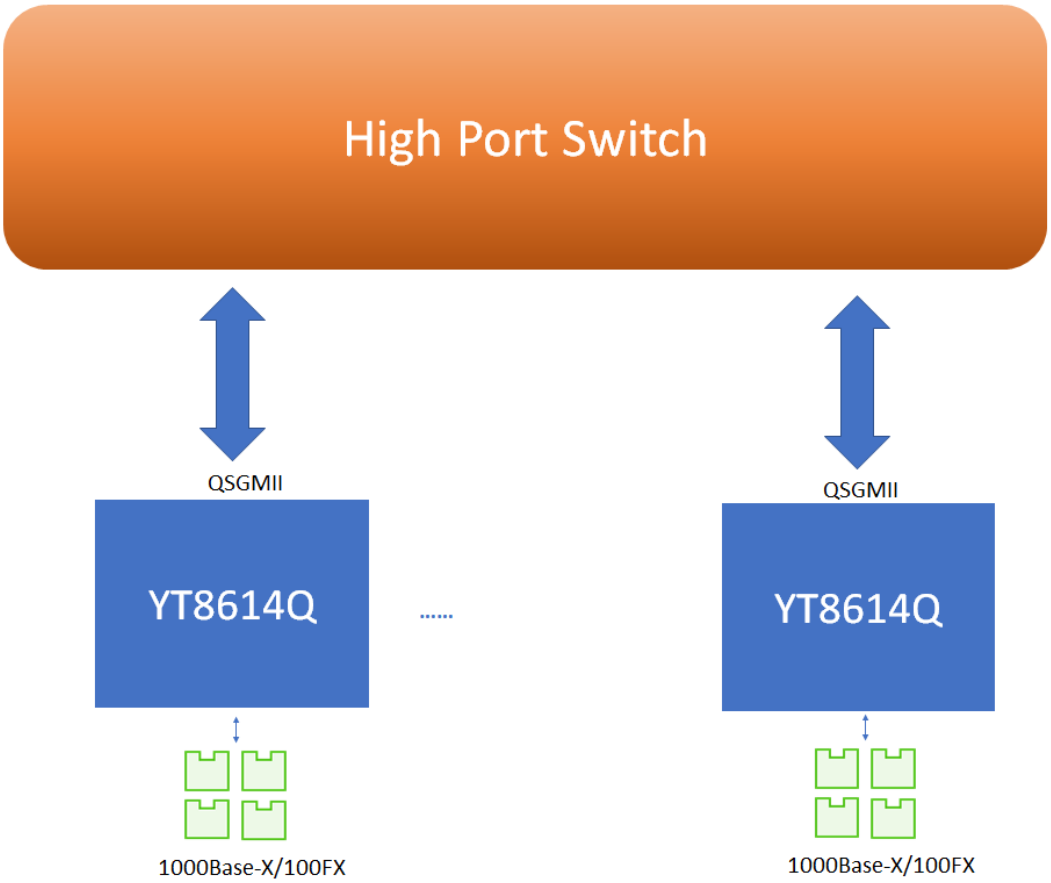


Figure 1. System Application

2. Pin Assignment

2.1. YT8614Q QFN88

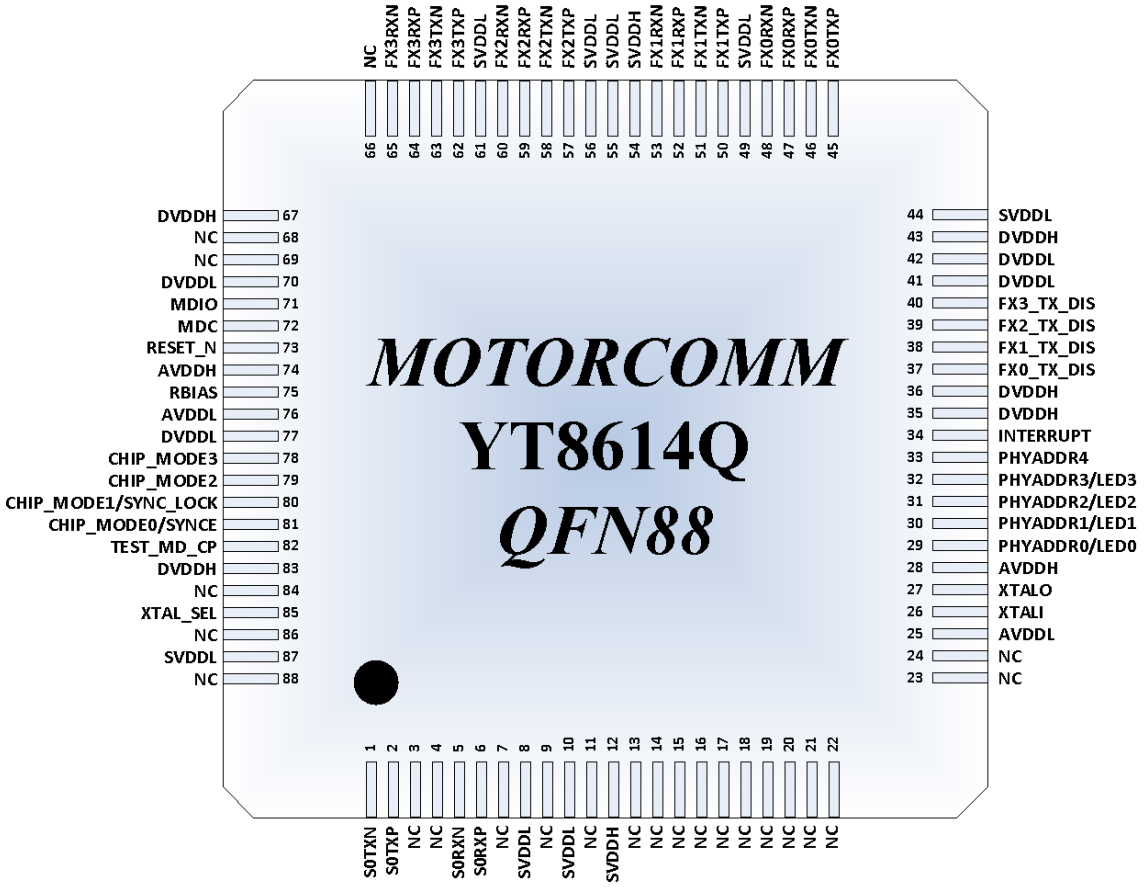


Figure 2. Pin Map

2.2. Pin Descriptions

- I: Input Pin
- AI: Analog Input Pin
- O: Output Pin
- AO: Analog Output Pin
- IO: Bidirectional Input/Output Pin
- AIO: Analog Bidirectional Input/Output Pin
- LI: Latched Input During Power UP or Hardware Reset
- P: Digital Power Pin
- AP: Analog Power Pin
- G: Digital Ground Pin

- AG: Analog Ground Pin
- PD: Internal Pull-Down
- PU: Internal Pull-UP
- SP: SerDes Power Pin
- SG: SerDes Ground Pin
- OD: Open Drain
- XT: Crystal Related

2.2.1. ALL pins

Table 1. All Pins Assignment

NO.	Name	TYPE
1	S0TXN	AO
2	S0TXP	AO
3	NC	-
4	NC	-
5	S0RXN	AI
6	S0RXP	AI
7	NC	-
8	SVDDL	SP
9	NC	-
10	SVDDL	SP
11	NC	-
12	SVDDH	SP
13	NC	-
14	NC	-
15	NC	-
16	NC	-
17	NC	-
18	NC	-
19	NC	-
20	NC	-
21	NC	-
22	NC	-
23	NC	-
24	NC	-
25	AVDDL	AP
26	XTALI	XT
27	XTALO	XT
28	AVDDH	AP
29	PHYADDR0/LED0	LI/O/PD
30	PHYADDR1/LED1	LI/O/PD
31	PHYADDR2/LED2	LI/O/PD
32	PHYADDR3/LED3	LI/O/PD
33	PHYADDR4	LI/PD
34	INTERRUPT	OD/PU
35	DVDDH	P
36	DVDDH	P

NO.	Name	TYPE
37	FX0_TX_DIS	O/PU
38	FX1_TX_DIS	O/PU
39	FX2_TX_DIS	O/PU
40	FX3_TX_DIS	O/PU
41	DVDDL	P
42	DVDDL	P
43	DVDDH	P
44	SVDDL	SP
45	FX0TXP	AO
46	FX0TXN	AO
47	FX0RXP	AI
48	FX0RXN	AI
49	SVDDL	SP
50	FX1TXP	AO
51	FX1TXN	AO
52	FX1RXP	AI
53	FX1RXN	AI
54	SVDDH	SP
55	SVDDL	SP
56	SVDDL	SP
57	FX2TXP	AO
58	FX2TXN	AO
59	FX2RXP	AI
60	FX2RXN	AI
61	SVDDL	SP
62	FX3TXP	AO
63	FX3TXN	AO
64	FX3RXP	AI
65	FX3RXN	AI
66	NC	-
67	DVDDH	P
68	NC	-
69	NC	-
70	DVDDL	P
71	MDIO	IO/PU
72	MDC	I/PD

NO.	Name	TYPE
73	RESET_N	I/PU
74	AVDDH	AP
75	RBIAS	AO
76	AVDDL	AP
77	DVDDL	P
78	CHIP_MODE3	LI/PD
79	CHIP_MODE2	LI/PD
80	CHIP_MODE1/SYNC_LOCK	LI/O/PU
81	CHIP_MODE0/SYNCE	LI/O/PD
82	TEST_MD_CP	I
83	DVDDH	P
84	NC	-
85	XTAL_SEL	LI/PD
86	NC	-
87	SVDDL	SP
88	NC	-
89	EPAD	G

2.2.2. QSGMII Interface Pins

Table 2. QSGMII Interface Pins

Pin Name	Pin No.	Type	Description
S0TXP	2	AO	these two pins are used for QSGMII Differential Output. 5GHz serial interfaces to transfer data to an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0TXN	1	AO	
S0RXP	6	AI	these two pins are used for QSGMII Differential Input. 5GHz serial interfaces to receive data from an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor.
S0RXN	5	AI	

2.2.3. 1.25G SERDES Interface Pins

Table 3. 1.25G SERDES Interface Pins

Pin Name	Pin No.	Type	Description
FX0RXP	47	AI	Port 0 SERDES Receiver Pair (1.25GHz Differential Signal Input).
FX0RXN	48		
FX0TXP	45	AO	Port 0 SERDES Transmit Pair (1.25GHz Differential Signal Output).
FX0TXN	46		
FX1RXP	52	AI	Port 1 SERDES Receiver Pair (1.25GHz Differential Signal Input).
FX1RXN	53		
FX1TXP	50	AO	Port 1 SERDES Transmit Pair (1.25GHz Differential Signal Output).
FX1TXN	51		
FX2RXP	59	AI	Port 2 SERDES Receiver Pair (1.25GHz Differential Signal

FX2RXN	60		Input).
FX2TXP	57	AO	Port 2 SERDES Transmit Pair (1.25GHz Differential Signal Output).
FX2TXN	58		
FX3RXP	64	AI	Port 3 SERDES Receiver Pair (1.25GHz Differential Signal Input).
FX3RXN	65		
FX3TXP	62	AO	Port 3 SERDES Transmit Pair (1.25GHz Differential Signal Output).
FX3TXN	63		
FX0_TX_DIS	37	O/PU	Port 0 100BASE-FX/1000BASE-X Transmit Optical module Power Control
FX1_TX_DIS	38	O/PU	Port 1 100BASE-FX/1000BASE-X Transmit Optical module Power Control
FX2_TX_DIS	39	O/PU	Port 2 100BASE-FX/1000BASE-X Transmit Optical module Power Control
FX3_TX_DIS	40	O/PU	Port 3 100BASE-FX/1000BASE-X Transmit Optical module Power Control

2.2.4. Configuration Pins

Table 2. Configuration Pins

Pin Name	Pin No.	Type	Description
PHYADDR0/ LED0	29	LI/O/PD	PHYADDR0, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. After power-up or reset its function is default port0 port LED indictor. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR1/ LED1	30	LI/O/PD	PHYADDR1, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. After power-up or reset its function is default port1 port LED indictor. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR2/ LED2	31	LI/O/PD	PHYADDR2, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. After power-up or reset its function is default port2 port LED indictor.

			Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.
PHYADDR3/ LED3	32	LI/O/PD	PHYADDR3, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. After power-up or reset its function is default port3 port LED indictor. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
PHYADDR4	33	LI/PD	PHYADDR4, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
CHIP_MODE3	78	LI/PD	CHIP MODE [3:0] refer to: 4'b0001, QSGMII + 1000BASE-X/100BASE-FX x4 mode, each port can also be set to SGMII_MAC separately by extend register. 4'b0010, QSGMII + SGMII_MAC x4 mode 4'b1100, QSGMII + SGMII_PHY x4 mode Other option is reserved. In addition, PIN 80 have sync lock indictor funcution and PIN 81 is SYNCE clock output.
CHIP_MODE2	79	LI/PD	
CHIP_MODE1/ SYNC_LOCK	80	LI/O/PU	
CHIP_MODE0/ SYNCE	81	LI/O/PD	
XTAL_SEL	85	LI/PD	Crytstal/Oscillator frequency select. 1'b0: 25MHz 1'b1: 50MHz

2.2.5. Miscellaneous Pins

Table 3. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
MDC	72	I/PD	MII Management Interface Clock Input. The clock reference for the MII management interface. The maximum frequency support is 12.5MHz.
MDIO	71	IO/PU	MII Management Interface Data Input/Output. MDIO transfer management data in and out of the device synchronous to the rising edge of MDC.

INTERRUPT	34	OD/PU	Interrupt output when Interrupt event occurs, active low. Always open drain, must pull-up to DVDDH via a 4.7K resistor.
RESET_N	73	I/PU	Hardware Reset (Active Low Reset Signal). To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled high for normal operation.
RBIAS	75	AO	Bias Resistor. An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND
XTALI	26	XT	25MHz Crystal Clock Input. 25MHz±50ppm tolerance crystal reference or oscillator input. When using a crystal, connect a loading capacitor from each pad to ground. When either using an oscillator or driving an external 25MHz clock from another device, XTALO should be kept floating. The maximum XTALI input voltage is 3.3V.
XTALO	27	XT	25Mhz Crystal Clock Output. 25MHz±50ppm tolerance crystal output. Refer to XTALI.
TEST_MD_CP	82	I	Reserved for chip manufacturing tests.Pull Down for normal operation. Suggested pull-down to GND via a 4.7K resistor.
NC	3,4,7,9 11,13,14,15 16,17,18,19 20,21,22,23 24,66,68,69 ,84,86,88	-	NC pins and keep floating. PIN68 is internally connected to DVDDH, it must be kept floating and other NC pins is not connected to any signal.

2.2.6. Power and GND Pins

Table 4. Power and GND Pins

Pin Name	Pin No.	Type	Description
AVDDH	28,74	AP	Analog High Voltage Power
AVDDL	25,76	AP	Analog Low Voltage Power
SVDDH	12,54	SP	SerDes High Voltage Power
SVDDL	8,10,44,49 55,56,61,87	SP	SerDes Low Voltage Power

DVDDH	35,36,43,67,83	P	Digital High Voltage Power
DVDDL	41,42,70,77	P	Digital Low Voltage Power
GND	EPAD	G	Digital/Analog Ground

3. Operational Description

3.1. Clock Selection

YT8614Q can be set to 25MHz or 50MHz reference clock input by setting pin85 XTAL_SEL . It uses 25MHz clock by default. If you use 50MHz clock, you must pull up XTAL_SEL PIN.

Table 5. Mode selection

XTAL_SEL	Clock frequency selection
Pull down(Default)	25MHz
Pull up	50MHz

3.2. Reset

YT8614Q have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up. RESET_N is also used for power on strapping. During RESET_N is active, YT8614 latches input value on strapping. Strapping is used as configuration information which provides flexibility in application without mdio access.

Table 6. Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms

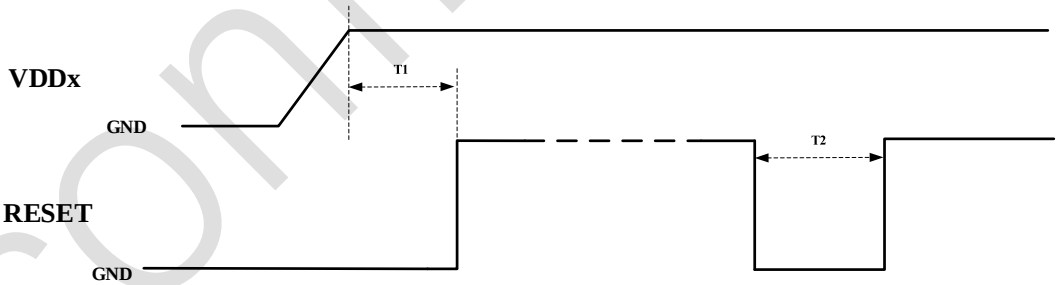


Figure 3. Reset Timing Diagram

3.3. PHY Address

For YT8614Q, Strapping PHYADDR[4:0] is used to generate phy address port 0. The other port's phy address is the sum of the PHYADDR [4:0] and port number. For example, if PHYADDR [4:0] = 8, the phy address of port 3 is 11 (the sum of 8 and 3)

3.4. Mode Selection

The CHIP_MODE[3:0] pins must be set to allow the YT8214Q to operate correctly. After power on or hardware reset, the setting values are latched and each 1.25G serdes is configured to corresponding mode.

Table 7. Mode selection

CHIP_MODE[3:0]	Mode	Description
4'b0001	QSGMII + 1000BASE-X/100BASE-FX x 4	Four fiber ports can also be set to SGMII_MAC separately by extend register 0xA019.
4'b0010	QSGMII + SGMII_MAC x 4	
4'b1100	QSGMII + SGMII_PHY x 4	
Other option	reserved	

3.5. Sync-E Clock Output

YT8614Q provides Synchronous Ethernet (Sync-E) clock output. Sync-E clock can output from SYNCE (pin 81). The Sync-E clock sources can be configured to recovery from QSGMII, or Fiber0~3 respectively. When SYNCE is locked, the SYNC_LOCK (pin 80) will be high if its extenal pull down, and be low if its external pull up.

The recovery clock for Sync-E can be either a 125MHz, 31.25MHz or 25MHz clock. It can also output 25MHz reference clock.

3.6. Interrupt

YT8614Q provides an active low interrupt output pin (INT_N) based on change of the PHY status.Every interrupt condition is represented by the read-only general interrupt status register (EXT_0xA011,0xA015).

The interrupts can be individually enable or disable by setting or clearing bits in the interrupt enable register(EXT_0xA010,0xA014).

Note 1: The interrupt of the YT8614Q is a level-triggered mechanism.

Note 2: The interrupt output pin (INT_N) is open drain mode, and must pull-up to DVDDIO via a 4.7K resistor.

3.7. LED

YT8614Q supports parallel LED mode, but The LED is turned off by default . LED0~LED3 correspond to the LED indicator of port0~port3 respectively .If you use the LED indicator, you must set common ext register 0xa004[15:12] to 4'b1111(LED3~LED0).

3.8. Management Interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and YT8614Q also support MDC clock rates up to 12.5 MHz.

4. Register Overview

4.1. Common EXT Register

4.1.1. SMI mux (0xA000)

Table 8. SMI mux (0xA000)

Bit	Symbol	Access	Default	Description
15:13	Reserved	RO	0x0	Reserved
12:8	MDIO_PHYAD	RO	0x0	the PHYAD field in current MDIO command
7:4	Reserved	RO	0x0	Reserved
3	en_brdst_q	RW	0x0	when bit1 smi_sds_phy is 1, this bit controls to broadcast write to all QSGMII channels. 1 enable froadcast write; 0 disable.
2	en_brdst_sf	RW	0x0	when bit1 smi_sds_phy is 1, this bit controls to broadcast write to all SGMIIs. 1 enable froadcast write; 0 disable.
1	Smi_sds_phy	RO	0x1	always1, 1 to access sds
0	smi_sf	RW	0x0	when smi_sds_phy is 1, this bit controls to access whether sds 0/1/2/3 (SGMII) register or sds 0 (QSGMII) register. 1 to access SGMII register; 0 to access QSGMII register.

4.1.2. LED enable (0xA004)

Table 9. LED enable (0xA000)

Bit	Symbol	Access	Default	Description
15	LED3_EN	RW	0x0	1: enable LED3 indicator 0: disable LED3 indicator
14	LED2_EN	RW	0x0	1: enable LED2 indicator 0: disable LED2 indicator
13	LED1_EN	RW	0x0	1: enable LED1 indicator 0: disable LED1 indicator
12	LED0_EN	RO	0x1	1: enable LED0 indicator 0: disable LED0 indicator
11:0	Reserved	RW	0x0	Reserved

4.1.3. SYNCE0 cfg (0xA006)

Table 10. SYNCE0 cfg (0xA006)

Bit	Symbol	Access	Default	Description
15	sync_clk_en_0	RW	0x0	1=enable to output the synce_clk0 to the PAD

				SYNC0
14	bp_sync_lock_gating_0	RW	0x0	When synce_clk0 is not locked, this bit controls whether to output the synce_clk0 or crystal clock to the PAD SYNC0 1: to output; 0: to not output.
13	sel_synce_125m_0	RW	0x0	bit13 and bit10 controls the synce_clk0's frequence and source: {sel_synce_125m_0, sel_clk_25m_xtl_0}, 2'b00: output 25MHz syncE clock; 2'b01: output 31.25MHz syncE clock; 2'b10: output 125MHz syncE clock; 2'b11: output 25MHz reference clock.
12:11	reserved	RO	0x0	always 0.
10	sel_clk_25m_xtl_0	RW	0x0	refer to bit13 sel_synce_125m_0 for detail.
9	sel_rclk_sds1_0	RW	0x0	Reserved
8	sel_rclk_sds0_0	RW	0x0	Synce_clk0 sourced from the 5G serdes. Bit8:4, select the source of the synce_clk0 from the recovered RX clocks. MSB has the higher priority, for example, bit8:4=18h means to output the 5G serdes's RX recovered clock; bit8:4=03h means to output the fiber/SGMII port 2's RX recovered clock.
7	sel_rclk_phy7_0	RW	0x0	Synce_clk0 sourced from the fiber/SGMII port3.
6	sel_rclk_phy6_0	RW	0x0	Synce_clk0 sourced from the fiber/SGMII port2.
5	sel_rclk_phy5_0	RW	0x0	Synce_clk0 sourced from the fiber/SGMII port1.
4	sel_rclk_phy4_0	RW	0x0	Synce_clk0 sourced from the fiber/SGMII port0.
3	sel_rclk_phy3_0	RW	0x0	Reserved
2	sel_rclk_phy2_0	RW	0x0	Reserved
1	sel_rclk_phy1_0	RW	0x0	Reserved
0	sel_rclk_phy0_0	RW	0x0	Reserved

4.1.4. chip_mode (0xA007)

Table . chip_mode (0xA007)

Bit	Symbol	Access	Default	Description
15:13	package_id	RO	0x0	strapping from input pad {1'0,PACKAGE_ID1,PACKAGE_ID0}
12	en_phy	RW POS	0x1	1: enable all the fiber/SGMII serdes ports; 0: disable all the fiber/SGMII serdes ports.
11:6	reserved	RO	0x0	always 0.

5	en_pwron_light	RW POS	0x1	make SLEDs or direct LEDs light for 200ms after hardware reset or power on reset.
4	reserved	RO	0x0	always 0.
3:0	chip_mode	RW POS	0x4	4'b0001, QSGMII to 1000BASE-X or SGMII_MAC x 4 (4 fiber ports' speed are programed via extended register A009h bit3:0 respectively when 100BASE-FX auto sensing is closed; force SGMII_MAC by ext reg a019 bit [3:0]); 4'b0010, Qsgmii x1(PHY) to SGMII_MAC x4 mode; 4'b1100, Qsgmii x1(MAC) to SGMII_PHY x4 mode; Other option is reserved

4.1.5. fiber speed cfg (0xA009)

Table 11. fiber speed cfg (0xA009)

Bit	Symbol	Access	Default	Description
15:12	reserved	RO	0x6	None
11	cmb3_rem_phy_lpbk_fib	RW	0x0	1: control to set the figer/SGMII serdes port3 to remote loopbakc mode.
10	cmb2_rem_phy_lpbk_fib	RW	0x0	1: control to set the figer/SGMII serdes port2 to remote loopbakc mode.
9	cmb1_rem_phy_lpbk_fib	RW	0x0	1: control to set the figer/SGMII serdes port1 to remote loopbakc mode.
8	cmb0_rem_phy_lpbk_fib	RW	0x0	1: control to set the figer/SGMII serdes port0 to remote loopbakc mode.
7:4	Reserved	RW	0x0	Reserved
3	s3_fib_speed_sel	RW	0x1	select the speed mode of 1.25G serdes #3 when it works as fiber and auto-sensing is disabled. 1: 1000BASE-X; 0: 100BASE-FX.
2	s2_fib_speed_sel	RW	0x1	select the speed mode of 1.25G serdes #2 when it works as fiber and auto-sensing is disabled. 1: 1000BASE-X; 0: 100BASE-FX.
1	s1_fib_speed_sel	RW	0x1	select the speed mode of 1.25G serdes #1 when it works as fiber and auto-sensing is disabled. 1: 1000BASE-X; 0: 100BASE-FX.
0	s0_fib_speed_sel	RW	0x1	select the speed mode of 1.25G serdes #0 when it works as fiber and auto-sensing is disabled. 1: 1000BASE-X; 0: 100BASE-FX.

4.1.6. PHY Link Up/Down INTn Mask (0xA010)

Table 12. PHY Link Up/Down INTn Mask (0xA010)

Bit	Symbol	Access	Default	Description
15	phy7_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 1.25G SerDes #port3 link up int 1: to enable the interrupt.
14	phy6_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 1.25G SerDes #port2 link up int 1: to enable the interrupt.
13	phy5_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 1.25G SerDes #port1 link up int 1: to enable the interrupt.
12	phy4_link_up_int_mask	RW	0x0	the interrupt mask bit for EXT A011 1.25G SerDes #port0 link up int 1: to enable the interrupt.
11	phy3_link_up_int_mask	RW	no use	reserved
10	phy2_link_up_int_mask	RW	no use	reserved
9	phy1_link_up_int_mask	RW	no use	reserved
8	phy0_link_up_int_mask	RW	no use	reserved
7	phy7_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 1.25G SerDes #port3 link down int 1: to enable the interrupt.
6	phy6_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 1.25G SerDes #port2 link down int 1: to enable the interrupt.
5	phy5_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 1.25G SerDes #port1 link down int 1: to enable the interrupt.
4	phy4_link_down_int_mask	RW	0x0	the interrupt mask bit for EXT A011 1.25G SerDes #port0 link down int 1: to enable the interrupt.
3	phy3_link_down_int_mask	RW	no use	reserved
2	phy2_link_down_int_mask	RW	no use	reserved
1	phy1_link_down_int_mask	RW	no use	reserved
0	phy0_link_down_int_mask	RW	no use	reserved

4.1.7. PHY Link Up/Down INTn Status (0xA011)

Table 13. PHY Link Up/Down INTn Status (0xA011)

Bit	Symbol	Access	Default	Description
15	phy7_link_up_int	RO	0x0	it's the 1.25G SerDes #port3 link up interrupt

				status.
14	phy6_link_up_int	RO	0x0	it's the 1.25G SerDes #port2 link up interrupt status.
13	phy5_link_up_int	RO	0x0	it's the 1.25G SerDes #port1 link up interrupt status.
12	phy4_link_up_int	RO	0x0	it's the 1.25G SerDes #port0 link up interrupt status.
11	phy3_link_up_int	RO	no use	reserved
10	phy2_link_up_int	RO	no use	reserved
9	phy1_link_up_int	RO	no use	reserved
8	phy0_link_up_int	RO	no use	reserved
7	phy7_link_down_int	RO	0x0	it's the 1.25G SerDes #port3 link down interrupt status.
6	phy6_link_down_int	RO	0x0	it's the 1.25G SerDes #port2 link down interrupt status.
5	phy5_link_down_int	RO	0x0	it's the 1.25G SerDes #port1 link down interrupt status.
4	phy4_link_down_int	RO	0x0	it's the 1.25G SerDes #port0 link down interrupt status.
3	phy3_link_down_int	RO	no use	reserved
2	phy2_link_down_int	RO	no use	reserved
1	phy1_link_down_int	RO	no use	reserved
0	phy0_link_down_int	RO	no use	reserved

4.1.8. QSGMII Legacy Interrupt Mask (0xA014)

Table 14. QSGMII Legacy Interrupt Mask (0xA014)

Bit	Symbol	Access	Default	Description
15	q1_ch3_link_up_int_mask	RO	no use	reserved
14	q1_ch2_link_up_int_mask	RO	no use	reserved
13	q1_ch1_link_up_int_mask	RO	no use	reserved
12	q1_ch0_link_up_int_mask	RO	no use	reserved
11	q0_ch3_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch3_link_up_int. 1: to enable the interrupt.
10	q0_ch2_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch2_link_up_int. 1: to enable the interrupt.
9	q0_ch1_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch1_link_up_int. 1: to enable the interrupt.
8	q0_ch0_link_up_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch0_link_up_int. 1: to enable the interrupt.
7	q1_ch3_link_down_int_mask	RO	no use	reserved

6	q1_ch2_link_down_int_mask	RO	no use	reserved
5	q1_ch1_link_down_int_mask	RO	no use	reserved
4	q1_ch0_link_down_int_mask	RO	no use	reserved
3	q0_ch3_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch3_link_down_int. 1: to enable the interrupt.
2	q0_ch2_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch2_link_down_int. 1: to enable the interrupt.
1	q0_ch1_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch1_link_down_int. 1: to enable the interrupt.
0	q0_ch0_link_down_int_mask	RO	0x0	the interrupt mask bit for EXT 0xA015 q0_ch0_link_down_int. 1: to enable the interrupt.

4.1.9. QSGMII Legacy Interrupt Status (0xA015)

Table 15. QSGMII Legacy Interrupt Status (0xA015)

Bit	Symbol	Access	Default	Description
15	q1_ch3_link_up_int	RO	no use	reserved
14	q1_ch2_link_up_int	RO	no use	reserved
13	q1_ch1_link_up_int	RO	no use	reserved
12	q1_ch0_link_up_int	RO	no use	reserved
11	q0_ch3_link_up_int	RO	0x0	It's the QSGMII channel 3 link up interrupt status.
10	q0_ch2_link_up_int	RO	0x0	It's the QSGMII channel 2 link up interrupt status.
9	q0_ch1_link_up_int	RO	0x0	It's the QSGMII channel 1 link up interrupt status.
8	q0_ch0_link_up_int	RO	0x0	It's the QSGMII channel 0 link up interrupt status.
7	q1_ch3_link_down_int	RO	no use	reserved
6	q1_ch2_link_down_int	RO	no use	reserved
5	q1_ch1_link_down_int	RO	no use	reserved
4	q1_ch0_link_down_int	RO	no use	reserved
3	q0_ch3_link_down_int	RO	0x0	It's the QSGMII channel 3 link down interrupt status.
2	q0_ch2_link_down_int	RO	0x0	It's the QSGMII channel 2 link down interrupt status.
1	q0_ch1_link_down_int	RO	0x0	It's the QSGMII channel 1 link down interrupt status.

0	q0_ch0_link_down_int	RO	0x0	It's the QSGMII channel 0 link down interrupt status.

4.1.10. Force sds to sgmac(0xA019)

Table . fiber speed cfg (0xA009)

Bit	Symbol	Access	Default	Description
15:4	Reserved	RO	0x0	always 0.
3	s3_force_sgmac	RW	0x0	when chip mode= 4'b0001, set firer/SGMII port3 to SGMII MAC mode
2	s2_force_sgmac	RW	0x0	when chip mode= 4'b0001, set firer/SGMII port2 to SGMII MAC mode
1	s1_force_sgmac	RW	0x0	when chip mode= 4'b0001, set firer/SGMII port1 to SGMII MAC mode
0	s0_force_sgmac	RW	0x0	when chip mode= 4'b0001, set firer/SGMII port0 to SGMII MAC mode

4.1.11. pkg_cfg0 (0xA0a0)

Table 16. pkg_cfg0 (0xA0a0)

Bit	Symbol	Access	Default	Description
15	u0_pkg_chk_en	RW	0x0	1: to enable RX/TX package checker. For RX checker, if ext.A0B7.15=0, RX checker checks the Fiber/SGMII port's GMII RX data,else checks the 5G Serdes' RX data;
14	u0_pkg_en_gate	RW	0x1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;
13	u0_bp_pkg_gen	RW	0x1	1: normal function; 0: test function, the TX data is sourced from pkg_gen;
12	u0_pkg_gen_en	RW SC	0x0	1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0.
11:8	u0_pkg_prm_lth	RW	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	u0_pkg_ipg_lth	RW	0xc	The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	u0_Xmit_mac_force_gen	RW	0x0	1: To enable pkg_gen to send out the generated data even when the link is not established.

2	u0_pkg_corrupt_crc	RW	0x0	1: to make pkg_gen to send out CRC error packages.
1:0	u0_pkg_payload	RW	0x0	Control the payload of the generated packages.

4.1.12. pkg_cfg1 (0xA0a1)

Table 17. pkg_cfg1 (0xA0a1)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_length	RW	0x40	To set the length of the generated packages.

4.1.13. pkg_cfg2 (0xA0a2)

Table 18. pkg_cfg2 (0xA0a2)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_burst_size	RW	0x0	To set the number of packages in a burst of package generation.

4.1.14. pkg_rx_valid0 (0xA0a3)

Table 19. pkg_rx_valid0 (0xA0a3)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_valid_high	RO RC	0x0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

4.1.15. pkg_rx_valid1 (0xA0a4)

Table 20. pkg_rx_valid1 (0xA0a4)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_valid_low	RO RC	0x0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

4.1.16. pkg_rx_os0 (0xA0a5)

Table 21. pkg_rx_os0 (0xA0a5)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_os_good_high	RO RC	0x0	Pkg_ib_os_good[31:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

4.1.17. pkg_rx_os1 (0xA0a6)

Table 22. pkg_rx_os1 (0xA0a6)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_os_good_low	RO RC	0x0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the

				number of RX packages from wire whose CRC are good and length are >1518Byte.

4.1.18. pkg_rx_us0 (0xA0a7)

Table 23. pkg_rx_us0 (0xA0a7)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_us_good_high	RO RC	0x0	Pkg_ib_us_good[31:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

4.1.19. pkg_rx_us1 (0xA0a8)

Table 24. pkg_rx_us1 (0xA0a8)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_us_good_low	RO RC	0x0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

4.1.20. pkg_rx_err (0xA0a9)

Table 25. pkg_rx_err (0xA0a9)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_err	RO RC	0x0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

4.1.21. pkg_rx_os_bad (0xA0aa)

Table 26. pkg_rx_os_bad (0xA0aa)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_os_bad	RO RC	0x0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >1518Byte.

4.1.22. pkg_rx_fragment (0xA0ab)

Table 27. pkg_rx_fragment (0xA0ab)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_frag	RO RC	0x0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

4.1.23. pkg_rx_nosfd (0xA0ac)

Table 28. pkg_rx_nosfd (0xA0ac)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_nosfd	RO RC	0x0	pkg_ib_nosfd is the number of RX packages

				from wire whose SFD is missed.

4.1.24. pkg_tx_valid0 (0xA0ad)

Table 29. pkg_tx_valid0 (0xA0ad)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_valid_high	RO RC	0x0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

4.1.25. pkg_tx_valid1 (0xA0ae)

Table 30. pkg_tx_valid1 (0xA0ae)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_valid_low	RO RC	0x0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

4.1.26. pkg_tx_os0 (0xA0af)

Table 31. pkg_tx_os0 (0xA0af)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_good_high	RO RC	0x0	Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

4.1.27. pkg_tx_os1 (0xA0b0)

Table 32. pkg_tx_os1 (0xA0b0)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_good_low	RO RC	0x0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

4.1.28. pkg_tx_us0 (0xA0b1)

Table 33. pkg_tx_us0 (0xA0b1)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_us_good_high	RO RC	0x0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

4.1.29. pkg_tx_us1 (0xA0b2)

Table 34. pkg_tx_us1 (0xA0b2)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_us_good_low	RO RC	0x0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

4.1.30. pkg_tx_err (0xA0b3)

Table 35. pkg_tx_err (0xA0b3)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_err	RO RC	0x0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

4.1.31. pkg_tx_os_bad (0xA0b4)

Table 36. pkg_tx_os_bad (0xA0b4)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_bad	RO RC	0x0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >1518Byte.

4.1.32. pkg_tx_fragment (0xA0b5)

Table 37. pkg_tx_fragment (0xA0b5)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_frag	RO RC	0x0	pkg_ob_frag is the number of TX packages from MII whose length are <64Byte.

4.1.33. pkg_tx_nosfd (0xA0b6)

Table 38. pkg_tx_nosfd (0xA0b6)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_nosfd	RO RC	0x0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

4.1.34. pkg_cfg3 (0xA0b7)

Table 39. pkg_cfg3 (0xA0b7)

Bit	Symbol	Access	Default	Description
15	u0_pkgchk_rxsrc_sel	RW	0x0	control RX checker's data source. =0, RX checker checks the Fiber/SGMII port's RX data, =1, it checks QSGMII's RX data
14	u0_pkgchk_txsrc_sel	RW	0x0	When ext.A0b7.10 is 0, it controls TX checker's

				data source. =0, TX checker checks Fiber/SGMII port's TX data; =1, it checks QSGMII's TX data. It is not valid when ext.A0b7.10 is 1.
13	u0_pkgen_txdir_sel	RW	0x0	Control the media the data generated by pkg_gen sent to; 0=to Fiber/SGMII port; 1=to QSGMII
12	u0_en_pkgen_da_sa	RW	0x0	1: set the DA/SA of the packet generated by pkg_gen to a programmed value; For DA, if EXT 0xA0B7 bit[11] is 1, the DA is set to broadcase address FF-FF-FF-FF-FF-FF; else, the DA is set to fix value, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by EXT 0xA0B9 bit[15:8]. For SA, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by EXT 0xA0B9 bit[7:0]. 0: the DA/SA is not programmed value
11	u0_pkg_brdcst	RW	0x0	Valid when EXT 0xA0B7 bit12 is 1. 1: set the DA to broadcase address FF-FF-FF-FF-FF-FF 0: set the DA to a fixed programmed value.
10	u0_pkgchk_txsrc_pkgen	RW	0x0	1'b1: the package checker on TX side will check the tx data generated by pkg_gen; 1'b0: the package checker on TX side will check the tx data of Fiber/SGMII port or QSGMII.
9	u0_pkg_en_az	RW	0x0	1: enable to generate and send out LPI pattern during IPG;
8:0	u0_pkg_in_az_t	RW	0x1ff	control the time dewll in LPI;

4.1.35. led cfg (0xA7ba)

Table 40. led cfg (0xA7ba)

Bit	Symbol	Access	Default	Description
15:14	reserved	RO	0x0	Reserved
13	Led_act_blk_ind_1	RW	0x0	When traffic is present, make LED1 BLINK no matter the previous LED status is ON or OFF, or make LED1 blink only when the previous LED status is ON.
12	Led_fdx_on_en_1	RW	0x0	1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED will be ON.
11	Led_hdx_on_en_1	RW	0x0	1: If BLINK status is not activated, when PHY

				link up and duplex mode is half duplex, LED will be ON.
10	Led_txact_blk_en_1	RW	0x1	1: If bit13 is 1, or bit13 is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, LED will be BLINK.
9	Led_rxact_blk_en_1	RW	0x1	If bit13 is 1, or bit13 is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, LED will be BLINK.
8	Led_txact_on_en_1	RW	0x0	1 = if BLINK status is not activated, when PHY link up and TX is active, make LED1 ON at least 10ms;
7	Led_rxact_on_en_1	RW	0x0	1 = if BLINK status is not activated, when PHY link up and RX is active, make LED1 ON at least 10ms;
6	Led_gt_on_en_1	RW	0x1	1 = if BLINK status is not activated, when PHY link up and speed mode is 1000Mbps, make LED1 ON;
5	Led_ht_on_en_1	RW	0x1	1 = if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED1 ON;
4	Led_bt_on_en_1	RW	0x1	1 = if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED1 ON;
3	Led_col_blk_en_1	RW	0x0	1 = if PHY link up and collision happen, make LED1 BLINK;
2	Led_gt_blk_en_1	RW	0x0	1 = if PHY link up and speed mode is 1000Mbps, make LED1 BLINK;
1	Led_ht_blk_en_1	RW	0x0	1 = if PHY link up and speed mode is 100Mbps, make LED1 BLINK;
0	Led_bt_blk_en_1	RW	0x0	1 = if PHY link up and speed mode is 10Mbps, make LED1 BLINK;

4.1.36. led cfg (0xA7bb)

Table 41. led cfg (0xA7bb)

Bit	Symbol	Access	Default	Description
15:0	led cfg port 1	RW	0x670	bit defination same with a7ba

4.1.37. led cfg (0xA7bc)

Table 42. led cfg (0xA7bc)

Bit	Symbol	Access	Default	Description

15:0	led cfg port 2	RW	0x670	bit defination same with a7ba

4.1.38. led cfg (0xA7bd)

Table 43. led cfg (0xA7bd)

Bit	Symbol	Access	Default	Description
15:0	led cfg port 3	RW	0x670	bit defination same with a7ba

4.1.39. led cfg (0xA7be)

Table 44. led cfg (0xA7be)

Bit	Symbol	Access	Default	Description
15	reserved	RO	0x0	reserved
14	led_force_en_3	RW	0x0	Led3 force mode enable.
13;12	led_force_ctrl_3	RW	0x0	Valid when bit14 is set. 00: force LED OFF; 01: force LED ON; 10: force LED Blink at BLINK Mode1; 11: force LED Blink at BLINK Mode2. LED could blinks at different frequency in BLINK Mode1 and BLINK Mode2. Refer to EXT A7BF[3:0] for the BLINK Mode2 and BLINK Mode1.
11	reserved	RO	0x0	Reserved
10	led_force_en_2	RW	0x0	Led2 force mode enable.
9:8	led_force_ctrl_2	RW	0x0	Valid when bit10 is set. 00: force LED OFF; 01: force LED ON; 10: force LED Blink at BLINK Mode1; 11: force LED Blink at BLINK Mode2. LED could blinks at different frequency in BLINK Mode1 and BLINK Mode2. Refer to EXT A7BF[3:0] for the BLINK Mode2 and BLINK Mode1.
7	reserved	RO	0x0	Reserved
6	led_force_en_1	RW	0x0	Led1 force mode enable.
5:4	led_force_ctrl_1	RW	0x0	Valid when bit6 is set. 00: force LED OFF; 01: force LED ON; 10: force LED Blink at BLINK Mode1; 11: force LED Blink at BLINK Mode2. LED could blinks at different frequency in

				BLINK Mode1 and BLINK Mode2. Refer to EXT A7BF[3:0] for the BLINK Mode2 and BLINK Mode1.
3	reserved	RO	0x0	Reserved
2	led_force_en_0	RW	0x0	Led0 force mode enable.
1:0	led_force_ctrl_0	RW	0x0	Valid when bit2 is set. 00: force LED OFF; 01: force LED ON; 10: force LED Blink at BLINK Mode1; 11: force LED Blink at BLINK Mode2. LED could blinks at different frequency in BLINK Mode1 and BLINK Mode2. Refer to EXT A7BF[3:0] for the BLINK Mode2 and BLINK Mode1.

4.1.40. led cfg (0xA7bf)

Table 45. led cfg (0xA7bf)

Bit	Symbol	Access	Default	Description
15:7	reserved	RO	0x0	Reserved
6:4	led_duty_0	RW	0x0	Select duty cycle of BLINK: 000: 50% ON and 50% OFF; 001: 67% ON and 33% OFF; 010: 75% ON and 25% OFF; 011: 83% ON and 17% OFF; 100: 50% ON and 50% OFF; 101: 33% ON and 67% OFF; 110: 25% ON and 75% OFF; 111: 17% ON and 83% OFF.
3:2	led_freq2_0	RW	0x1	Select frequency of BLINK Mode2: 00: 4Hz; 01: 8Hz; 10: 16Hz; 11: 32Hz.
1:0	led_freq1_0	RW	0x2	Select frequency of BLINK Mode2: 00: 4Hz; 01: 8Hz; 10: 16Hz; 11: 32Hz.

4.2. 1.25G 5G Sds MII Register

4.2.1. Basic control register (0x00)

Table 46. Basic control register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.
14	Loopback	RW	0x0	Internal loopback control
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero.
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation;
11	Power_down	RW	0x0	1 = Power down
10	Isolate	RW	0x0	Isolate phy from RGMII/SGMII/FIBER.
9	Re_Autoneg	RW SC	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART.
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.
7	Collision_Test	RW	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.
6	Speed_ Selection(MSB)	RW	0x1	See bit13.
5	mr_undirectional	RW	0x0	1 = PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established
4:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

4.2.2. Basic status register (0x01)

Table 47. Basic status register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x0	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x0	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x0	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x1	Whether support EXTended status register in 0Fh
7	Unidirect_Ability	RO	0x1	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed
5	Autoneg_Complete	RO	0x0	1'b0: Auto-negotiation process not completed
4	Remote_Fault	RO RC SWC LH	0x0	1'b0: no remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation
2	Link_Status	RO SWC LL	0x0	Link status
1	Jabber_Detect	RO	0x0	always 0
0	Extended_Capability	RO	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh

4.2.3. Sds identification register1 (0x02)

Table 48. Sds identification register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x4f51	Bits 3 to 18 of the Organizationally Unique Identifier

4.2.4. Sds identification register2 (0x03)

Table 49. Sds identification register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x3a	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0xa	6 bits manufacturer's type number

3:0	Revision_No	RO	0x9	4 bits manufacturer's revision number

4.2.5. Auto-Negotiation advertisement (0x04)

Table 50. Auto-Negotiation advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
14	Ack	RO	0x0	Always 0
13:12	Remote_Fault	RO	0x0	Always 0
11:9	Reserved	RO	0x0	Reserved
8	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
7	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
6	Half_duplex	RW	0x0	Half duplex ability
5	Full_duplex	RW	0x1	Full duplex ability
4:0	Reserved	RO	0x0	Reserved

4.2.6. Auto-Negotiation link partner ability (0x05)

Table 51. Auto-Negotiation link partner ability (0x05)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO SWC	0x0	NEXT page. Received Code Word Bit 15
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14
13:12	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13:12
11:9	RESERVED	RO	0x0	Reserved. Received Code Word Bit 11:9
8:7	PAUSE	RO SWC	0x0	Pause. Received Code Word Bit 8:7
6	HALF_DUPLEX	RO SWC	0x0	Half duplex. Received Code Word Bit 6
5	FULL_DUPLEX	RO SWC	0x0	Full duplex. Received Code Word Bit 5
4:0	RESERVED	RO	0x0	Reserved. Received Code Word Bit 4:0

4.2.7. Auto-Negotiation expansion register (0x06)

Table 52. Auto-Negotiation expansion register (0x06)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	Local NEXT Page able	RO	0x0	1 = Local Device supports NEXT Page
1	Page received	RO RC LH	0x0	1 = A new page is received

0	Reserved	RO	0x0	Reserved

4.2.8. Auto-Negotiation NEXT Page register (0x07)

Table 53. Auto-Negotiation NEXT Page register (0x07)

Bit	Symbol	Access	Default	Description
15:0	NEXT Page	RO	0x0	always be 0

4.2.9. Auto-Negotiation link partner Received NEXT Page register (0x08)

Table 54. Auto-Negotiation link partner Received NEXT Page register (0x08)

Bit	Symbol	Access	Default	Description
15:0	Link Partner NEXT Page	RO	0x0	always be 0

4.2.10. Extended status register (0x0F)

Table 55. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x1	1 = PHY supports 1000BASE-X Full Duplex
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex.
13	1000BASE-T Full Duplex	RO	0x0	1 = PHY supports 1000BASE-T Full Duplex
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex
11:0	Reserved	RO	0x0	Always 0

4.2.11. Sds specific status register (0x11)

Table 56. Sds specific status register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
12:11	Pause	RO	0x0	Pause to mac
10	Link status real-time	RO	0x0	1 = Link up
9	Rx_lpi_active	RO	0x0	rx lpi is active
8	Duplex_error	RO	0x0	realtime duplex error
7	En_flowctrl_rx	RO	0x0	realtime en_flowctrl_rx
6	En_flowctrl_tx	RO	0x0	realtime en_flowctrl_tx
5:4	Ser_mode_cfg	RO	0x0	realtime serdes working mode. 00: SG_MAC; 01: SG_PHY; 10: FIB_1000; 11: FIB_100.
3:1	Xmit	RO	0x0	realtime transmit statemachine. 001: Xmit Idle; 010: Xmit Config; 100: Xmit Data.

0	Syncstatus	RO	0x0	realtime syncstatus

4.2.12. receive err counter mon (0x15)

Table 57. receive err counter mon (0x15)

Bit	Symbol	Access	Default	Description
15:0	error_counter_rx	RO SWC	0x0	receive error counter

4.2.13. lint fail counter mon (0x16)

Table 58. lint fail counter mon (0x16)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Link_fail_cnt	RO SWC RC	0x0	link fail counter

4.3. 1.25G Sds EXT Register

4.3.1. sds prbs cfg1 (0x05)

Table 59. sds prbs cfg1 (0x05)

Bit	Symbol	Access	Default	Description
15	En_prbs	RW	0x0	enable TX PRBS or self-defined pattern, the pattern type is determined by bit7:5 test_mode.
14	En_bert	RW	0x0	enable Bit Error Rate Test;
13	Prbs_invert	RW	0x0	TX error injection function, it has highest polarity than prbs_err_once and prbs_err_cont. 1: to send polarity inverted PRBS or self-defined pattern;
12	Prbs_err_cont	RW	0x0	TX error injection function, it has the lowest polarity.1: to inject error on TX pattern continuously and periodic, the period is controlled by prbs_err_rate.
11:10	Prbs_err_rate	RW	0x0	It's valid only when prbs_err_cont is 1. 2'b00: inject one error every 1024 cycles; 2'b01: inject one error every 2048 cycles; 2'b10: inject one error every 4096 cycles; 2'b11: inject one error every 8192 cycles;
9	Prbs_err_once	RW	0x0	TX error injection function.At the rising of this bit, to send polarity inverted PRBS or self-defined pattern for one cycle;
8	Test_mode_prbs31	RW	0x0	1: PRBS31, bit7:5 test_mode[2:0] has no effect.0: not PRBS31, bit7:5 test_mode[2:0] take effect then.

7:5	Test_mode	RW	0x0	Control the TX pattern in test mode: 0x0, PRBS7; 0x1, PRBS10; 0x2, Fix pattern, the fix pattern is controlled by Ext.6;0x3, 010101…; 0x4, 00110011…; 0x5, 00000_11111_00000_11111…; 0x6, 0000_0000_00_1111_1111_11…; 0x7, Increase pattern, 0->1023->0->1023…
4	Duration_check_en	RW	0x0	enable fixed number of bits check define in sds EXT BA/BB
3:2	Reserved	RO	0x0	Reserved
1	rx_crc_err	RO	0x0	pkg_chk crc_err latch
0	jumbo_enable	RW	0x0	jumbo package enable

4.3.2. sds prbs cfg2 (0x06)

Table 60. sds prbs cfg2 (0x06)

Bit	Symbol	Access	Default	Description
15:10	Reserved	RO	0x0	Reserved
9:0	Fix_pattern_9_0	RW	0x0	fix pattern transmited in test_mode 2

4.3.3. sds prbs mon1 (0x08)

Table 61. sds prbs mon1 (0x08)

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	0x0	Reserved
8	Err	RO	0x0	Err flag after PRBS has synchronized
7:2	Reserved	RO	0x0	Reserved
1	Bitsync_latch	RO LL	0x0	PRBS test synchronization status, once the sync is lost, this bit will latch low, until it's been read out.
0	Bitsync	RO	0x0	real time synchronization status

4.3.4. sds prbs mon2 (0x09)

Table 62. sds prbs mon2 (0x09)

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_15_0	RO	0x0	real time lowest 16 bits received error bit counter

4.3.5. sds prbs mon3 (0x0A)

Table 63. sds prbs mon3 (0x0A)

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_31_16	RO	0x0	real time highest 16 bits received error bit counter

4.3.6. analog cfg2 (0xA1)

Table 64. analog cfg2 (0xA1)

Bit	Symbol	Access	Default	Description
15:12	Tx_driver_stg2	RW	0xA	Amplitude control of TX driver, 4'b0000: min; 4'b1111: max
11	Tx_driver_stg1	RW	0x1	TX driver stage1 amplitude control
10:8	Tx_ckdiv10_con	RW	0x0	tx divide by 10 clock delay control
7:6	vb_tx_term	RW	0x0	not used
5	tx_vamp_post	RW	0x0	not used
4	tx_post_en	RW	0x0	Enable or disable TX de-emphasis. 1'b0: disable; 1'b1: enable
3:1	tx_driver_post	RO	0x7	Amplitude control of TX de-emphasis.3'b000: min; 3'b111: max
0	Tx_pd	RW	0x0	power down analog tx

4.4. 5G Sds EXT Register

4.4.1. sds prbs cfg1 (0x05)

Table 65. sds prbs cfg1 (0x05)

Bit	Symbol	Access	Default	Description
15	En_prbs	RW	0x0	enable TX PRBS or self-defined pattern, the pattern type is determined by bit7:5 test_mode.
14	En_bert	RW	0x0	enable Bit Error Rate Test;
13	Prbs_invert	RW	0x0	TX error injection function, it has highest polarity than prbs_err_once and prbs_err_cont. 1: to send polarity inverted PRBS or self-defined pattern;
12	Prbs_err_cont	RW	0x0	TX error injection function, it has the lowest polarity.1: to inject error on TX pattern continuously and periodic, the period is controlled by prbs_err_rate.
11:10	Prbs_err_rate	RW	0x0	It's valid only when prbs_err_cont is 1. 2'b00: inject one error every 1024 cycles; 2'b01: inject one error every 2048 cycles; 2'b10: inject one error every 4096 cycles; 2'b11: inject one error every 8192 cycles;
9	Prbs_err_once	RW	0x0	TX error injection function.At the rising of this bit, to send polarity inverted PRBS or self-defined pattern for one cycle;
8	Test_mode_prbs31	RW	0x0	1: PRBS31, bit7:5 test_mode[2:0] has no effect.0: not PRBS31, bit7:5 test_mode[2:0]

				take effect then.
7:5	Test_mode	RW	0x0	Control the TX pattern in test mode: 3'h0, PRBS7; 3'h1, PRBS10; 3'h2, Fix pattern, the fix pattern is controlled by Ext.6;3'h3, 010101…; 3'h4, 00110011…; 3'h5, 00000_11111_00000_11111…; 3'h6, 0000_0000_00_1111_1111_11…; 3'h7, Increase pattern, 0->1023->0->1023…
4	Duration_check_en	RW	0x0	enable fixed number of bits check defined in sds EXT BA/BB
3:0	Reserved	RO	0x0	Reserved

4.4.2. sds prbs cfg2 (0x06)

Table 66. sds prbs cfg2 (0x06)

Bit	Symbol	Access	Default	Description
15:0	Fix_pattern_15_0	RW	0x0	fix pattern transmited in test_mode 2

4.4.3. sds prbs cfg2 (0x07)

Table 67. sds prbs cfg2 (0x07)

Bit	Symbol	Access	Default	Description
15:4	Reserved	RO	0x0	Reserved
3:0	Fix_pattern_19_16	RW	0x0	fix pattern transmited in test_mode 2

4.4.4. sds prbs mon1 (0x08)

Table 68. sds prbs mon1 (0x08)

Bit	Symbol	Access	Default	Description
15:9	Fix_pattern	RO	0x0	Reserved
8	Err	RO	0x0	Err flag after PRBS has synchronized
7:2	Reserved	RO	0x0	Reserved
1	bisync_latch_low	RO LL	0x0	PRBS test synchronization status, once the sync is lost, this bit will latch low, until it's been read out.
0	Bitsync	RO	0x0	real time PRBS test synchronization status

4.4.5. sds prbs mon2 (0x09)

Table 69. sds prbs mon2 (0x09)

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_15_0	RO	0x0	real time lowest 16 bits received error bit counter

4.4.6. sds prbs mon3 (0x0A)

Table 70. sds prbs mon3 (0x0A)

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_31_16	RO	0x0	real time highest 16 bits received error bit counter

4.4.7. analog cfg2 (0xA1)

Table 71. analog cfg2 (0xA1)

Bit	Symbol	Access	Default	Description
15:12	Tx_driver_stg2	RW	0xA	TX driver stage2 amplitude control bit<3:2>: 00 +0mA 01: +2.5mA 10:+2.5mA 11+5mA bit<1:0>: 00 +0mA 01: +0.625mA 10: +1.25mA 11:+2.5mA
11	Tx_driver_stg1	RW	0x1	TX driver stage1 amplitude control
10:8	Reserved	RO	0x0	Reserved
7:6	vb_tx_term	RW	0x2	tx output common mode voltage when tx power down 00: 0.7V 01:0.8V 10:0.9V 11:1V
5	tx_vamp_post	RW	0x0	TX driver post stage1 amplitude control.
4	Reserved	RO	0x0	always 0.
3:1	tx_driver_post	RW	0x7	TX driver stage2 de-emphasize control bit<2>: 0 +0mA 1: +2.5mA bit<1:0>: 00 +0mA 01: +0.625mA 10: +1.25mA 11:+2.5mA
0	Tx_pd	RW	0x0	power down analog tx

5. DC Characteristics

5.1. Absolute Maximum Ratings

Table 72. Absolute Maximum Ratings

Description	Symbol	Mini	Max	Unit
3.3 V power supply	DVDDH, AVDDH, SVDDH	-0.3	3.63	V
1.2 V power supply	DVDDL, AVDDL,SVDDL	-0.2	1.32	V
Junction Temperature		-	125	℃
Storage Temperature		-45	125	℃

Note：These absolute maximum ratings indicate levels where permanent damage to the device can occur. The function of chip is not guaranteed under thess conditions. The chip at these conditions may effect long-term reliability of the device.

5.2. Recommended Operating Conditions

Table 73. Recommended Operating Conditions

Description	Pins	Min	Typ	Max	Unit
3.3 V power supply	DVDDH, AVDDH, SVDDH	3.135	3.30	3.465	V
1.2 V power supply	DVDDL, AVDDL, SVDDL	1.14	1.20	1.26	V
Ambient Operation Temperature Ta Commercial		0	-	70	℃
Ambient Operation Temperature Ta Industry		-40	-	85	℃

5.3. DC Characteristics

Table 74. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
DVDDH, AVDDH, SVDDH	3.3V Supply Voltage	3.135	3.30	3.465	V
DVDDL, AVDDL, SVDDL	1.2V Supply Voltage	1.14	1.20	1.26	V
Voh	High Level Output Voltage	2.4	-	-	V
Vol	Low Level Output Voltage	-	-	0.4	V
Vih	High Level Input Voltage	DVDDH-0.7	-	-	V
Vil	Low Level Input Voltage	-	-	GND+0.7	V

5.4. Power Consumption

Table 75. QSGMII to 1000BASE-X x 4 Power Consumption

Condition	3.3V(mA)	1.2V(mA)	Power Consumption(mW)
Hardware Reset	8.3	10.7	40.2
Link Up @1000Mbps	43.2	196.1	377.9
Traffic @1000Mbps	43.2	196.2	378

Note: Test by TT IC with 3.3V and 1.2V at room temperature.

Table 76. QSGMII to 1000BASE-X x 4 Maximum Power Consumption

Condition	3.3V(mA)	1.2V(mA)	Power Consumption(mW)
Hardware Reset	12.5	16.1	60.6
Link Up @1000Mbps	64.8	294.2	566.9
Traffic @1000Mbps	64.9	295	568.2

Note: Test by FF corner IC 3.3V and 1.2V at high temperature 85℃.

6. AC and Timing Characteristics

6.1. Power and Reset Sequence

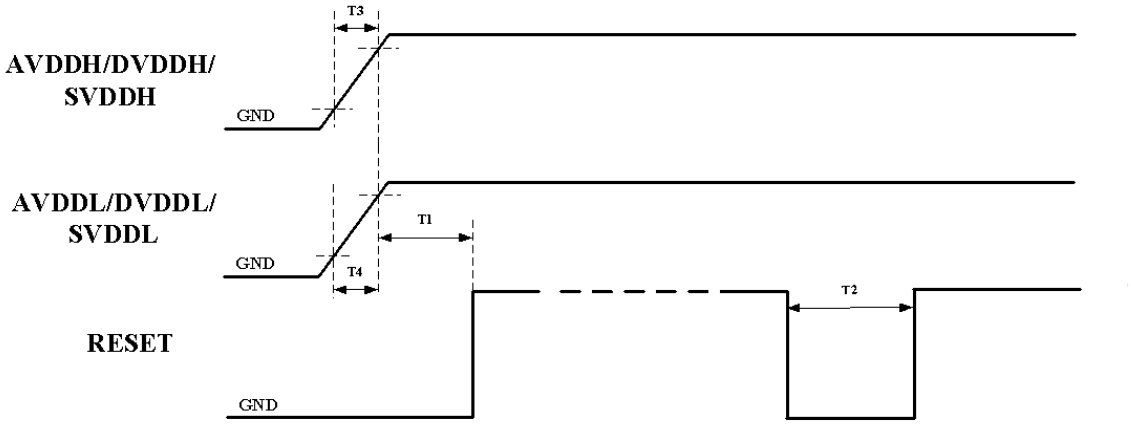


Figure 4. Power and Reset Sequence

Table 77. Power and Reset Sequence

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high.	10	-	-	ms
T2	The duration of reset signal remain low timing.	10	-	-	ms
T3	AVDDH/DVDDH/SVDDH power rising time.	0.5	-	-	ms
T4	AVDDL/DVDDL/SVDDL power rising time.	0.5	-	-	ms

6.2. Crystal Requirement

Table 78. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Parallel Resonant Crystal Reference Frequency	-	25	-	MHz
Fref Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-50	-	50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.5	-	-	V
Vil	Crystal output low level	-	-	0.4	V

6.3. Oscillator/External Clock Requirement

Table 79. Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency	-	25	-	MHz
Frequency tolerance	-50	-	50	PPM
Duty Cycle	40	-	60	%
Vih	1.5	-	-	V
Vil	-	-	0.4	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns
RMS Jitter (12kHz~20MHz)	-	-	1	ps

6.4. QSGMII Differential Transmitter Characteristics

Table 80. QSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	-	200	-	ps
T_X1	Eye Mask	-	-	0.15	UI
T_X2	Eye Mask	-	-	0.4	UI
T_Y1	Eye Mask	200	-	-	mV
T_Y2	Eye Mask	-	-	450	mV
$T_{TX-JITTER}$	Output Jitter	-	-	0.30	UI
$T_{Tx-RISE}$	Output Rise Time	30	-	-	ps
$T_{TX-FALL}$	Output Fall Time	30	-	-	ps
R_{TX}	Differential Resistance	80	100	120	ohm
C_{TX}	AC Coupling Capacitor	75	100	200	nF
L_{TX}	Transmit Length in PCB(FR4)	-	-	10	inch

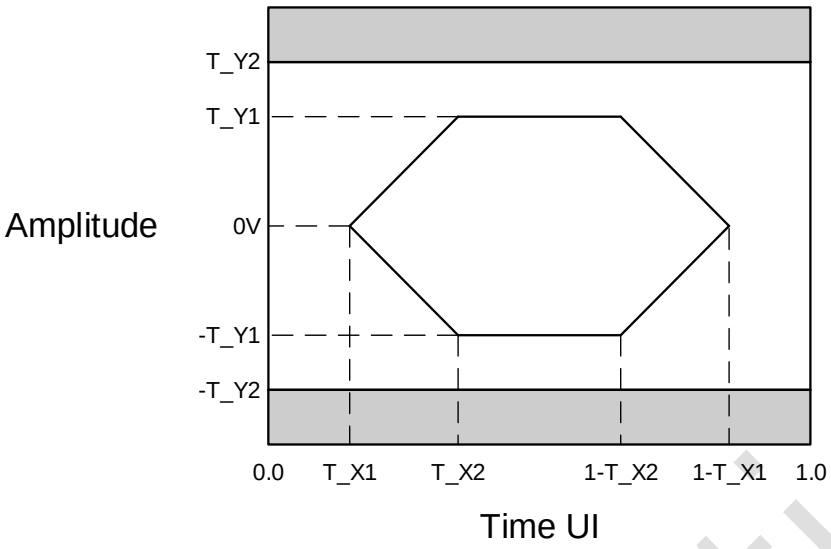


Figure 5. QSGMII Differential Transmitter Eye Diagram

6.5. QSGMII Differential Receiver Characteristics

Table 81. QSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	-	200	-	ps
R_X1	Eye Mask	-	-	0.3	UI
R_Y1	Eye Mask	50	-	-	mV
R_Y2	Eye Mask	-	-	600	mV
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.60	UI
R_{RX}	Differential Resistance	80	100	120	ohm

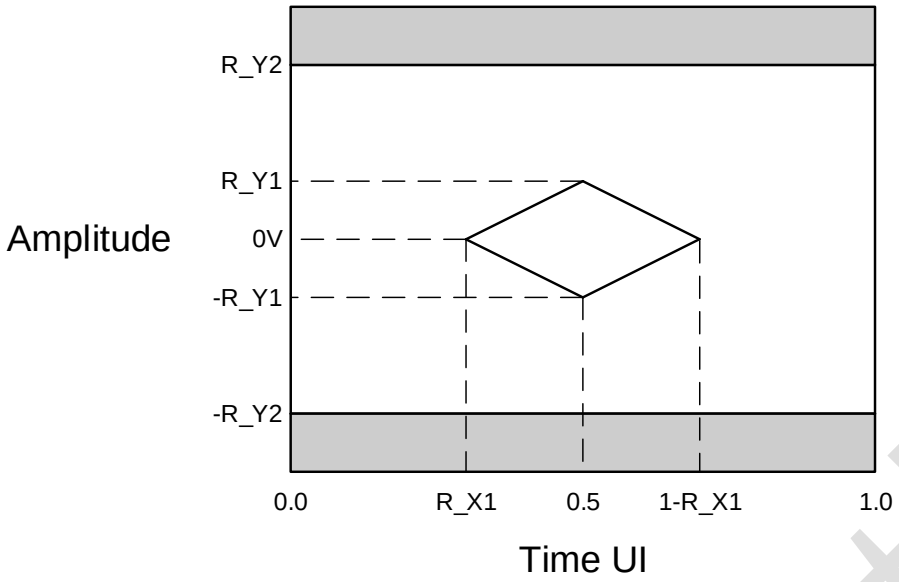


Figure 6. QSGMII Differential Receiver Eye Diagram

6.6. 1.25G SERDES Differential Transmitter Characteristics

Table 82. 1.25G SERDES Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ±75ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	450	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	TTX-JITTER-MAX = 1 - TTX-EYE-MIN = 0.375UI
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling Capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB(FR4)	-	-	10	inch	-

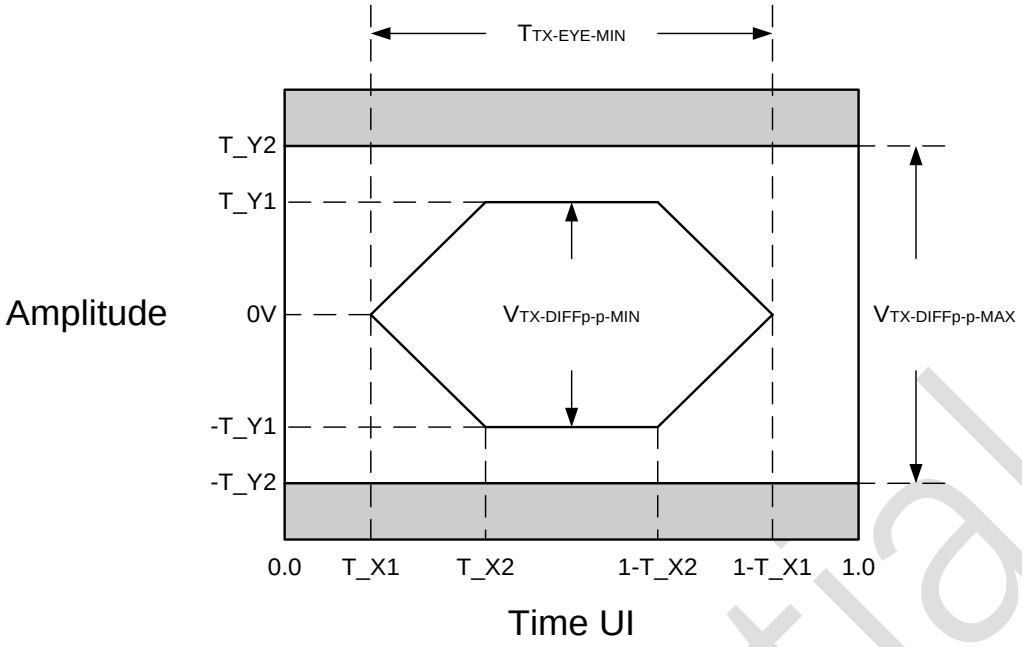


Figure 7. 1.25G Serdes Differential Transmitter Eye Diagram

6.7. 1.25G SERDES Differential Receiver Characteristics

Table 83. 1.25G SERDES Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ±75ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	100	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	TRX-JITTER-MAX = 1 - TRX-EYE-MIN = 0.625UI
R_{RX}	Differential Resistance	80	100	120	ohm	-

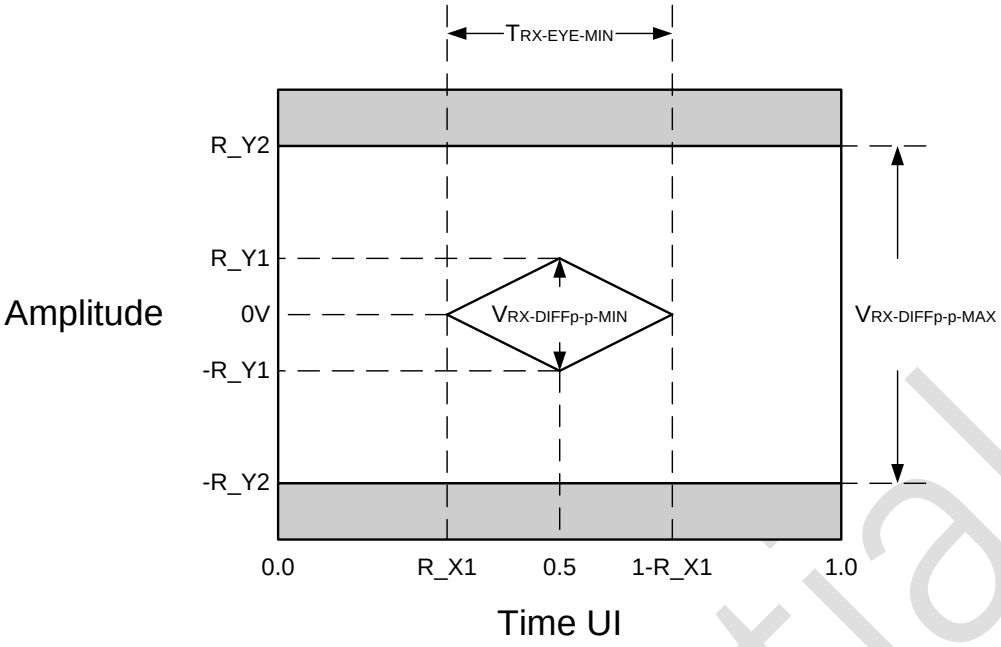


Figure 8. 1.25G Serdes Differential Receiver Eye Diagram

6.8. SMI (MDC/MDIO) Interface Characteristics

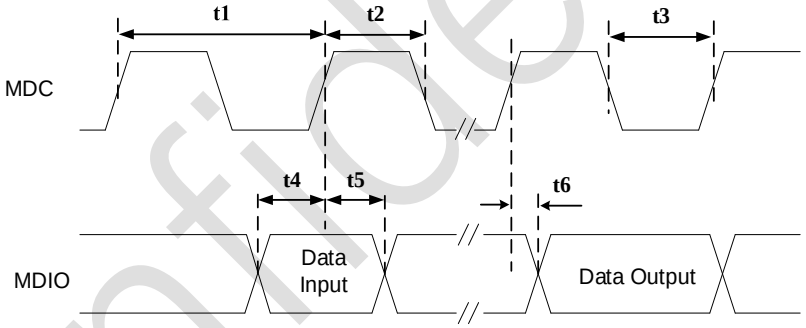


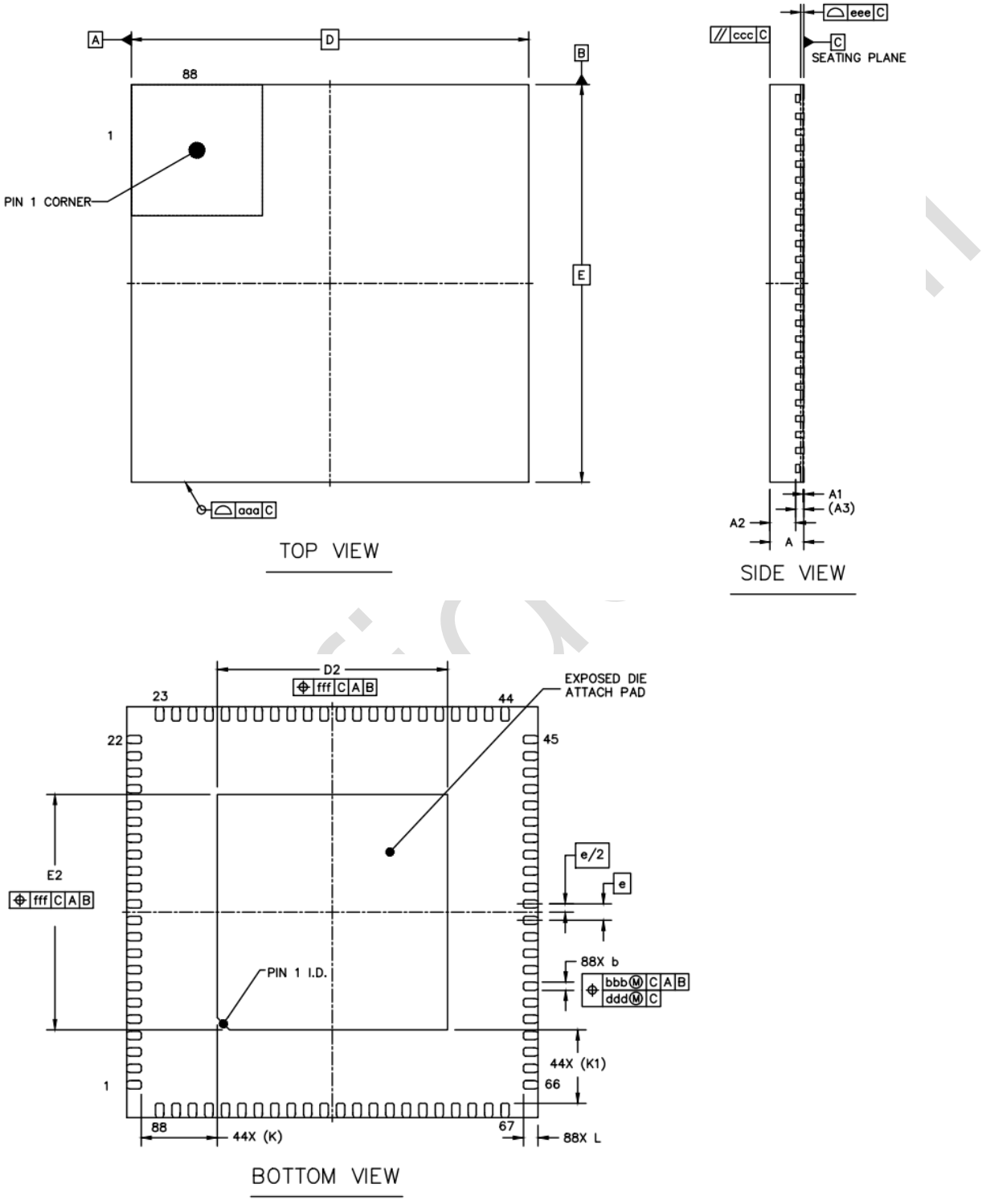
Figure 9. SMI (MDC/MDIO) Timing

Table 84. SMI (MDC/MDIO) Interface Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	80	-	-	ns
t2	MDC High Time	32	-	-	ns
t3	MDC Low Time	32	-	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC rising edge (Data Output)	0	-	20	ns

7. Mechanical and Thermal

7.1. Mechanical Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	5.5	5.6	5.7
	Y	E2	5.63	5.73	5.83
LEAD LENGTH		L	0.25	0.35	0.45

7.2. Thermal Information

Table 85. Thermal Resistance

Symbol	Parameter	Condition	Typ	Units
θJA	Thermal resistance - junction to ambient θJA = (TJ - TA)/ P P = power dissipation that produced change in junction temperature.	JEDEC 3.0 in. x 4.5 in dimensions and 4-layer PCB with no air flow TA=25 ℃	29.1	℃/W
θJC	Thermal resistance - junction to case θJC = (TJ - TC)/ P P = power dissipation that produced change in junction temperature. TC = the top case temperature of package	JEDEC 3.0 in. x 4.5 in dimensions and 4-layer PCB with no air flow TA=25 ℃	22.5	℃/W
θJB	Thermal resistance - junction to board θJB = (TJ - TB)/ P P = power dissipation that produced change in junction temperature. TB = board temperature at steady state	JEDEC 3.0 in. x 4.5 in dimensions and 4-layer PCB with no air flow TA=25 ℃	13	℃/W

8. Ordering Information

Motorcomm offers an RoHS package that is compliant with RoHS.

Part Number	Grade	Package	Pack	Status	Operation Temp
YT8614QC	Consumer	QFN-88 E-PAD	Tape Reel 1500ea	Mass Production	0 ~70 ℃
YT8614QH	Industrial	QFN-88 E-PAD	Tape Reel 1500ea	Mass Production	-40 ~ 85 ℃