16-Bit ADC with On-board Reference

PRODUCT DESCRIPTION

The MS1100 is a 16bit high-precision ADC. The on-board reference provides a differential input range of ±2.048V. The MS1100 uses an I^2C serial interface. The power supply ranges from 2.7V to 5.5V.

The MS1100 can perform conversions at rates of 15, 30, 60 or 240 samples per second (SPS). The MS1100 integrates programmable gain amplifier and gain is up to 8. In single-conversion mode, the MS1100 automatically enter into power-down state after a conversion, greatly reducing power dissipation.

The MS1100 is designed for applications requiring high resolution measurement and where space and power dissipation are major considerations, such as portable instrument, industry control and smart transmitter.

SOT23-6

FEATURES

- I^2C Serial Interface
- On-board Reference: 2.048V ±0.5%
- Temperature Drift: 10ppm/°C
- On-board PGA and OSC
- 16Bit No Missing Codes
- INL (Integral Non-linearity): 0.01%
- I^2C Address Number: 8
- Programmable Data Rate: 15SPS to 240SPS
- Operating Voltage: 2.7V to 5.5V
- Low Current Consumption: 315µA

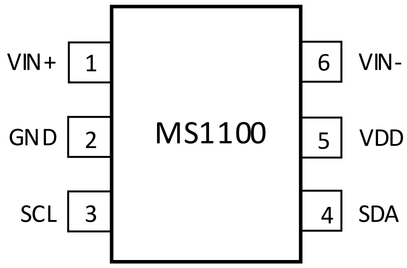
APPLICATIONS

- Portable Instrument
- Industry Process Control
- Smart Transmitter
- Factory Automation
- Temperature Measurement

PRODUCT SPECIFICATION

Part Number	I^2C Address	Range	Package	Marking
MS1100	1001 000	00	SOT23-6	1100
MS1100	1001 001	01	SOT23-6	1100
MS1100	1001 010	02	SOT23-6	1100
MS1100	1001 011	03	SOT23-6	1100
MS1100	1001 100	04	SOT23-6	1100
MS1100	1001 101	05	SOT23-6	1100
MS1100	1001 110	06	SOT23-6	1100
MS1100	1001 111	07	SOT23-6	1100

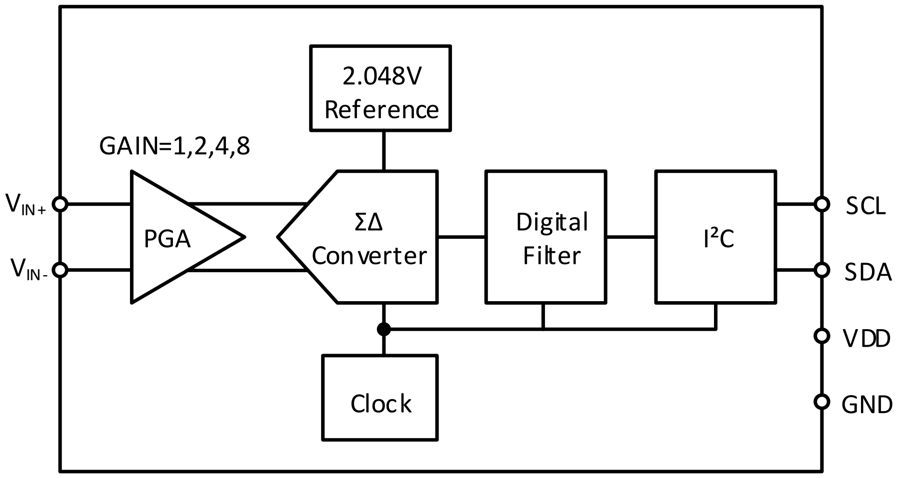
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbol	Type	Description
1	VIN+	I	Differential Positive Input
2	GND	-	Ground
3	SCL	I	Serial Clock Input
4	SDA	I/O	Serial Data: Transmits and Receives Data
5	VDD	-	Power Supply
6	VIN-	I	Differential Negative Input

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Symbol	Parameter	Ratings	Unit
Power Supply	VDD	-0.3 ~ 6	V
Input Current	IIN	100mA, Momentary	mA
Input Current	IIN	10mA, Continuous	mA
Analog Input (A0, A1 to GND)	VIN	-0.3 ~ VDD+0.3	V
SDA, SCL Voltage to GND	V	-0.5 ~ 6	V
Maximum Junction Temperature	T	150	°C
Storage Temperature	Tstg	-60 ~ 150	°C
Lead Temperature	T	260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature	TA	VDD=2.7V to 3.6V	-40		125	°C
		VDD=3.6V to 5.5V	-30		125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VDD=5.0V.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Full-Scale Input Voltage	(VIN+)-(VIN-)		±2.048/PGA		V
Analog Input Voltage	VIN+ to GND, VIN- to GND	GND-0.2		VDD+0.2	V
Differential Input Impedance			2.8/PGA		MΩ
Common-Mode Input Impedance	PGA=1		3.5		MΩ
	PGA=2		3.5		MΩ
	PGA=4		1.8		MΩ
	PGA=8		0.9		MΩ
System Performance					
Resolution and No Missing Codes	DR=00	12		12	Bits
	DR=01	14		14	Bits
	DR=10	15		15	Bits
	DR=11	16		16	Bits
Output Rate	DR=00	180	240	308	SPS
	DR=01	45	60	77	SPS
	DR=10	22	30	39	SPS
	DR=11	11	15	20	SPS
Integral Non-linearity	DR=11, PGA=1, End Point [1]		±0.004	±0.010	% of FSR[2]
Offset Error	PGA=1		8	15	mV
	PGA=2		8	15	mV
	PGA=4		8	15	mV
	PGA=8		8	15	mV
Offset Drift	PGA=1		1.2		μV/°C
	PGA=2		0.6		μV/°C
	PGA=4		0.3		μV/°C
	PGA=8		0.3		μV/°C
Offset VS. VDD	PGA=1		800		μV/V
	PGA=2		400		μV/V
	PGA=4		200		μV/V
	PGA=8		150		μV/V

Parameter	Condition	Min	Typ	Max	Unit
System Performance					
Gain Error			0.05	0.4	%
PGA Gain Match Error [3]	Any two gain match		0.02	0.1	%
Gain Error Drift			10		ppm/°C
Gain VS. VDD			80		ppm/V
Common-Mode Rejection Ratio	DC input and PGA=8	95	105		dB
	DC input and PGA=1		100		dB
Digital Input/Output					
Input High Voltage		0.7×VDD		6	V
Input Low Voltage		GND-0.5		0.3×VDD	V
Output Low Voltage	IOL=3mA	GND		0.4	V
Input High Peak Current				10	μA
Input Low Peak Current		-10			μA
Power Supply Requirements					
Operating Voltage	VDD	2.7		5.5	V
Supply Current	Power-down		0.05	2	μA
	Operation		315	350	μA
Power Dissipation	VDD=5.0V		1.6	1.9	mW
	VDD=3.0V		0.96		mW

Note：

1. 99% of full-scale.
2. FSR = full-scale range = 2 × 2.048V/PGA = 4.096V/PGA.
3. Includes all errors from PGA and reference.

FUNCTION DESCRIPTION

The MS1100 is a 16-bit, fully differential, delta-sigma analog-to-digital converter. The MS1100 consists of a delta-sigma A/D converter with adjustable gain, a 2.048V voltage reference, a clock oscillator, a digital filter and an I^2C interface. It has easy design and configuration, so users can easily achieve accurate measurement

Analog-to-Digital Converter

The MS1100 A/D converter core consists of a differential switched-capacitor delta-sigma modulator and a digital filter. The modulator measures the voltage difference between the positive and negative analog inputs and compares it to reference voltage, which is 2.048V in the MS1100. The digital filter receives a high-speed bit stream from the modulator and outputs digital signal, which is proportional to the input voltage.

Voltage Reference

The MS1100 has a 2.048V on-board voltage reference without need for external reference.

Output Code Calculation

The number of bits for the MS1100 depends on update rate, as shown in Table 1.

Table 1. Minimum and Maximum Codes

Update Rate	Number Of Bits	Minimum Code	Maximum Code
15SPS	16	-32768	32767
30SPS	15	-16384	16383
60SPS	14	-8192	8191
240SPS	12	-2048	2047

The output code of the MS1100 is in binary two's complement format, right-justified and sign-extended. Table 2 shows the output codes for various input levels.

Table 2. Output Codes for Different Input Signals

Data Rate	Differential Input Signal				
	-2.048V	-1LSB	0 (Ideal)	+1LSB	+2.048V
15SPS	8000_H	$FFFF_H$	0000_H	0001_H	$7FFF_H$
30SPS	$C000_H$	$FFFF_H$	0000_H	0001_H	$3FFF_H$
60SPS	$E000_H$	$FFFF_H$	0000_H	0001_H	$1FFF_H$
240SPS	$F800_H$	$FFFF_H$	0000_H	0001_H	$07FF_H$

Note 1: Differential input; do not drive the MS1100 absolute inputs below −200mV.

The output code is given by the expression:

$$\text{Output Code} = -1\times\text{Minimum Code}\times\text{PGA}\times\frac{(V_{IN+})-(V_{IN-})}{2.048V}\ \ldots\ldots\ldots\ldots(V_{IN+}<V_{IN-})$$

$$\text{Output Code} = 1\times\text{Maximum Code}\times\text{PGA}\times\frac{(V_{IN+})-(V_{IN-})}{2.048V}\ \ldots\ldots\ldots\ldots(V_{IN+}\geq V_{IN-})$$

The maximum code is $2^{n-1}-1$, while the minimum code is $-1\times2^{n-1}$.

Clock Oscillator

The MS1100 features an on-board clock oscillator, which drives modulator and digital filter without need for external clock.

Input Impedance

The input stage of the MS1100 uses switched-capacitor. The equivalent resistance value depends on the capacitor value and switching frequency. The capacitor value depends on the PGA setting. The clock is generated by the on-board clock oscillator. The typical operating frequency is 275kHz.

The common-mode and differential input impedance are different. Details see in Electrical Characteristics.

For input source with high output impedance, buffer may be necessary externally on input terminal.

Aliasing

If the input signal frequency of the MS1100 exceeds half of the update rate, aliasing will occur. To prevent aliasing, the input signal must be band-limited. The digital filter of the MS1100 provides some attenuation of high-frequency noise to some extent, but sinc filter cannot completely replace an anti-aliasing filter. For a few applications, external filtering also is needed.

When designing input filter circuit, remember to take into account the impedance match between the filter and the MS1100 input.

Operation Mode

The MS1100 has two conversion modes: continuous conversion and single conversion.

In continuous conversion mode, after a conversion has been completed, the MS1100 places the result in the result register and immediately begins another conversion.

In single conversion mode, the MS1100 will wait until the $\overline{\text{ST/DRDY}}$ bit in the configuration register is set to 1. Then the MS1100 start a conversion. After the conversion is completed, the MS1100 places the result in the result register, resets the $\overline{\text{ST/DRDY}}$ bit to 0 and powers down.

When switched from continuous conversion mode to single conversion mode, the MS1100 completes the current conversion, resets the $\overline{\text{ST/DRDY}}$ bit to 0 and powers down.

Reset and Power-up

When the MS1100 powers up, it automatically performs a reset. The MS1100 sets all of the bits in the configuration register to their default settings.

The MS1100 responds to the I^2C General Call Reset command. When the MS1100 receives a General Call Reset, it performs a reset.

I^2C Interface

The MS1100 communicates through an I^2C interface.

A timing diagram is shown in Figure 1. The related parameters for this diagram are given in Table 3.

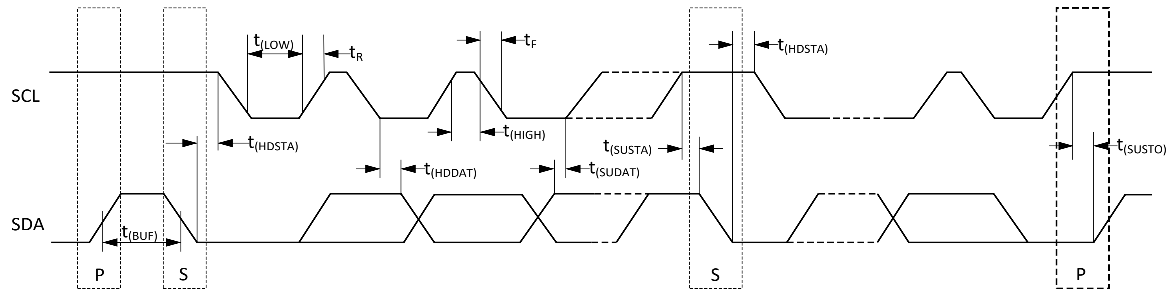


Figure 1. I^2C Timing Diagram

Table 3. Timing Diagram Definitions

Parameter		Fast-Speed Mode		Unit
		Min	Max	
$t_{(SCLK)}$	SCLK Operating Frequency		0.4	MHz
$t_{(BUF)}$	Bus START to STOP Idle Time	600		ns
$t_{(HDSTA)}$	START Hold Time	600		ns
$t_{(SUSTA)}$	Repeated START Setup Time	600		ns
$t_{(SUSTO)}$	STOP Setup Time	600		ns
$t_{(HDDAT)}$	Data Hold Time	0		ns
$t_{(SUDAT)}$	Data Setup Time	100		ns
$t_{(LOW)}$	SCLK Clock Low Level Period	1300		ns
$t_{(HIGH)}$	SCLK Clock High Level Period	600		ns
t_F	Clock/Data Fall Time		300	ns
t_R	Clock/Data Rise Time		300	ns

Result Register

The 16-bit result register contains the conversion result in binary two's complement format. After reset or power-up, the result register is cleared 0, and remains until the first conversion is completed. The format of result register is shown in Table 4.

Table 4. Result Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Configuration Register

The 8-bit configuration register can be used to control the operation mode, update rate and PGA. The format of configuration register is shown in Table 5. The default setting is 8CH.

Table 5. Configuration Register

Bit	7	6	5	4	3	2	1	0
Name	$\overline{\text{ST/DRDY}}$	0	0	SC	DR1	DR0	PGA1	PGA0
Default	1	0	0	0	1	1	0	0

Bit 7 : $\overline{\text{ST/DRDY}}$

The meaning of the $\overline{\text{ST/DRDY}}$ bit depends on whether it is being written to or read from.

In single conversion mode, writing 1 to the $\overline{\text{ST/DRDY}}$ bit indicates a conversion to start, and writing 0 has no effect. In continuous mode, the MS1100 ignores the value written to $\overline{\text{ST/DRDY}}$.

In continuous conversion mode, use $\overline{\text{ST/DRDY}}$ bit to determine whether new conversion data is ready. If $\overline{\text{ST/DRDY}}$ is 1, the data in the result register has already been read. If it is 0, the data in the result register is new, and has not yet been read.

In single conversion mode, use $\overline{\text{ST/DRDY}}$ bit to determine whether a conversion has completed. If $\overline{\text{ST/DRDY}}$ is 1, the data in the result register is old, and the conversion is still in process. if it is 0, the data in the result register is the new conversion result.

The MS1100 first outputs the value of result register, then the value of configuration register. The state of the $\overline{\text{ST/DRDY}}$ bit applies to the data just read from the result register, rather than the data from the next read operation.

Bit 6-5 : Reserved

Bit 6-5 must be set to 0.

Bit 4 : SC

Conversion mode select bit. When SC is 1, the MS1100 is in single conversion mode; when SC is 0, it is in continuous conversion mode. The default setting is 0.

Bits 3-2 : DR

Update rate select bits, as shown in Table 6.

Table 6. DR Bits

DR1	DR0	Data Rate	Resolution
0	0	240SPS	12 Bit
0	1	60SPS	14 Bit
1	0	30SPS	15 Bit
1[1]	1[1]	15SPS	16 Bit

Note 1: Default setting

Bit 1-0 : PGA

Gain setting select bits, as shown in Table 7.

Table 7. PGA Bits

PGA1	PGA0	Gain
0[1]	0[1]	1
0	1	2
1	0	4
1	1	8

Note 1: Default setting

Reading from the MS1100

Read the value in the result register and the configuration register. First address the MS1100, then read three bytes from the device. The first two bytes are the result register's contents, and the third byte is the configuration register's contents.

It is not required to read the configuration register. It is permissible to read fewer than three bytes during a read operation. Reading more than three bytes from the MS1100 has no effect. All bytes from the fourth byte will be FFH.

The timing diagram of typical read operation for the MS1100 is shown in Figure 2.

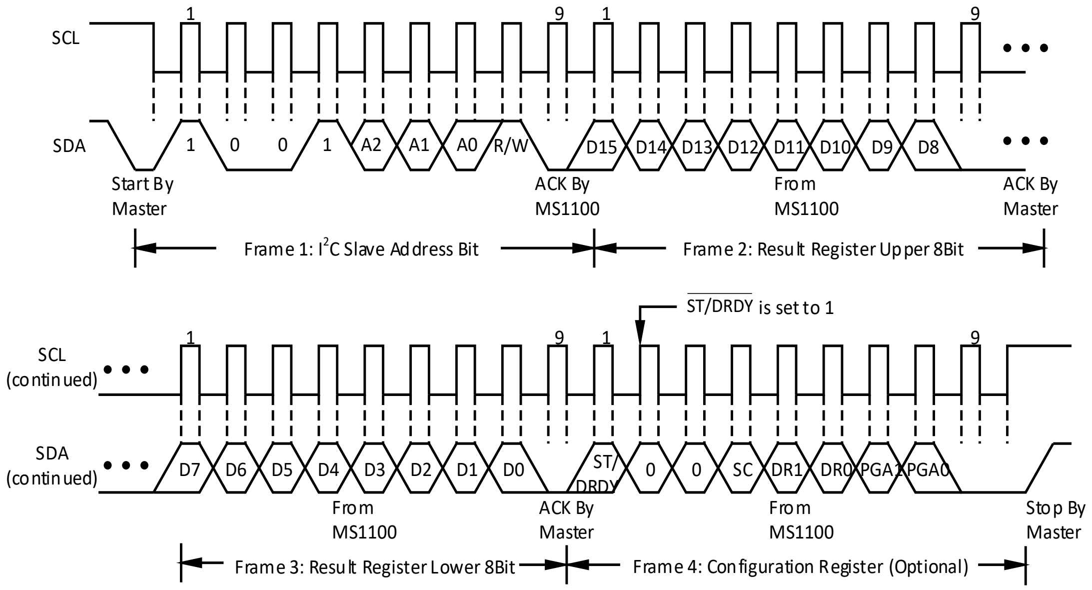


Figure 2. Timing Diagram for Reading from the MS1100

Writing to the MS1100

Write to the configuration register. First address the MS1100, then write into one byte. The byte will be written to the configuration register.

Writing more than one byte to the MS1100 has no effect. The MS1100 will ignore any byte after the first byte. The timing diagram of typical write operation for the MS1100 is shown in Figure 3.

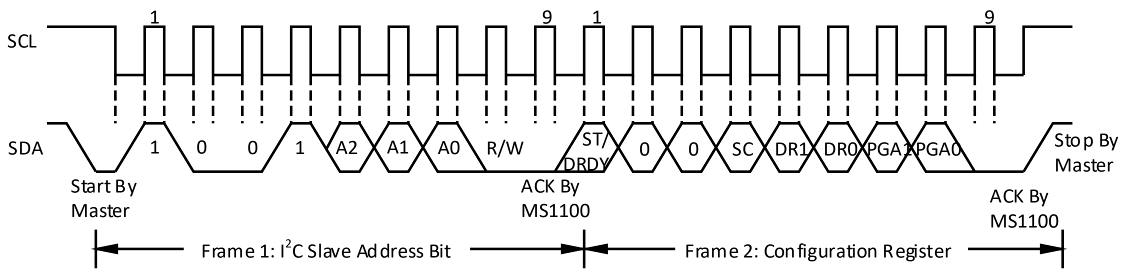


Figure 3. Timing Diagram for Writing to the MS1100

APPLICATIONS INFORMATION

Basic Connection

For many applications, the basic connection diagram of the MS1100 is shown in Figure 4.

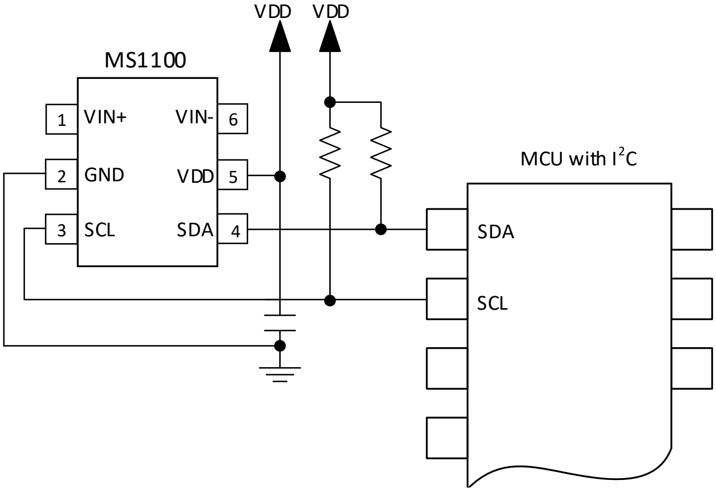


Figure 4. Typical Connections of the MS1100

Connecting Multiple Devices

Multiple MS1100s can be connected to a I^{2}C bus. The MS1100 is available in different eight versions, each of which has a different I^{2}C address. An example showing three MS1100s connected on a same bus is shown in Figure 5. Up to eight MS1100s (use differential eight versions of the MS1100) can be connected to a I^{2}C bus.

Note that I^{2}C bus only needs one set of pull-up resistors.

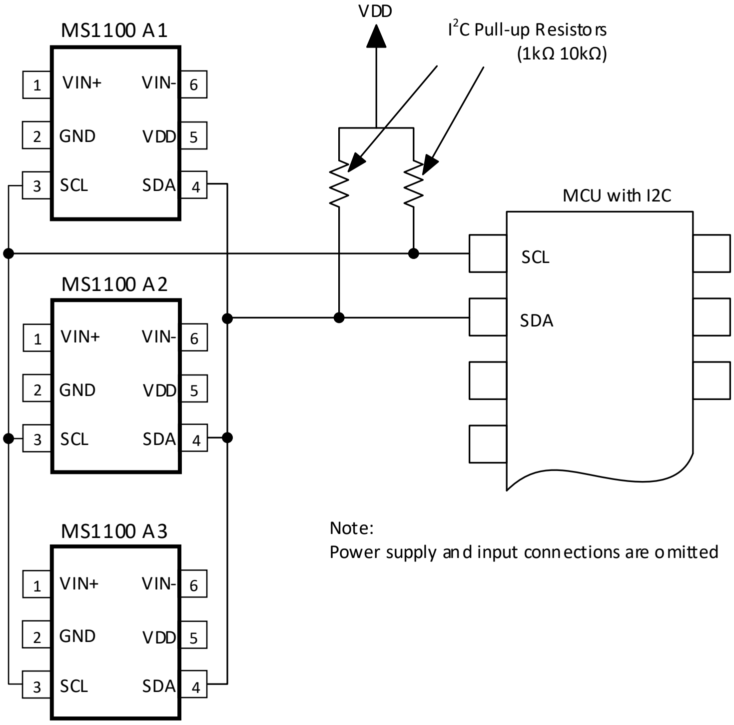


Figure 5. Connecting Multiple MS1100s

Low-Side Current Monitor

Figure 6 shows a circuit for a low-side current monitor. The circuit reads the voltage across a shunt resistor, the voltage of which is amplified by the MS8552, and the result is read by the MS1100.

It is suggested that the MS1100 be operated at a gain of 8. The gain of the MS8552 can be reduced. For a gain of 8, the op amp should provide output voltage of no greater than 0.256V. Therefore, the shunt resistor is sized to provide a maximum voltage drop of 64mV at full-scale current.

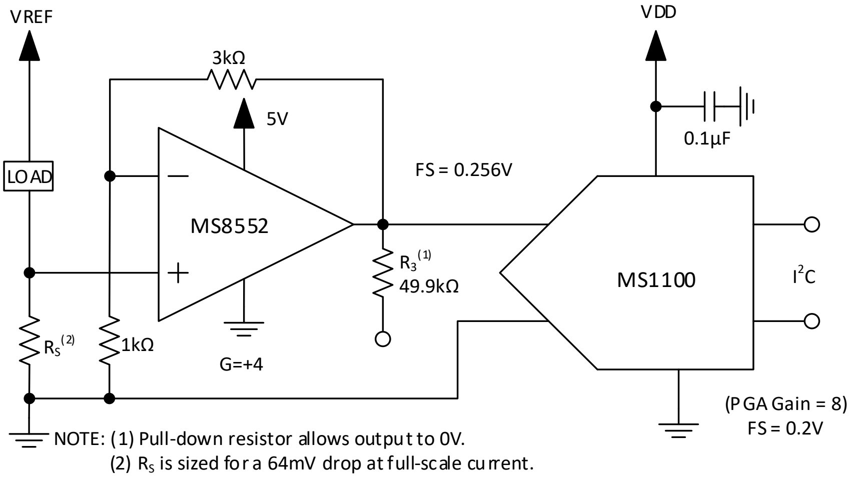
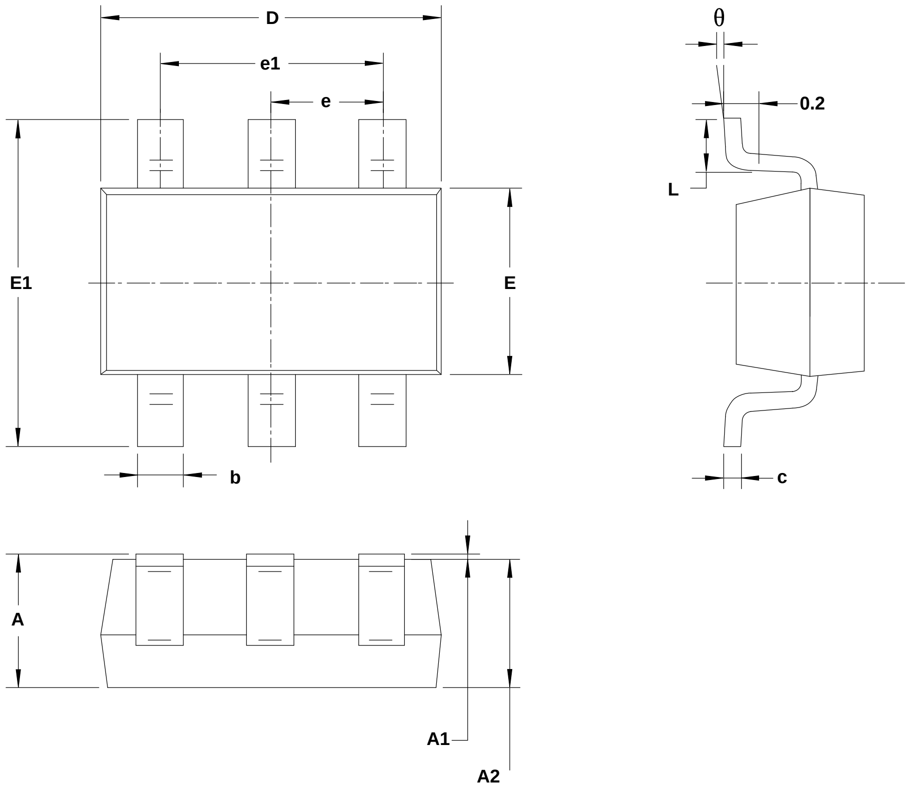


Figure 6. Low-Side Current Measurement

PACKAGE OUTLINE DIMENSIONS

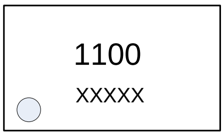
SOT23-6



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.20	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950BSC		0.037BSC	
e1	1.900BSC		0.075BSC	
L	0.300	0.600	0.012	0.024
θ	0º	8º	0º	8º

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name : 1100

Product Code : XXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS1100	SOT23-6	3000	10	30000	4	120000

STATEMENT

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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