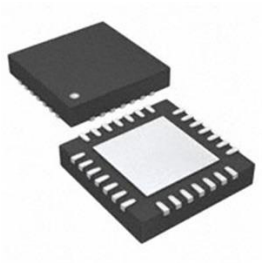
Three Phase Brushless Motor Pre-Driver

PRODUCT DESCRIPTION

The MS4931 is a three-phase brushless motor pre-driver chip, up to 35V operating voltage,can drive a wide range of N-channel power MOSFETs.

The chip has functions of stall guard, over temperature protection,and synchronous rectification. Internal synchronization allows the chip to reduce power consumption by turning on the appropriate power MOSFETS during current decay. The chip has enable,direction, and brake inputs to control current,FG1 and FG2 outputs to control motor rotation.



QFN28

FEATURES

- Drive 6 N-type Power MOSFETs
- Synchronous Rectifier,Shutdown Mode, Low Power
- Low Voltage Protection,Over Temperature Protection
- Hall Elements Input or Hall Ic Input
- PWM Control Current, Positive and Reverse Rotation Model
- FG1 and FG2 Output
- 5V LDO Out
- Stall Guard Protection
- QFN28 Package

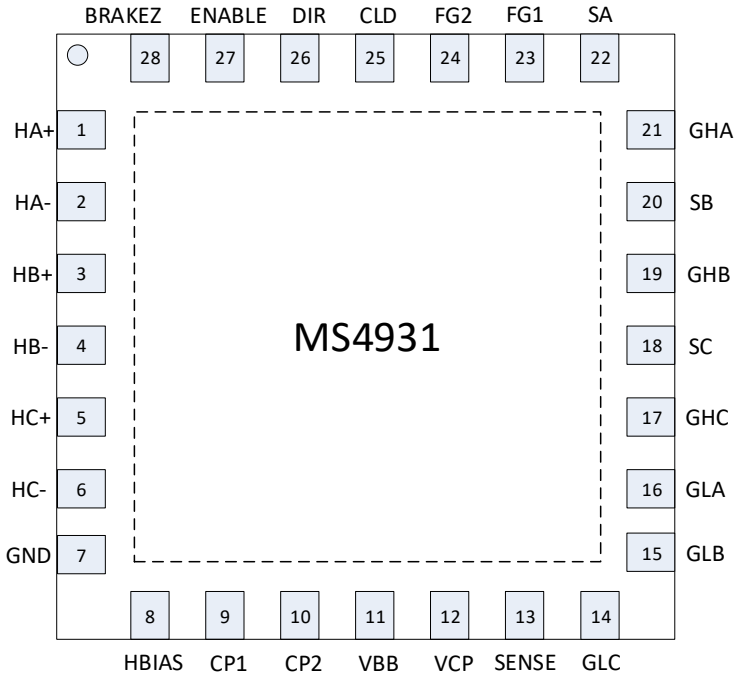
APPLICATIONS

- Laser Printer,Copier
- Power Rotate Tools
- Water Pump, Gas Pump
- Monitoring Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS4931	QFN28	MS4931

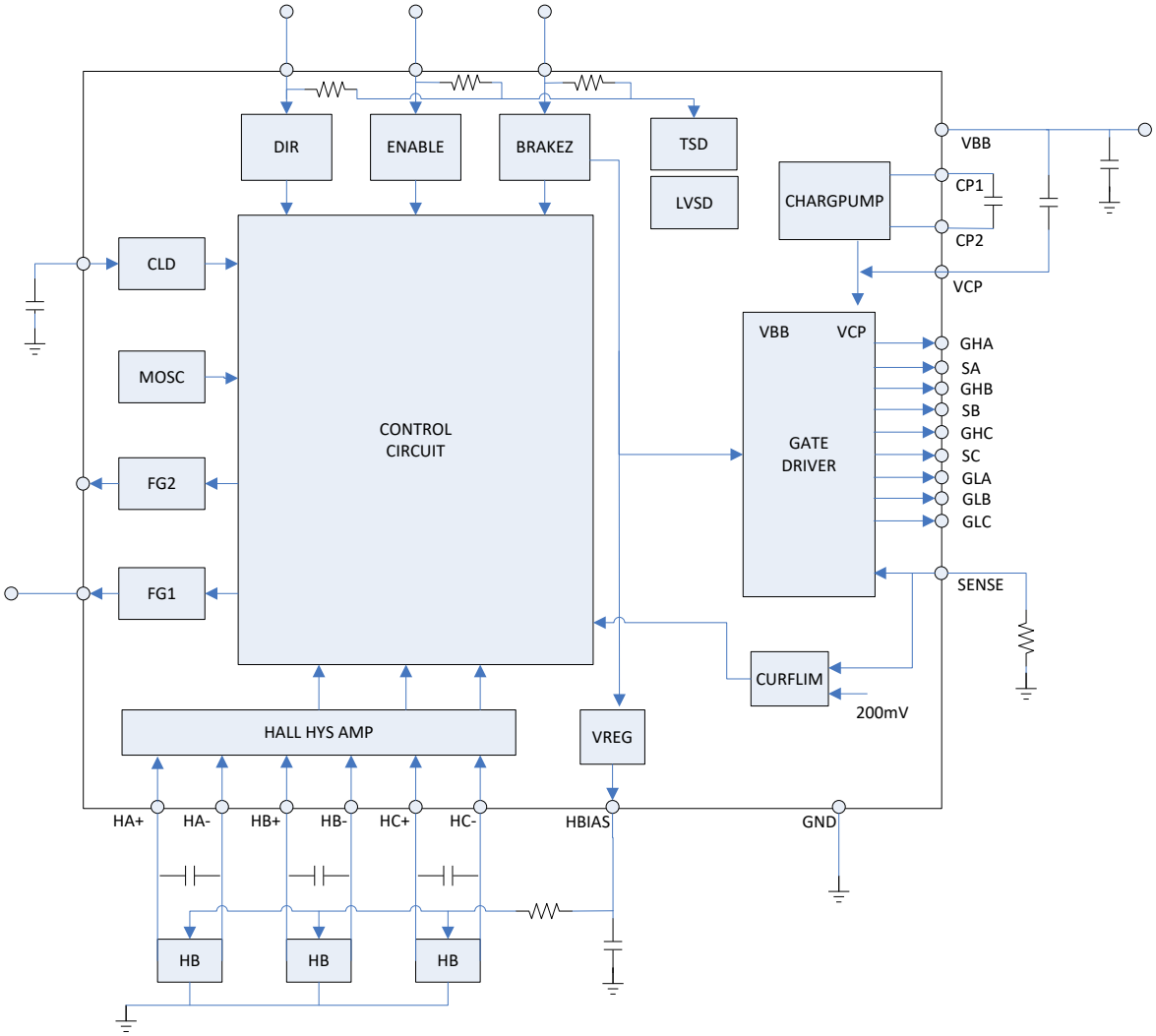
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	HA+	I	HALL Input H：IN+>IN-；L：IN->IN+
2	HA-		
3	HB+		
4	HB-		
5	HC+		
6	HC-		
7	GND	-	Ground
8	HBIAS	O	5V LDO Out
9	CP1	O	Charge-pump Capacitor
10	CP2		
11	VBB	P	Power
12	VCP	I/O	Charge-pump Output
13	SENSE	O	Current Sense Pin
14	GLC	O	H-bridge Low Side Output C
15	GLB		H-bridge Low Side Output B
16	GLA		H-bridge Low Side Output A
17	GHC		H-bridge High Side Output C
18	SC		Output C
19	GHB		H-bridge High Side Output B
20	SB		Output B
21	GHA		H-bridge High Side Output A
22	SA		Output A
23	FG1	O	Hall Output (3ϕ)
24	FG2	O	Hall Output (1ϕ)
25	CLD	I/O	Stall Guard Capacitor
26	DIR	I	Rotate Direction
27	ENABLE	I	PWM Speed Control
28	BRAKEZ	I	Motor Brake 0: Brake 1 or Open: Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Supply Voltage	VBBmax	35	V
Charge-pump Voltage	VGmax	42	V
Junction Temperature	Tjmax	150	°C
Operating Temperature Range	Topr	-40 ~ 105	°C
Store Temperature Range	Tstr	-55 ~ 150	°C
Suggest Supply Voltage	VBB	8 ~ 35	V
LDO Output Current	IREG	0 ~ -200	mA
FG Voltage	VFG	0 ~ 6	V
FG Current	IFG	0 ~ 14	mA

ELECTRICAL CHARACTERISTICS

VBB=24V, TA = 25°C.Unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Current 1	ICC1			3.8	4.7	mA
Supply Current 2	ICC2	Charge-pump On, Output Disable		0.89	1.1	mA
Output Driver						
High Side Gate Drive Voltage	VGS(H)	IGATE=2mA		5.2		V
Low Side Gate Drive Voltage	VGS(L)	IGATE=2mA		5.6		V
Gate Drive Current	IGATE	GH=GL=4	20	30		mA
Gate Drive Pull Down Resistor	RGATE			30		Ω
Dead Time	tdead	ID=-1A		1.2		μs
Current Limit Threshold Voltage	VREF	ID=1A , Rsense=0.2Ω		200		mV
5V HBIAS						
HBIAS Output Voltage	HBIAS	IO=-5mA	5.5	5.6	5.7	V
Line Regulation	ΔV(REG1)	VBB=8 to 35V,IO=-5mA			7	mV
Load Regulation	ΔV(REG2)	IO=-5mA to -10mA			0.4	mV
HALL Amplifier						
Hall Input Current	IB(HA)		-130			nA
Common Mode Input Range	VICM2	When use hall IC	0		HBIAS	V
Hall Input Range	VHIN	Sine waive input	80			mVp-p
Hall Input Hysteresis	ΔVIN(HA)			20		mV
Hall Input Threshold Up	VSLH			8		mV
Hall Input Threshold Down	VSHL			-12		mV
CLD Oscillator						
CLD High Level	VOH(CLD)			3.07		V
CLD Low Level	VOL(CLD)			1.08		V
Amplitude	V(CLD)			2.0		Vp-p
External Capacitor Charge Current	ICHG1(CLD)	VCHG1=2V		-11.3		μA
External Capacitor Discharge Current	ICHG2(CLD)	VCHG2=2V		11.3		μA
Oscillator Frequency	f(CLD)	C=0.022μF		129		Hz
Charge-pump						
VCP Voltage	VGOUT			VBB+5.2		V
Pump Frequency	f(CP)		42	50	70	kHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Internal PWM						
Oscillation Frequency	f(PWM)		41	51.5	62	kHz
Current Limit						
RF Pin Limit Voltage	VRF			0.2		V
Blank Time	tblank			1.2		μs
Over Temperature Protection						
Shutdown Temperature	TSD		146	154	158	°C
Hysteresis Width	ΔTSD		20	30	40	°C
Low Voltage Protection (5V HBIAS)						
Operation Voltage	VSD		4.0	4.17	4.4	V
Hysteresis Width	ΔVSD		0.29	0.30	0.31	V
FG /FG2						
Output on Resistor	VOL(FG)	IFG=5mA		17	20	Ω
Leakage Current	IL(FG)	Vo=5V			10	μA
Logic Input Pins(BRAKEZ, ENABLE,DIR)						
High Level Input Voltage	VIH		1.75		HBIAS	V
Low Level Input Voltage	VIL		0		1.65	V
Left Open Dc Voltage	VIO			3/5×HBIAS		V
Input Hysteresis Width	VIS		0.3	0.4	0.5	V
High Level Input Current	IIH	VBRAKEZ=HBIAS	41	51	65	μA
Low Level Input Current	IIL	VBRAKEZ=0V	-65	-76	-95	μA

Logic True Table

(IN="High" means $IN^+ > IN^-$), ("H"=SOURCE,"L"=SINK, "Z"=High-impedance)

HALL In						Pre-driver						Output		
DIR	HA	HB	HC	BRAKEZ	ENB	GHA	GLA	GHB	GLB	GHC	GLC	A	B	C
1	H	L	H	H	L	H	L	L	H	L	L	H	L	Z
	H	L	L	H	L	H	L	L	L	L	H	H	Z	L
	H	H	L	H	L	L	L	H	L	L	H	Z	H	L
	L	H	L	H	L	L	H	H	L	L	L	L	H	Z
	L	H	H	H	L	L	H	L	L	H	L	L	Z	H
	L	L	H	H	L	L	L	L	H	H	L	Z	L	H
0	H	L	H	H	L	L	H	H	L	L	L	L	H	Z
	L	L	H	H	L	L	L	H	L	L	H	Z	H	L
	L	H	H	H	L	H	L	L	L	L	H	H	Z	L

HALL In						Pre-driver						Output		
DIR	HA	HB	HC	BRAKEZ	ENB	GHA	GLA	GHB	GLB	GHC	GLC	A	B	C
0	L	H	L	H	L	H	L	L	H	L	L	H	L	Z
	H	H	L	H	L	L	L	L	H	H	L	Z	L	H
	H	L	L	H	L	L	H	L	L	H	L	L	Z	H
X	H	H	H	H	X	L	L	L	L	L	L	Z	Z	Z
X	L	L	L	H	X	L	L	L	L	L	L	Z	Z	Z
X	X	X	X	L	X	L	H	L	H	L	H	L	L	L

FG

IN1	IN2	IN3	FG1	FG2
H	L	H	H	H
H	L	L	L	H
H	H	L	H	H
L	H	L	L	L
L	H	H	H	L
L	L	H	L	L

BRAKEZ,ENABLE

Input	BRAKEZ	ENABLE
High or Open	Active	Output Off
Low	Stop(Short Brake)	Output On

CLD Function

BRAKEZ Set High	——>	Protection Released and Count Reset(Initial Reset)
DIR Switched	——>	Protection Released and Count Reset
ENABLE 0% Duty	——>	Protection Released and Count Reset
Low Voltage Protection	——>	Protection Released and Count Reset(Initial Reset)
Over Temperature Protection	——>	Stop Counting

FUNCTION DESCRIPTION

Output Drive Circuit

The chip adopts a direct PWM drive method to reduce power . It regulates the drive force of the motor by changing the duty of output. The output PWM switching is performed by the upper-side output transistor. This IC performs synchronous rectification, and is intended to reduce heat generation compared to diode regeneration.

Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation I = VRF/Rf (VRF= 0.20V (typical), Rf: current detection resistor). This circuit suppresses the output current by reducing the duty of output.

The current limiter circuit has an operation delay (approx. 1.2μs) to detect reverse recovery current flowing in the diode due to the PWM operation, and prevent a malfunction of the current limiting operation. If the coil resistance of the motor is small, or the inductance is low, the current at startup (the state in which there is no back electromotive force generated in the motor) will change rapidly. As a result,the operation delay may sometimes cause the current limiting operation to take place when a value is above the set current. In such a case, it is necessary to set the current limit value while taking into consideration the increase in current due to the delay.

The PWM frequency in the current limiter circuit is determined by the internal reference oscillator, and is approximately 50kHz.

Speed Control Method

Pulses are input to the ENABLE pin, and the output can be controlled by varying the duty cycle of these pulses.

When a low-level input voltage is applied to ENABLE pin,the output at the PWM side (upper side) is set to ON.

When a high-level input voltage is applied to ENABLE pin,the output at the PWM side (upper side) is set to OFF.

If it is necessary to input pulses using inverted logic, this can be done by adding an external transistor (NPN).

When the input to the ENABLE pin remains high-level for a certain period, the IC judges that the duty is 0%, causing the CSD circuit count to be reset .

Constraint Protection Circuit

The MS4931 includes a constraint protection circuit for protecting the IC and the motor in a motor constraint mode. This circuit operates when the motor is in an operation condition and the Hall signal does not switch over for a certain period. Note that while this constraint protection is operating, the upper-side output transistor will be OFF.

Time setting is performed according to the capacitance of the capacitor connected to the CLD pin.

Set time (s) ≈ 90 × C (μF)

When a 0.022μF capacitor is connected, the protection time becomes approximately 2.0 seconds. The set time must be selected to a value that provides adequate margin with respect to the motor startup time.

Conditions for releasing the constraint protection state:

- When the BRAKEZ pin is in a STOP state → Protection released and count reset(Initial reset)
- When the DIR pin is switched → Protection released and count reset
- When 0% duty is detected at the PWMIN pin input → Protection released and count reset

- When low-voltage condition is detected → Protection released and count reset (Initial reset)
- When TSD condition is detected → Stop counting

The CLD pin also functions as the initial reset pulse generation pin. If it is connected to ground, the logic circuit will go into a reset state, preventing speed control from taking place. Consequently, when not using constraint protection, connect a resistor of approximately 220kΩ and a capacitor of about 4700pF in parallel to ground.

Low Voltage Protection Circuit

The MS4931 incorporates a comparator that uses the band gap voltage as the reference. The circuit monitors the voltage at the HBIAS pin (5.6V). When the BRAKEZ pin is low and the voltage at the HBIAS pin falls below 4.15V (typ.),the protection circuit is activated .Thus all output transistors are set to OFF.

Thermal Shutdown Circuit

When the IC junction temperature exceeds 154°C (design target value), the thermal shutdown circuit is activated, and all the output transistors are set to OFF.

Hall Input Signal

A pulse input with the amplitude in excess of the hysteresis (35mV maximum) is required for the Hall inputs.

It is desirable that the amplitude of the Hall input signal be 100mVp-p or more in consideration of the effect of noise and phase displacement.

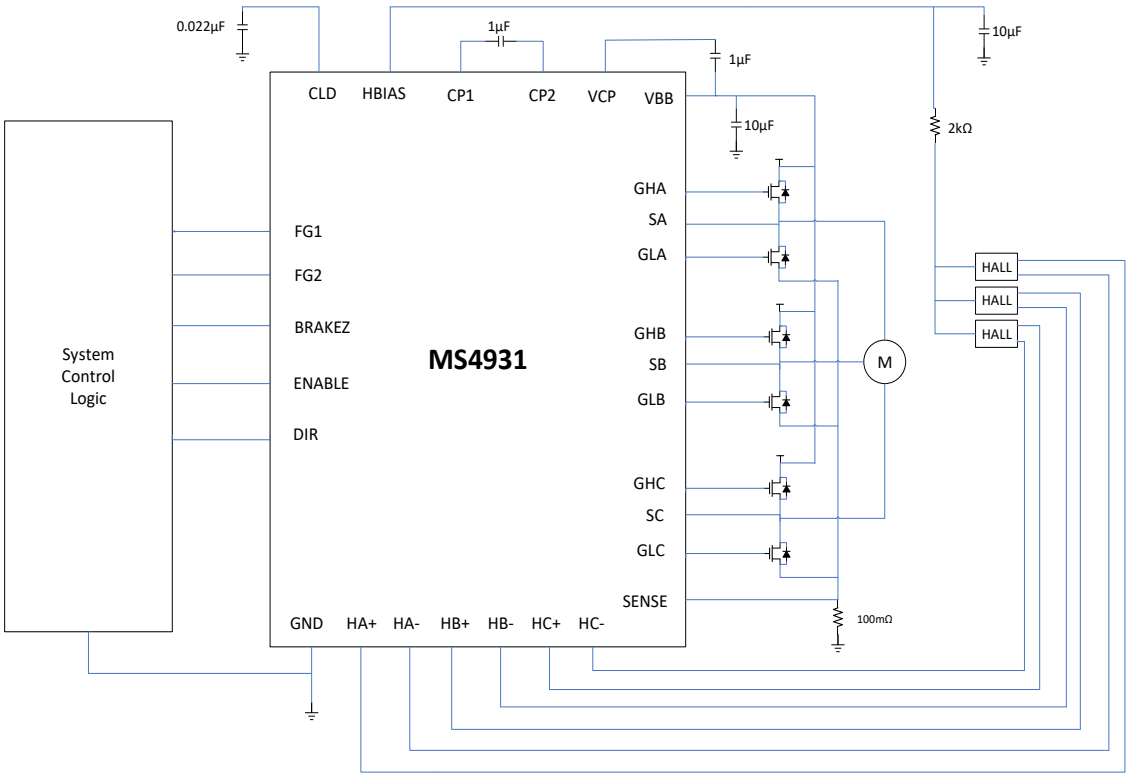
Charge-pump

The charge-pump is used to generate a gate supply greater than the VBB in order to drive the source-side DMOS gates.

A 1μF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes.

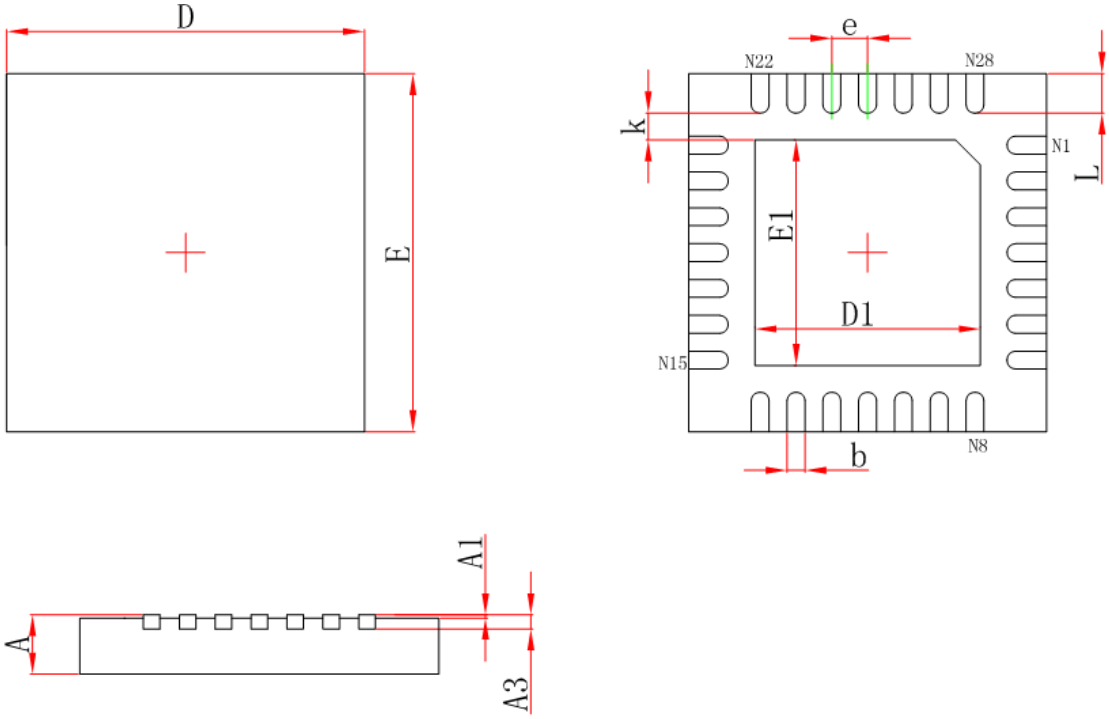
A 1μF ceramic capacitor is required between VCP and VBB to act as a reservoir to operate the high-side DMOS devices.

TYPICAL APPLICATION DIAGRAM



PACKAGE OUTLINE DIMENSIONS

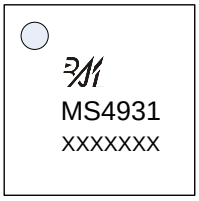
QFN28



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.001	0.002
A3	0.203REF		0.008REF	
b	0.180	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
D1	3.050	3.250	0.120	0.128
E1	3.050	3.250	0.120	0.128
e	0.500TYP		0.020TYP	
L	0.450	0.650	0.018	0.026
k	0.200MIN		0.008MIN	

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS4931

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS4931	QFN28	1000	8	8000	4	32000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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