# N-Channel Depletion-Mode MOSFET

## Ordering Information

| $BV_{DSX}$ / $BV_{DGX}$ | $R_{DS(ON)}$ (max) | $I_{DSS}$ (min) | Order Number / Package |
|---|---|---|---|
| | | | TO-236AB* |
| 500V | 1.0KΩ | 1.0mA | LND250K1 |

*Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

Product marking for SOT-23:

NDE✻

where ✻ = 2-week alpha date code

## Features

- ❑ ESD gate protection
- ❑ Free from secondary breakdown
- ❑ Low power drive requirement
- ❑ Ease of paralleling
- ❑ Excellent thermal stability
- ❑ Integral source-drain diode
- ❑ High input impedance and low $C_{ISS}$

## Advanced DMOS Technology

The LND2 is a high voltage N-channel depletion mode (normally-on) transistor utilizing Supertex's lateral DMOS technology. The gate is ESD protected.

The LND2 is ideal for high voltage applications in the areas of normally-on switches, precision constant current sources, voltage ramp generation and amplification.

## Applications

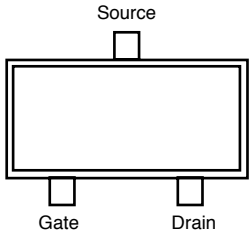
- ❑ Solid state relays
- ❑ Normally-on switches
- ❑ Converters
- ❑ Power supply circuits
- ❑ Constant current sources
- ❑ Input protection circuits

## Absolute Maximum Ratings

| | |
|---|---|
| Drain-to-Source Voltage | $BV_{DSX}$ |
| Drain-to-Gate Voltage | $BV_{DGX}$ |
| Gate-to-Source Voltage | ±20V |
| Operating and Storage Temperature | -55°C to +150°C |
| Soldering Temperature* | 300°C |

* Distance of 1.6 mm from case for 10 seconds.

## Package Options




TO-236AB

(SOT-23)

top view

Note: See Package Outline section for dimensions.

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# Thermal Characteristics

| Package | $I_D$ (continuous)* | $I_D$ (pulsed) | Power Dissipation @$T_A$ = 25°C | $\theta_{jc}$ °C/W | $\theta_{ja}$ °C/W | $I_{DR}$ | $I_{DRM}$* |
|---|---|---|---|---|---|---|---|
| TO-236AB | 13mA | 30mA | 0.36W | 200 | 350 | 13mA | 30mA |

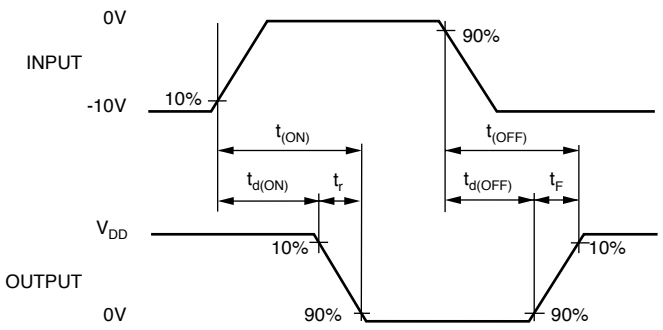
* $I_D$ (continuous) is limited by max rated $T_j$.

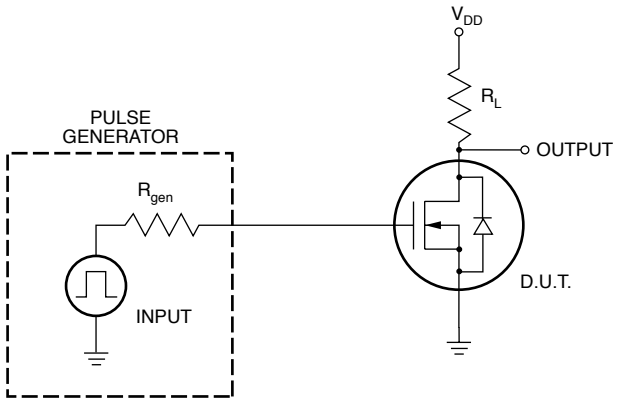
# Electrical Characteristics (@ 25°C unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSX}$ | Drain-to-Source Breakdown Voltage | 500 | | | V | $V_{GS}$ = -10V, $I_D$ = 1.0mA |
| $V_{GS(OFF)}$ | Gate-to-Source OFF Voltage | -1.0 | | -3.0 | V | $V_{DS}$ = 25V, $I_D$ = 100nA |
| $\Delta V_{GS(OFF)}$ | Change in $V_{GS(OFF)}$ with Temperature | | | 5.0 | mV/°C | $V_{DS}$ = 25V, $I_D$ = 100nA |
| $I_{GSS}$ | Gate Body Leakage Current | | | 100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| $I_{D(OFF)}$ | Drain-to-Source Leakage Current | | | 100 | nA | $V_{GS}$ = -10V, $V_{DS}$ = 450V |
| | | | | 100 | µA | $V_{GS}$ = -10V, $V_{DS}$ = 0.8V max rating, $T_A$ =125°C |
| $I_{DSS}$ | Saturated Drain-to-Source Current | 1.0 | | 3.0 | mA | $V_{GS}$ = 0V, $V_{DS}$ = 25V |
| $R_{DS(ON)}$ | Static Drain-to-Source ON-State Resistance | | 850 | 1K | Ω | $V_{GS}$ = 0V, $I_D$ = 0.5mA |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with Temperature | | | 1.2 | %/°C | $V_{GS}$ = 0V, $I_D$ = 0.5mA |
| $G_{FS}$ | Forward Transconductance | 1.0 | 2.0 | | m℧ | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $C_{ISS}$ | Input Capacitance | | 7.5 | 10 | pF | $V_{GS}$ = -10V, $V_{DS}$ = 25V, f = 1MHz |
| $C_{OSS}$ | Output Capacitance | | 2.0 | 3.5 | | |
| $C_{RSS}$ | Reverse Transfer Capacitance | | 0.5 | 1.0 | | |
| $t_{d(ON)}$ | Turn-ON Delay Time | | 0.09 | | µs | $V_{DD}$ = 25V, $I_D$ = 1.0mA, $R_{GEN}$ = 25Ω |
| tr | Rise Time | | 0.45 | | | |
| $t_{d(OFF)}$ | Turn-OFF Delay Time | | 0.1 | | | |
| $t_f$ | Fall Time | | 1.3 | | | |
| $V_{SD}$ | Diode Forward Voltage Drop | | | 0.9 | V | $V_{GS}$ = -10V, $I_{SD}$ = 1.0mA |
| $t_{rr}$ | Reverse Recovery Time | | 200 | | ns | $V_{GS}$ = -10V, $I_{SD}$ = 1.0mA |

**Notes:**
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

# Switching Waveforms and Test Circuit

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