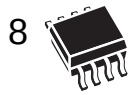
M34A02

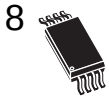
2 Kbit Serial SMBus EEPROM for ACR Card Configuration

PRODUCT PREVIEW

- Two Wire SMBus Serial Interface
- 2.7V to 3.6V Single Supply Voltage
- Hardware Write Control
- BYTE and PAGE WRITE (up to 16 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width

DESCRIPTION

These electrically erasable programmable memory (EEPROM) devices are organized as 256x8 bits, and operate down to 2.7 V.

These devices are available in Plastic Small Outline and Thin Shrink Small Outline packages.

These devices are written by the ACR card-issuer, and then accessed in Read mode in the application, using the ACR Serial Bus protocol. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The device carries a built-in 4-bit Device Type Identifier code (1011).

The device behaves as a slave in the ACR Serial Bus protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition

Figure 1. Logic Diagram

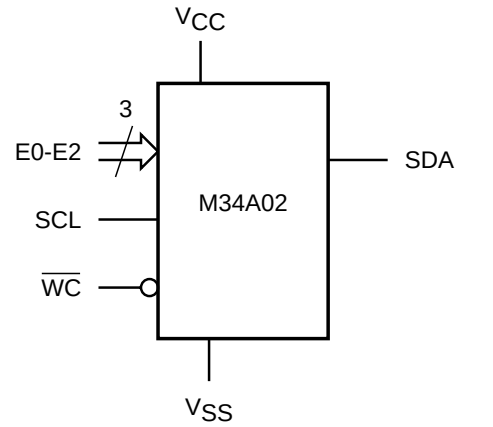


Table 1. Signal Names

E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. SO and TSSOP Connections

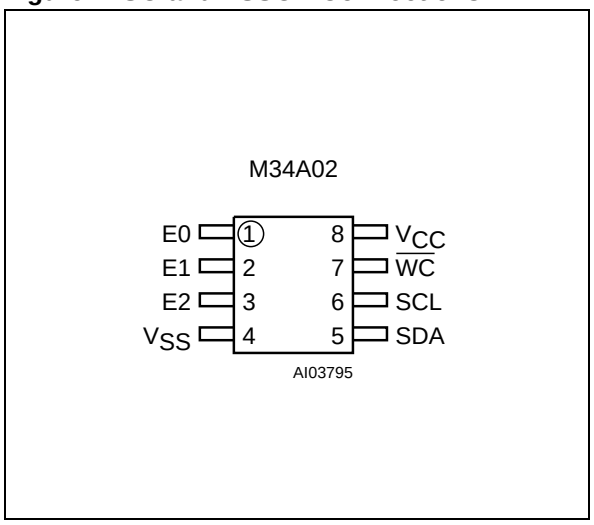
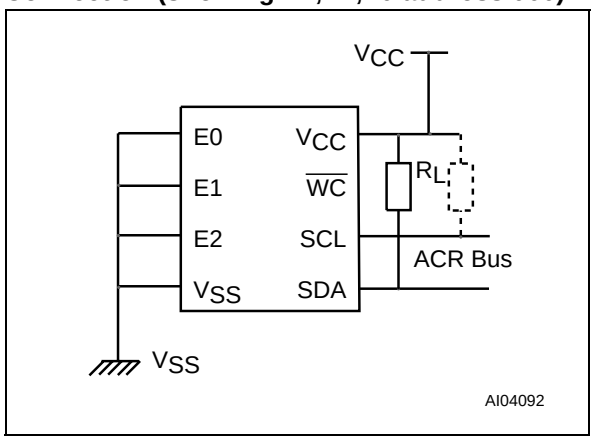


Figure 3. Typical ACR Application PCB Connection (showing E2,E1,E0 address 000)



Note: 1. This arrangement on the chip enable lines allows the application to start at ACR address 000h.

is followed by a Device Select code and R$\overline{W}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. The internal reset is held active until V_{CC} has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this line is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	SO8: 20 seconds (max) [2]	235	°C
		TSSOP8: 20 seconds (max) [2]	235	
V_{IO}	Input or Output range		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [3]		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. IPC/JEDEC J-STD-020A
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. These inputs should be tied to V_{CC} or V_{SS}, to establish the Device Select Code.

Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent erase and write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is held High. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is held High, Device Select and Address bytes are acknowledged, Data bytes are *not* acknowledged.

DEVICE OPERATION

The device supports the ACR Serial Bus protocol. This is summarized in Figure 4. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communication.

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of the SDA line while the clock SCL is stable in the High state. A Stop condition terminates communication between the device and the bus master. A Stop condition at the end of a Read command, provided that it is followed by NoAck, forces the device into its Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL).

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an ACR Serial Bus

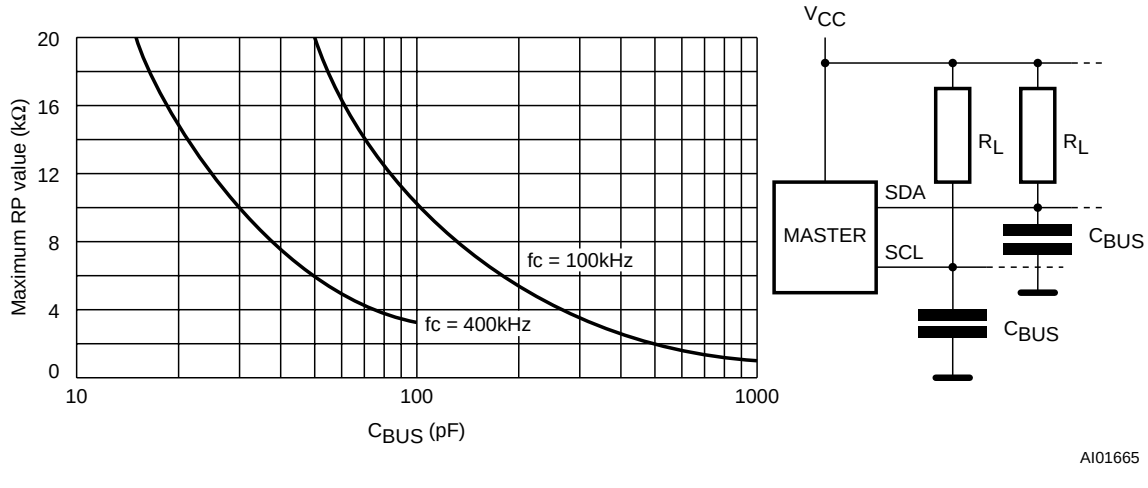
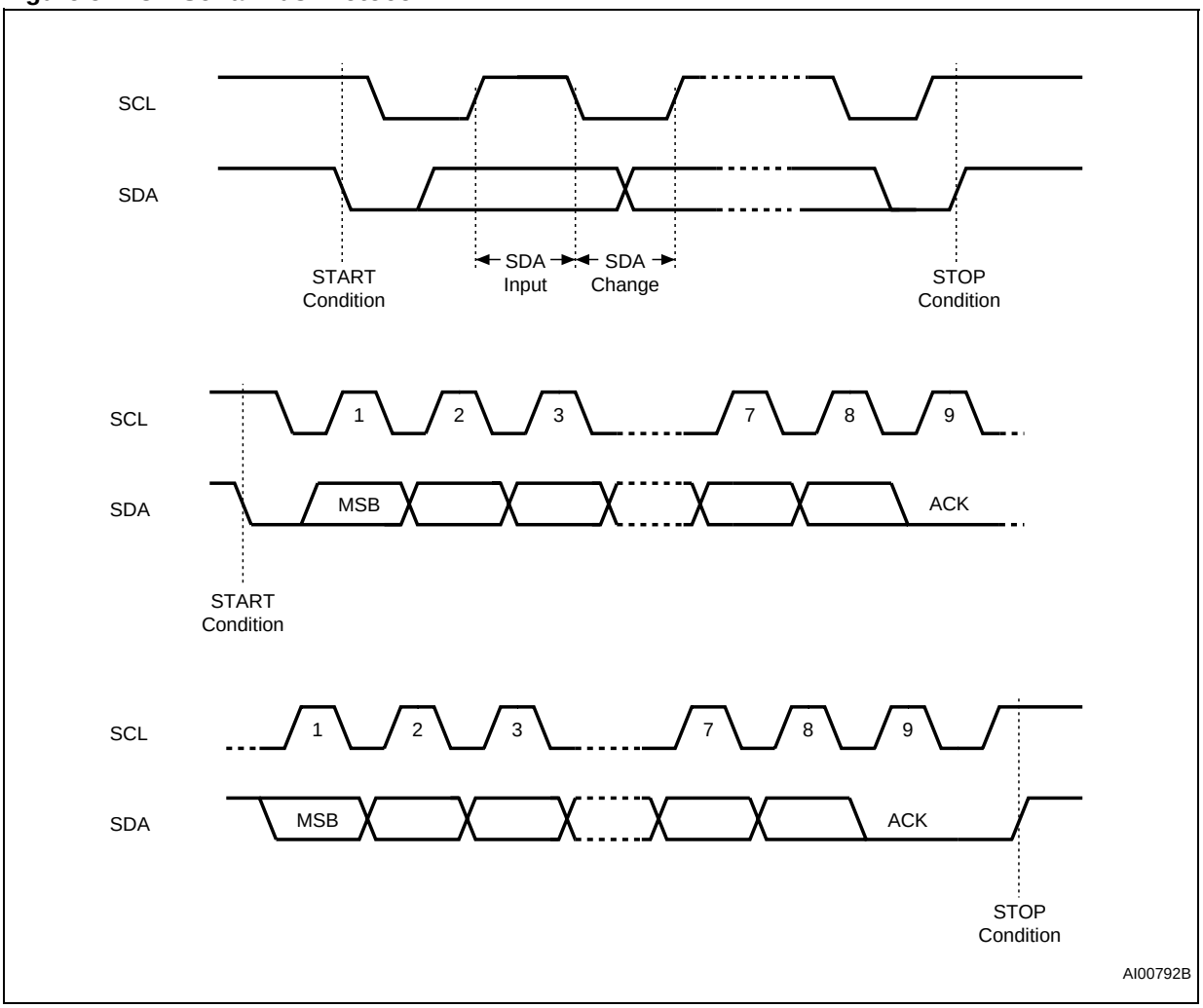


Figure 5. ACR Serial Bus Protocol



For correct device operation, Serial Data (SDA) must be stable before the rising edge of Serial Clock (SCL), and the data must change *only* after Serial Clock (SCL) is Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the 8-bit byte, shown in Table 3, on Serial Data (SDA) (most significant bit first). This consists of the 7-bit Device Select code, and the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1011b.

Up to eight memory devices can be connected on a single bus. Each one is given a unique 3-bit code on Chip Enable (E0, E1, E2). When the Device Select Code is received on Serial Data (SDA), the device only responds if the Chip Select Code is the

Table 3. Device Select Code [1]

	Device Type Identifier				Chip Enable			R$\overline{\text{W}}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	1	E2	E1	E0	R$\overline{\text{W}}$

Note: 1. The most significant bit, b7, is sent first.

Table 4. Operating Modes

Mode	R$\overline{W}$ bit	$\overline{WC}$ [1]	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, R$\overline{W}$ = 1
Random Address Read	0	X	1	START, Device Select, R$\overline{W}$ = 0, Address
	1	X		reSTART, Device Select, R$\overline{W}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, R$\overline{W}$ = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, R$\overline{W}$ = 0

Note: 1. X = V_{IH} or V_{IL}.

same as the pattern applied on Chip Enable (E0, E1, E2).

The 8th bit is the Read/$\overline{Write}$ bit (R$\overline{W}$). This bit is set to 1 for Read and 0 for Write operations. If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Figure 6. Write Mode Sequences with $\overline{WC}$=1 (data write inhibited)

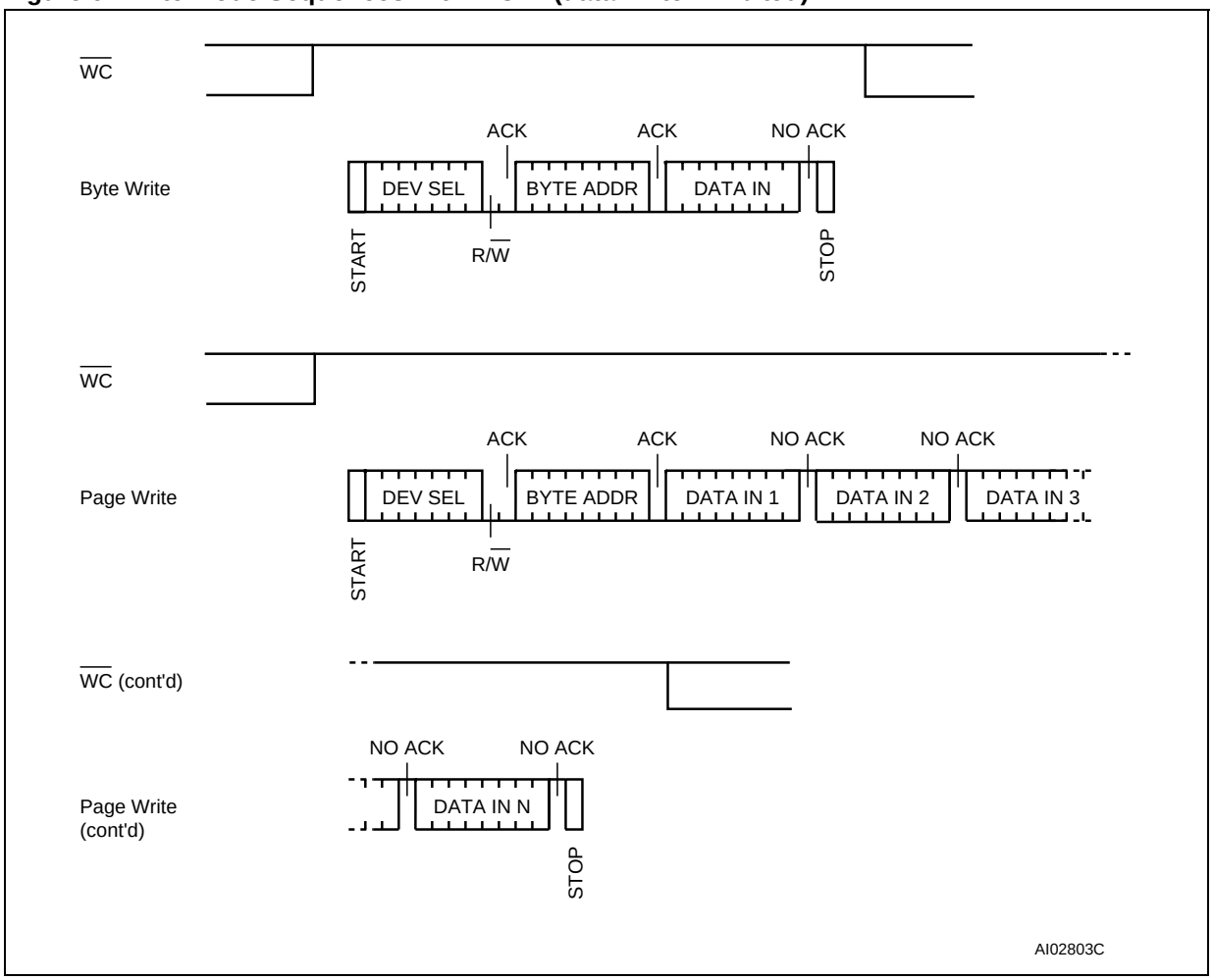
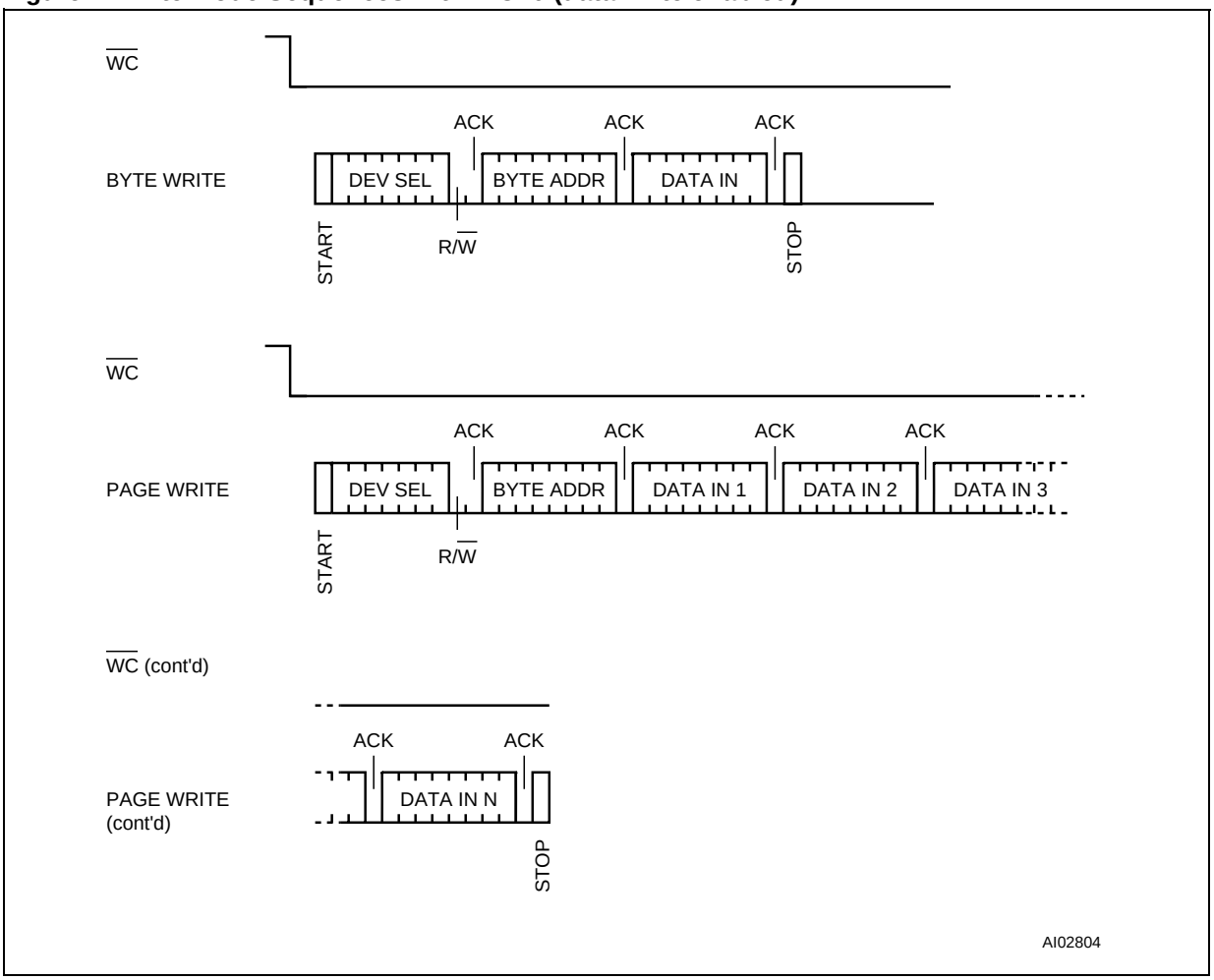


Figure 7. Write Mode Sequences with $\overline{WC}$=0 (data write enabled)



Write Operations

Following a Start condition the bus master sends a Device Select code with the RW bit reset to 0. The device acknowledges this, as shown in Figure 6, and waits for one address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if Write Control ($\overline{WC}$) is taken High. Any Write instruction with Write Control ($\overline{WC}$) held High (during a period of time from the Start condition until the end of the address byte) will not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in Figure 5.

Each data byte in the memory has a 8-bit address.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests (and sends NoAck in reply to them).

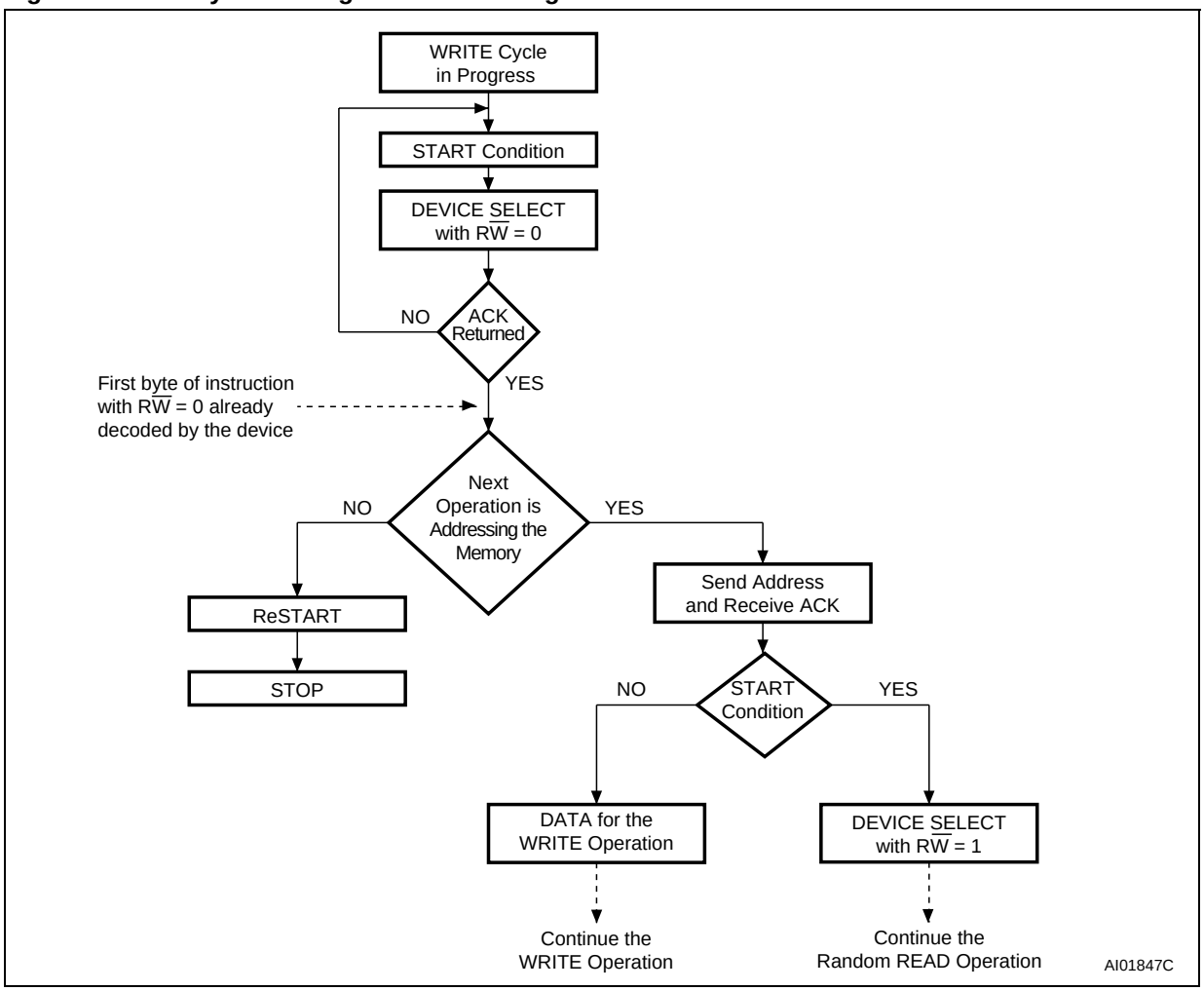
Byte Write

After the Device Select code and the address byte, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$), the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 6.

Page Write

The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits (b7-b4) are the same. If more bytes are sent than will fit up to the end of the row, a condition known

Figure 8. Write Cycle Polling Flowchart using ACK



as 'roll-over' occurs. Data starts to become overwritten (in a way not formally specified in this data sheet).

The bus master sends from one up to 16 bytes of data, each of which is acknowledged by the memory if Write Control ($\overline{WC}$) is Low. If Write Control ($\overline{WC}$) is High, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 4 least significant bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Minimizing System Delays by Polling On ACK

During the internal Write cycle, the device disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Table 6, but the typical time is shorter. To make use of this, an Ack polling sequence can be used by the bus master.

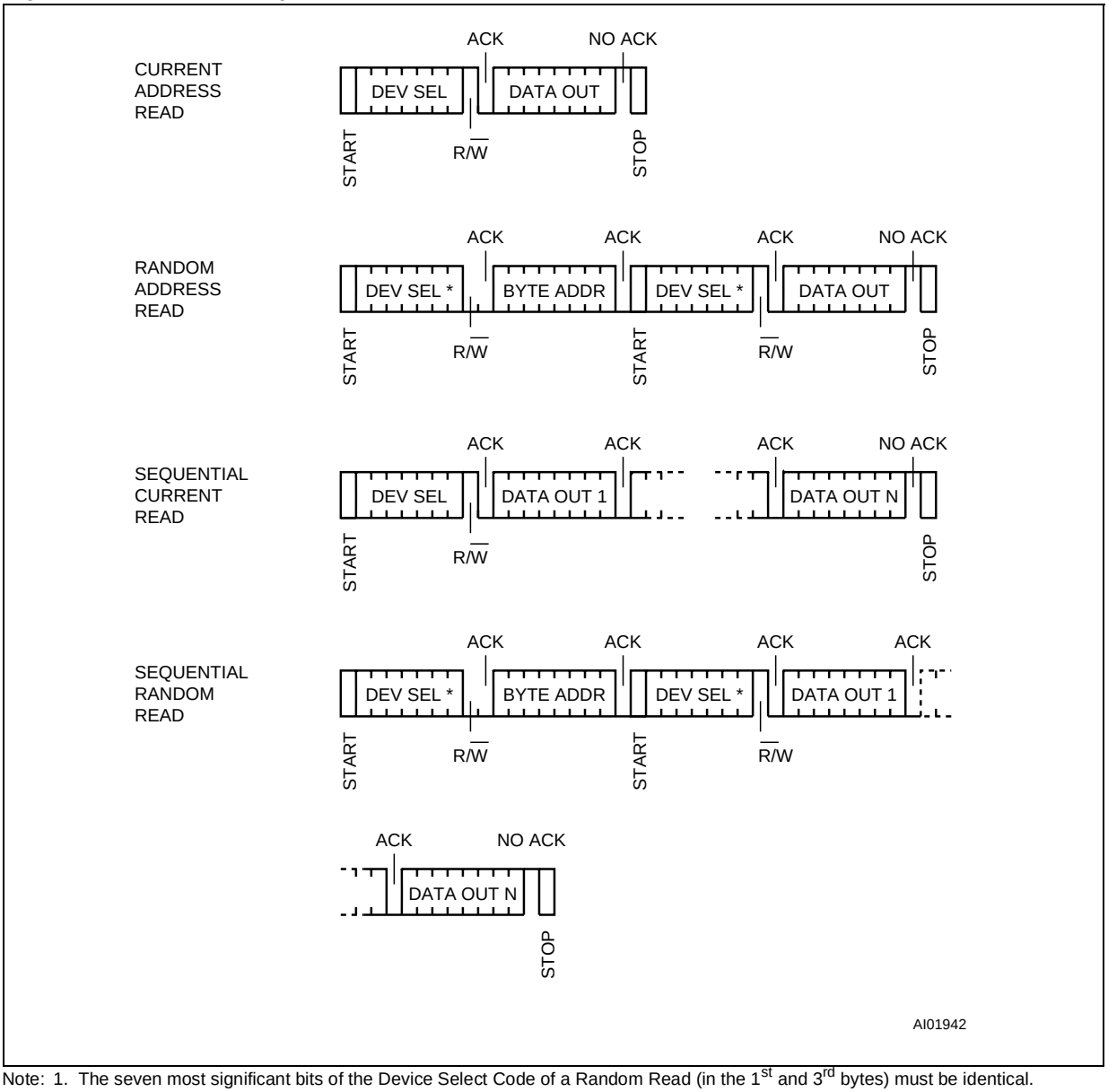
The sequence, as shown in Figure 7, is:

– Initial condition: a Write cycle is in progress.
– Step 1: the bus master issues a Start condition followed by a Device Select code (the first byte of the new instruction).
– Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

Read Operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

Figure 9. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 3rd bytes) must be identical.

Random Address Read

A dummy Write is performed to load the address into the address counter (as shown in Figure 8) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the RW bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 8, *without* acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte

Table 5. DC Characteristics
(T_A = –40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E2, E1, E0)	$0 V \le V_{IN} \le V_{CC}$		± 2	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=3.6V, f_c=100kHz (rise/fall time < 30ns)		2	mA
		V_{CC} =2.7V, f_c=100kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC}		1	µA
V_{IL}	Input Low Voltage (E0-E2, SCL, SDA)		– 0.3	0.8	V
V_{IH}	Input High Voltage (E0-E2, SCL, SDA)		2.1	V_{CC}+1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		– 0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		2.1	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA		0.4	V

Table 6. AC Characteristics

Symbol	Alt.	Parameter	M34A02 V_{CC}=2.7 to 3.6V T_A = –40 to 85°C		Unit
			Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} [2]	t_R	SDA Rise Time		1000	ns
t_{DL1DL2} [2]	t_F	SDA Fall Time		300	ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{CHDX} [1]	$t_{SU:STA}$	START Set-up Time	4.7		µs
t_{DLCL}	$t_{HD:STA}$	START Hold Time	4		µs
t_{DXCX}	$t_{SU:DAT}$	SDA In Set-up Time	250		ns
t_{CLDX}	$t_{HD:DAT}$	SDA In Hold Time	0		µs
t_{CHDH}	$t_{SU:STO}$	STOP Set-up Time	4		µs
t_{DHDL}	t_{BUF}	Time the bus must be free between STOP and next START	4.7		µs
t_{CLQV} [3]	t_{AA}	Clock Low to SDA Out Valid	400	900	ns
t_{CLQX}	t_{DH}	SDA Out Hold Time after Clock Low	300		ns
f_C	f_{SCL}	Clock Frequency	10	100	kHz
t_W	t_{WR}	Write Time		10	ms

Note: 1. For a reStart condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

Figure 10. AC Measurement Conditions

Input Rise and Fall Times	<= 50 ns
Input Pulse Voltages	0.4V to 2.3V
Input and Output Timing Reference Voltages	0.8V to 2.1V

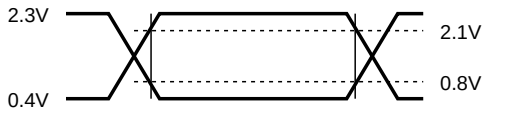


Table 7. Input Parameters[1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	V_{IN} < 0.5 V	5	70	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	V_{IN} > 0.7V_{CC}	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

Note: 1. Sampled only, not 100% tested.

Figure 11. AC Waveforms

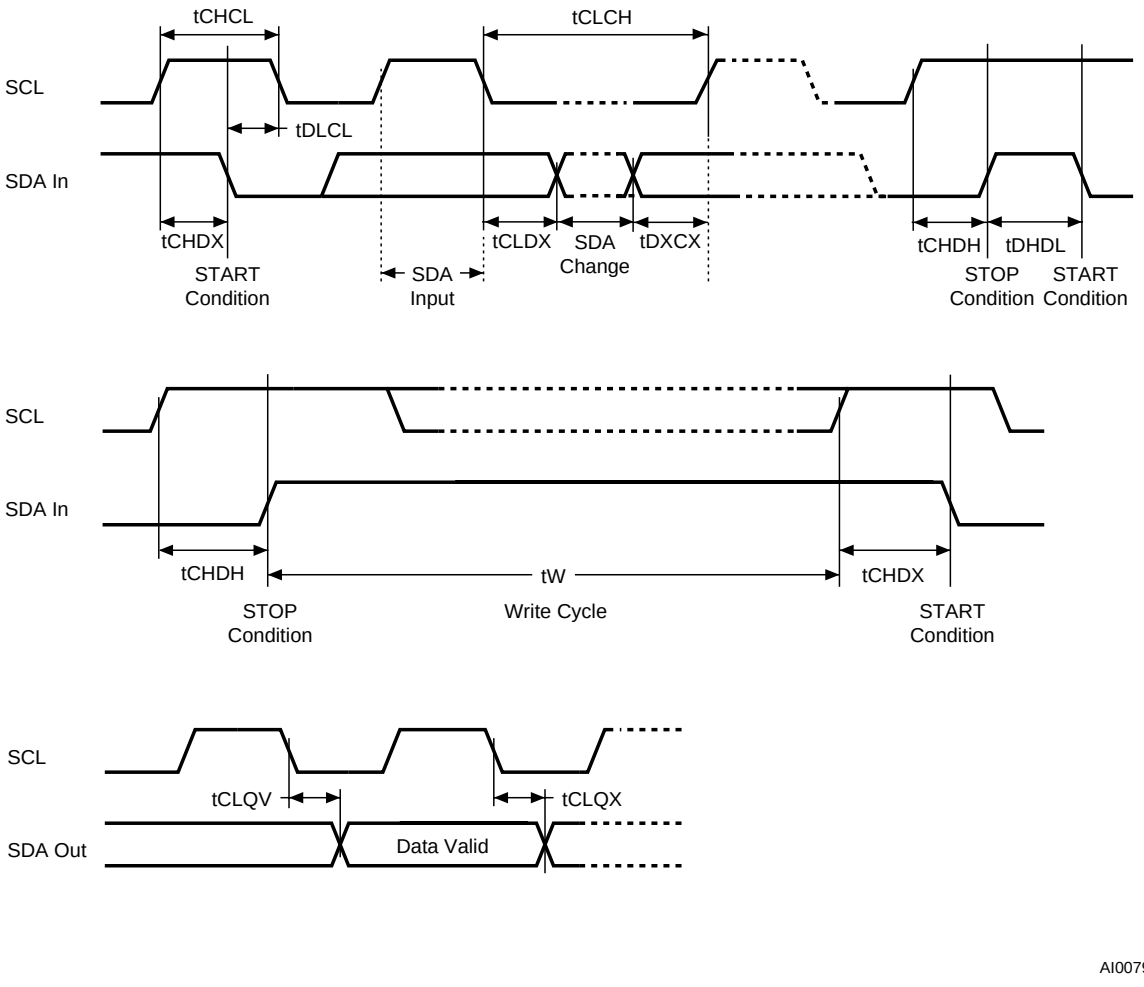
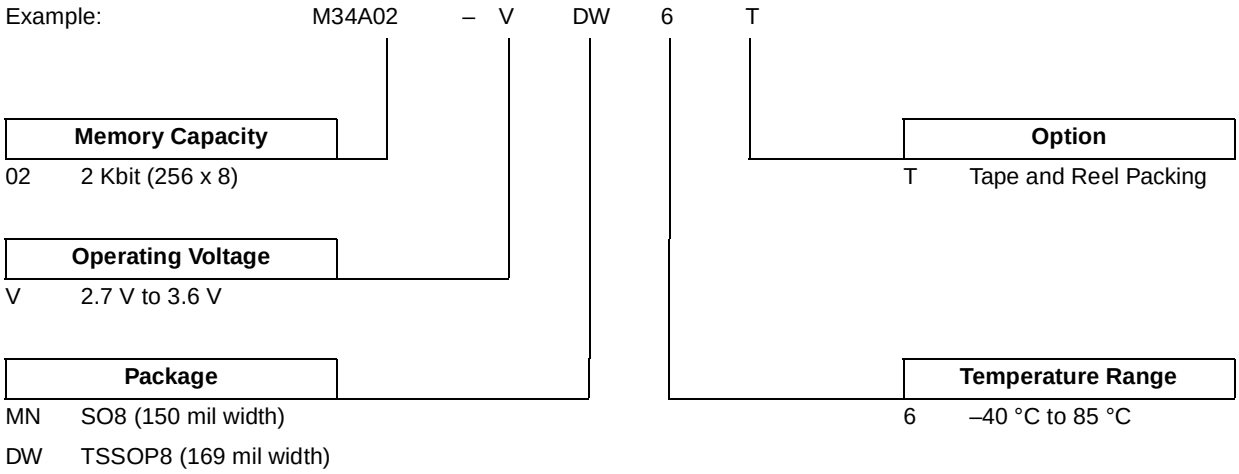


Table 8. Ordering Information Scheme



output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in Figure 8.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

Acknowledge in Read Mode

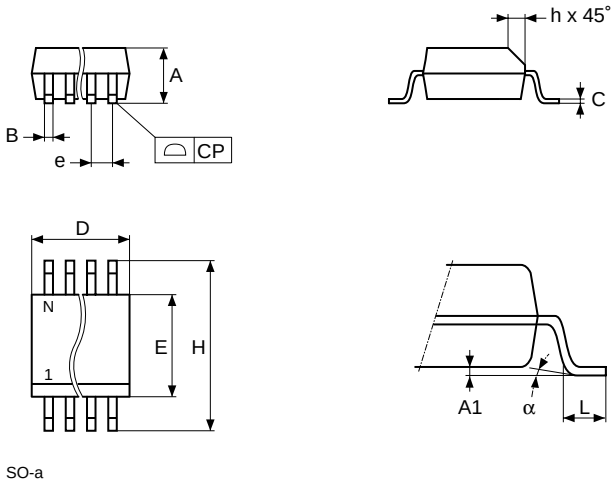
For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Stand-by mode.

ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all 1s (FFh).

The notation used for the device number is as shown in Table 8. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width



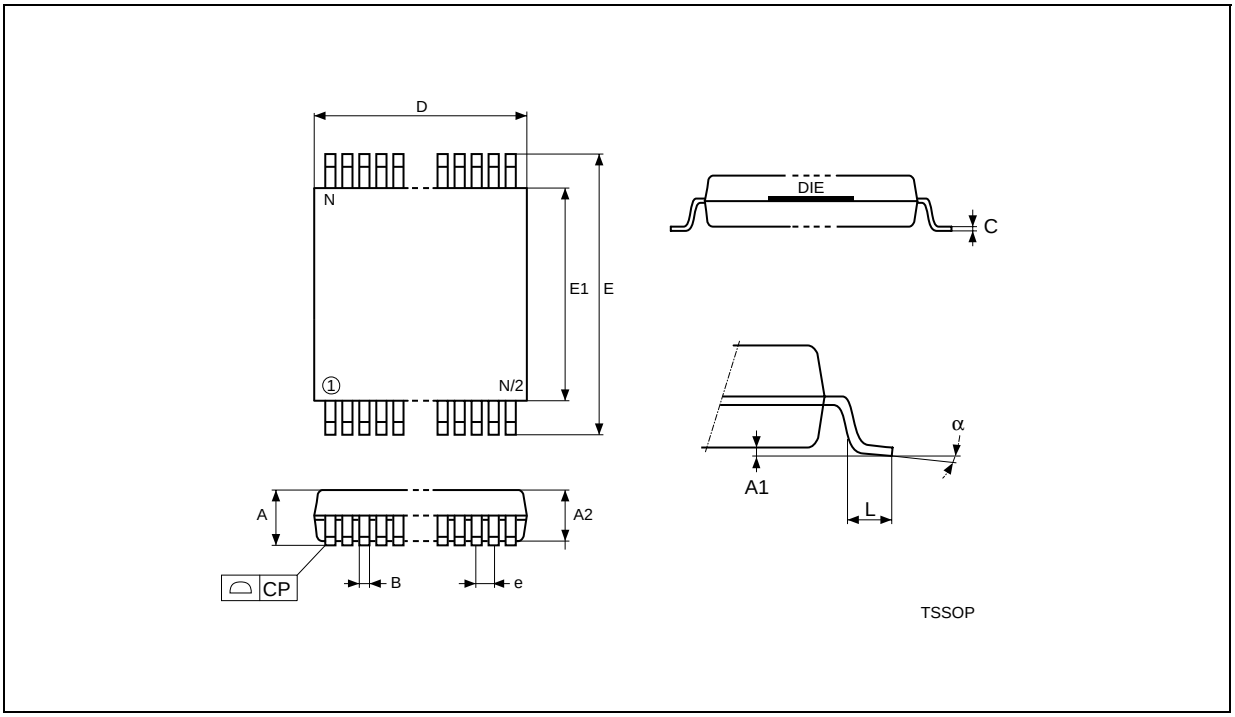
SO-a

Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

TSSOP8 – 8 lead Thin Shrink Small Outline



Note: 1. Drawing is not to scale.

TSSOP8 – 8 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	8			8		
CP			0.08			0.003

Table 9. Revision History

Date	Rev.	Description of Revision
19-Sep-2000	1.0	Document written
14-Mar-2001	1.1	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated
20-Apr-2001	1.2	References to I^2C changed to ACR Serial Bus