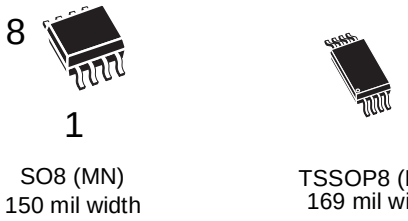
M34C00

3 x 128 bit Serial I²C Bus EEPROM For ee-Tags

PRELIMINARY DATA

- Two-Wire I^2C Serial Interface
  Supports 400 kHz Protocol
- 2.5 V to 5.5 V Single Supply Voltage
- 384-bit EEPROM divided in three areas:
  - 128 bits of non-erasable memory
  - 128 bits of standard EEPROM
  - 128 bits that can be permanently Write-protected (to behave as ROM)
- Self-Timed Program Cycle
- Enhanced ESD/Latch-Up Protection
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention



SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

DESCRIPTION

The M34C00 is a 384-bit serial EEPROM. The bottom third of the memory area (from location 00h to 0Fh) can be Write-protected using a specially designed software Write-protection mechanism. By sending the device a specific sequence, the first 128 bits of the memory become permanently Write-protected. Care must be taken when using this sequence as its effect cannot be reversed.

The top third of the memory area (from location 20h to 2Fh) is already configured to give the functional equivalence of a non-erasable memory. That is, it is initialized to all 1s (FFh), and the user is able to reset any number of those 1s to 0; but there is no mechanism for the user to set a 0 back to a 1.

The M34C00 is a 384-bit electrically erasable programmable memory (EEPROM), organized as 48 x 8 bits.

Figure 1. Logic Diagram

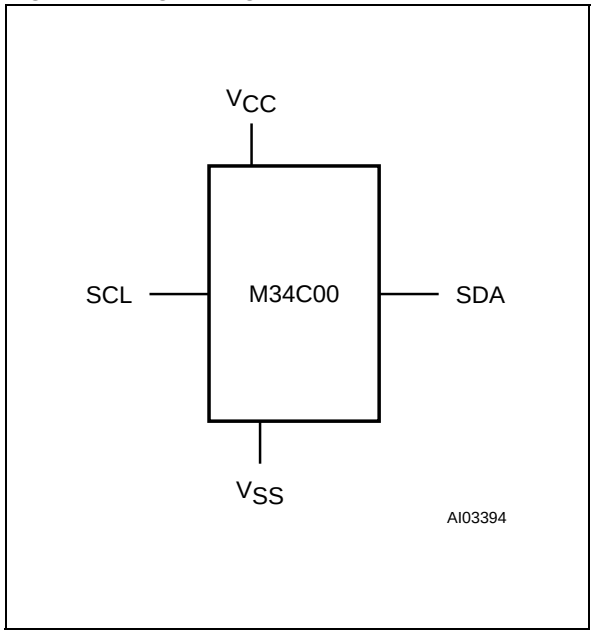
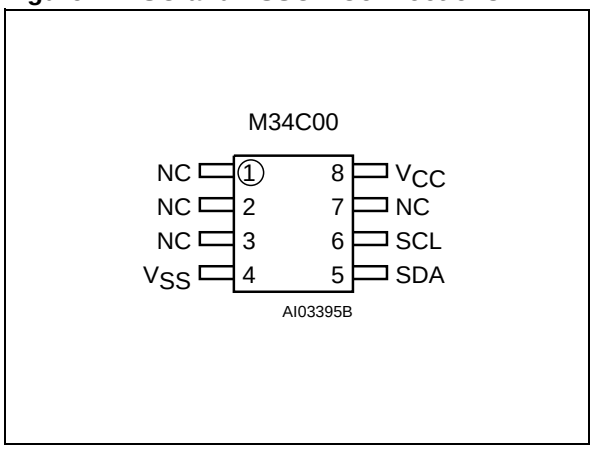


Table 1. Signal Names

SDA	Serial Data
SCL	Serial Clock
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. SO and TSSOP Connections



Note: 1. NC = Not Connected

These devices are compatible with the I^2C memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The device carries a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition to access the memory area and a second Device Type Identifier code (0110) to access the Protection Register.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select code and $\overline{RW}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. The internal reset is held active until V_{CC} has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

This signal is used to strobe all data in and out of the device. In applications where this line is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

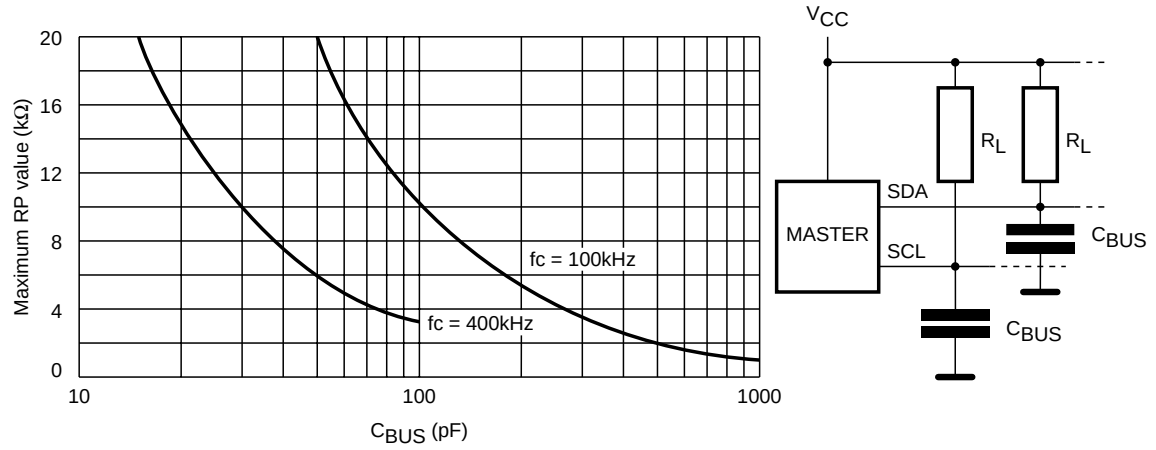
This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	SOT23: t.b.d. SO: 20 seconds (max) [2] TSSOP: 20 seconds (max) [2]	t.b.d. 235 235	°C
V_{IO}	Input or Output range		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [3]		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. IPC/JEDEC J-STD-020A
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus



collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

DEVICE OPERATION

The device supports the I^2C protocol. This is summarized in Figure 4. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M34C00 device is always a slave in all communication.

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a programming cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable, and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Data Input

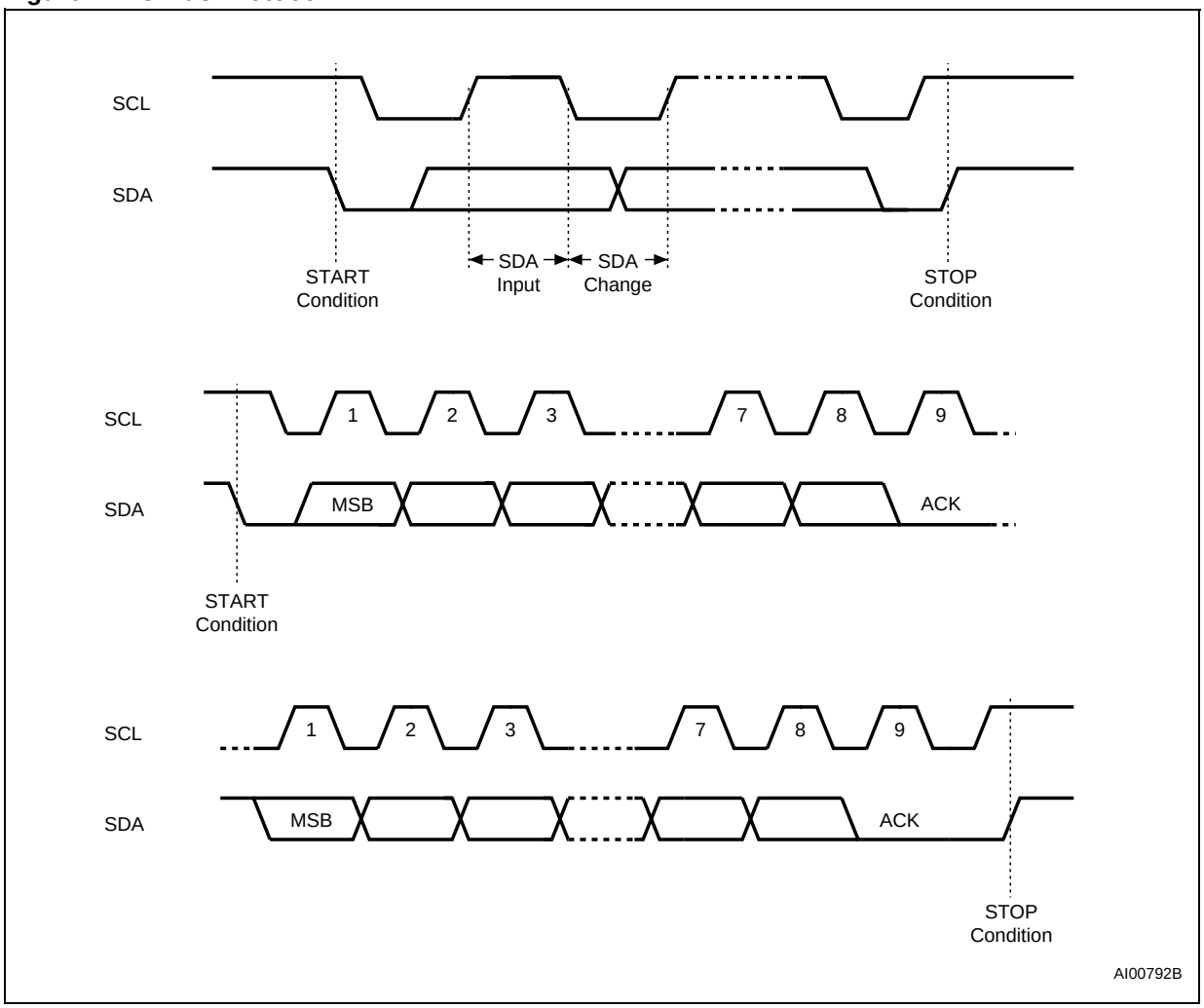
During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the data on Serial Data (SDA)

Table 3. Device Select Code

	Device Type Identifier[1]							$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (three arrays)	1	0	1	0	1	1	1	$R\overline{W}$
Protection Register Select Code	0	1	1	0	1	1	1	$R\overline{W}$

Note: 1. The most significant bit (b7) is sent first.

Figure 4. I²C Bus Protocol



must change *only* when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the 8-bit byte, shown in Table 3, on Serial Data (SDA) (most significant bit first). This consists of the 7-bit Device Select code, and the Read/Write bit (RW).

To address the memory array, the 4-bit Device Type Identifier is 1010b. To address the Protection Register, it is 0110b, as shown in Table 3.

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations. If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Memory Partitioning

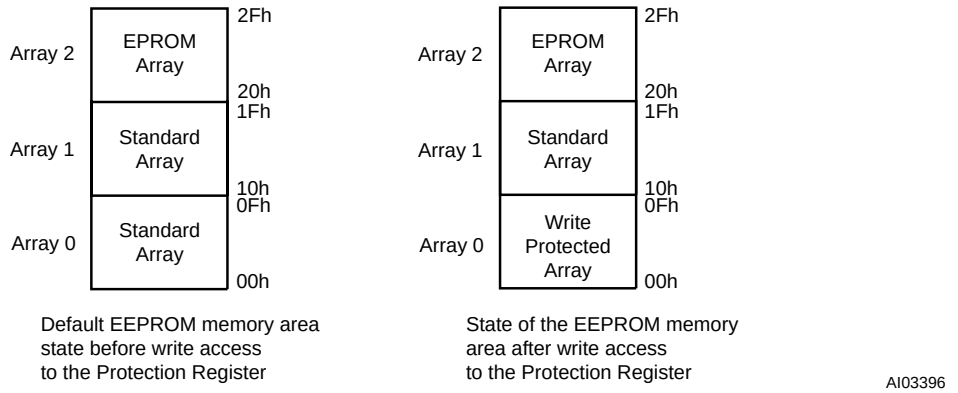
The memory is divided in three arrays:

- Array-0: Write-protectable Array (00h to 0Fh)
- Array-1: EEPROM Array (10h to 1Fh)
- Array-2: Non-Erasable Memory Array (20h to 2Fh)

The 4 least significant bits of the address byte determine the byte that is to be addressed within the given array. The next 2 more significant address bits determine the array that is to be addressed (Array-0, Array-1, Array-2 or Invalid). The 2 most significant address bits are Don't Care.

If the address is of the form xx11xxxx, the device recognises that an attempt is being made to

Figure 5. Memory Partitioning



address the Invalid array, and immediately deselects itself.

The Write-protectable array consists of 16 bytes of EEPROM, which can be used as normal EEPROM until this array is set in its Write-protected mode. Once Write-protected, this array becomes functionally equivalent to a Read-Only Memory (ROM), and cannot be modified further. The procedure to set this array in its Write-protected mode is described later.

Array-2 also consists of 16 bytes of EEPROM, but configured to give the functional equivalence of non-erasable memory. That is, it is initialized to contain all 1s (FFh), with the user able to reset any 1 to a 0, but unable to set any 0 to a 1. One application envisaged for this array is as a non-resettable 128-token array.

WRITE AND READ OPERATIONS

Write Operations

Following a Start condition the bus master sends a Device Select code with the $R\overline{W}$ bit reset to 0. The device acknowledges this, as shown in Figure 6, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

Byte Write

After the Device Select code and the address byte, the bus master sends one data byte. If the addressed location is in the Write-protected area, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not in a Write-protected area, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 6.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

Minimizing System Delays by Polling On ACK

During the internal Write cycle, the device disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Table 6, but the typical time is shorter. To make use of this, an Ack polling sequence can be used by the bus master.

The sequence, as shown in Figure 7, is:

– Initial condition: a Write cycle is in progress.

– Step 1: the bus master issues a Start condition followed by a Device Select code (the first byte of the new instruction).

– Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

Figure 6. Byte Write Sequences (showing differences in Acknowledge bits)

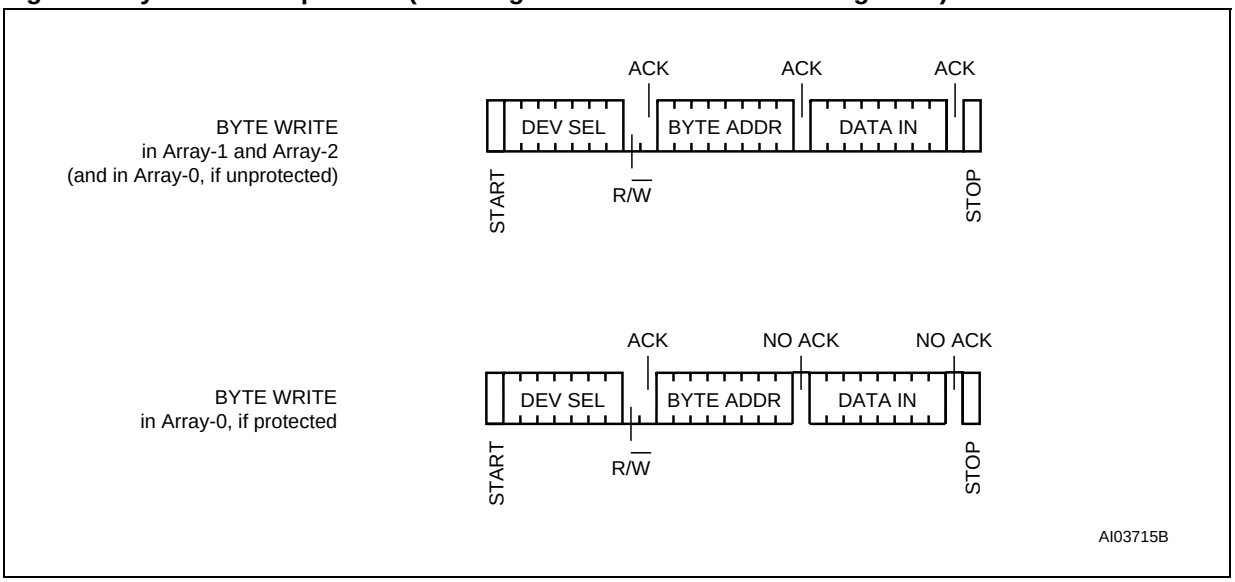
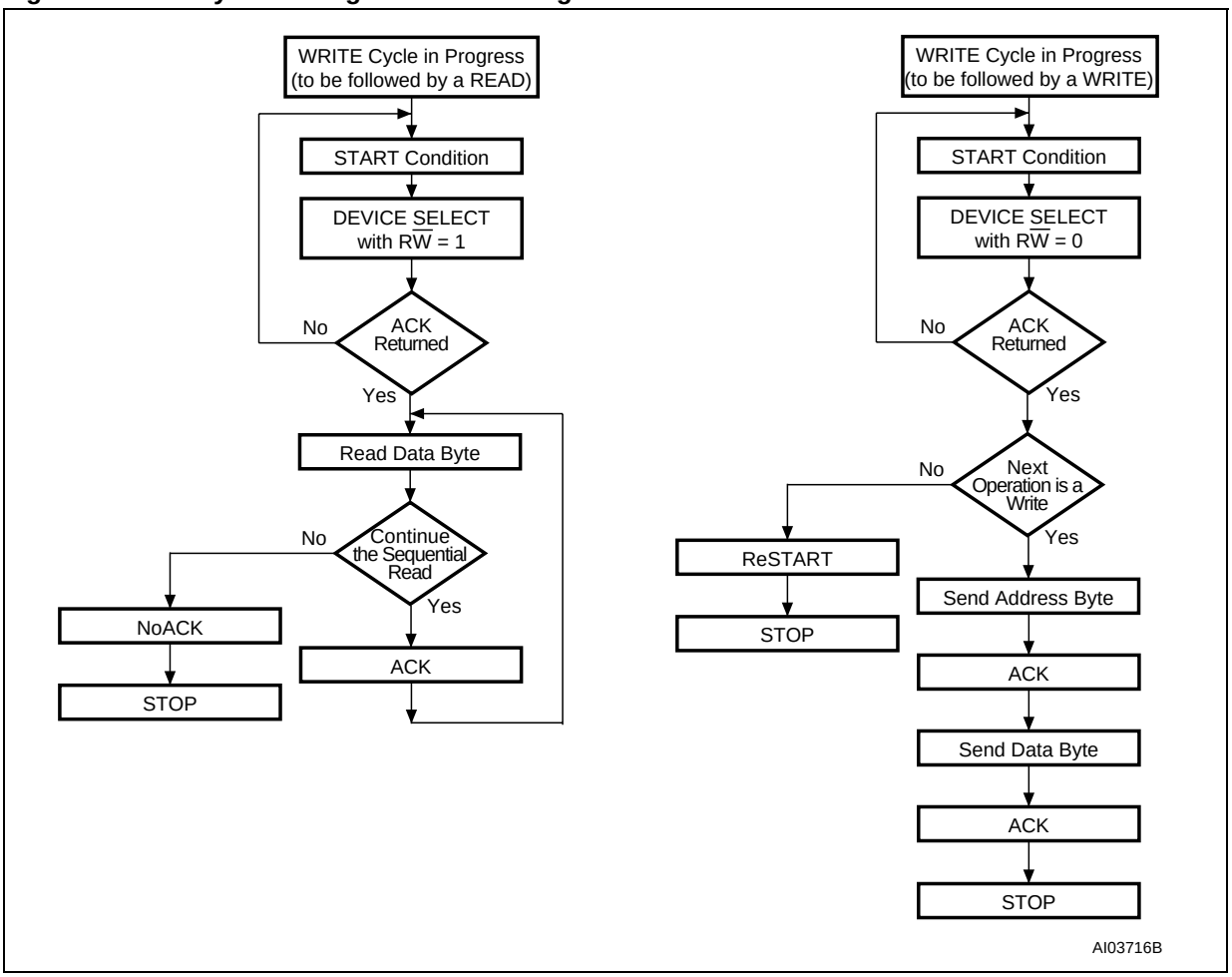


Figure 7. Write Cycle Polling Flowchart using ACK



Read Operation

Following a Start condition, the bus master sends a Device Select code with the RW bit set to 1. The device acknowledges this, and outputs the byte in location 00h. The counter is then incremented, and the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte output, and *must* generate a Stop condition, as shown in Figure 8.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the internal address counter rolls over, to continue reading from the start of the memory.

Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not pull Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Stand-by mode.

Setting the Write-Protection by Writing to the Protection Register

The M34C00 has a software Write-protection function, using the Protection Register, that allows the bottom 16 bytes of the memory area (addresses 00h to 0Fh) to be permanently Write-protected. The Write-protection feature is activated by writing once to the Protection Register.

The Protection Register is written with the device select code set to 0110.1110b (as shown in Figure 9). Address and data bytes must be sent with this command, but their values are all ignored, and are treated as Don't Care. Once the Protection Register has been written, the Write-protection of the first 16 bytes of the memory is enabled, and it is not possible to unprotect these 16 bytes, even if the device is powered off and on.

When the Protection Register has been written, the M34C00 no longer responds to the device type identifier 0110b for either Read or Write operations.

Table 4. Write Time

	Write Time[1]
WRITE to Array-0 (when not protected)	t_W
WRITE to Array-0 (when Write-protected)	0
WRITE to Array-1	t_W
WRITE to Array-2	t_W

Note: 1. For the value to t_W please see Table 6.

Figure 8. Read Sequence

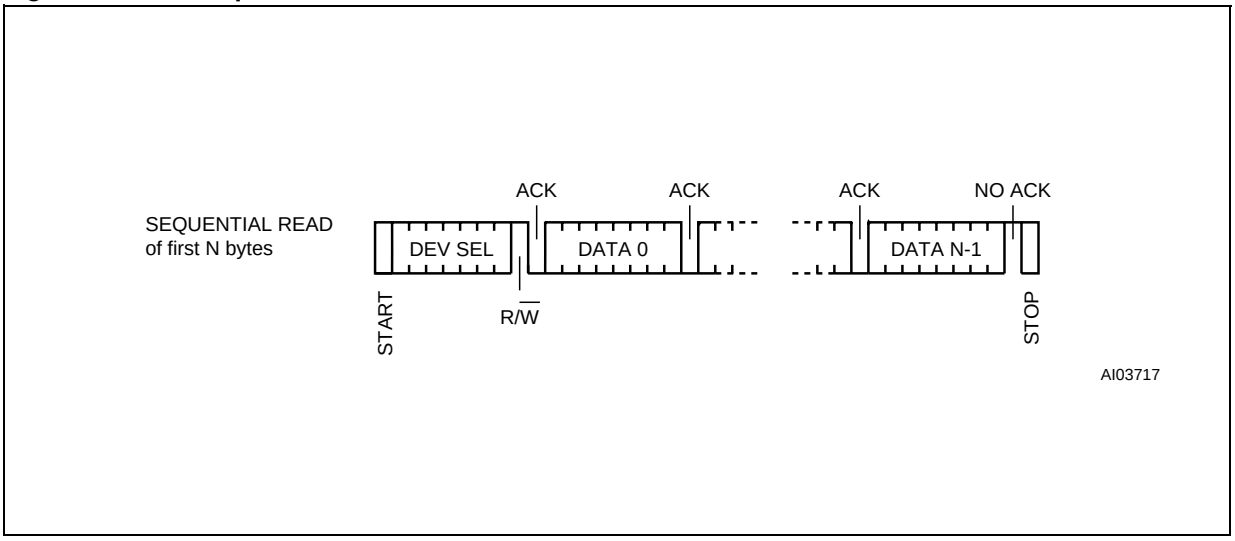
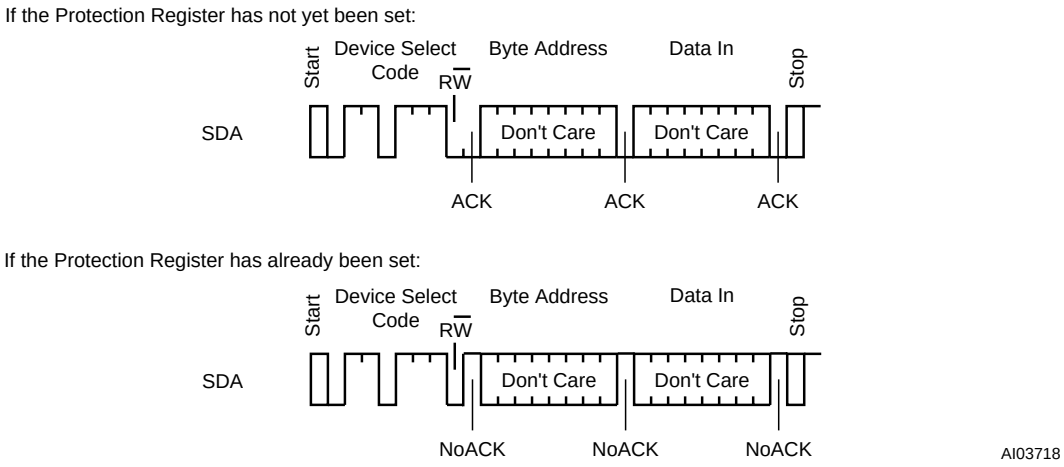


Figure 9. Setting the Protection Register



Reading the Protection Register

To determine whether the Write-protection feature has been activated, it is possible to read the Protection Register, as shown in Figure 10.

– If the Protection Register has not been set, the device acknowledges the read sequence
– If the Protection Register has been set, the device deselects itself after it has received the device select code. Consequently, each part of the sequence is not acknowledged.

Figure 10. Reading the Protection Register

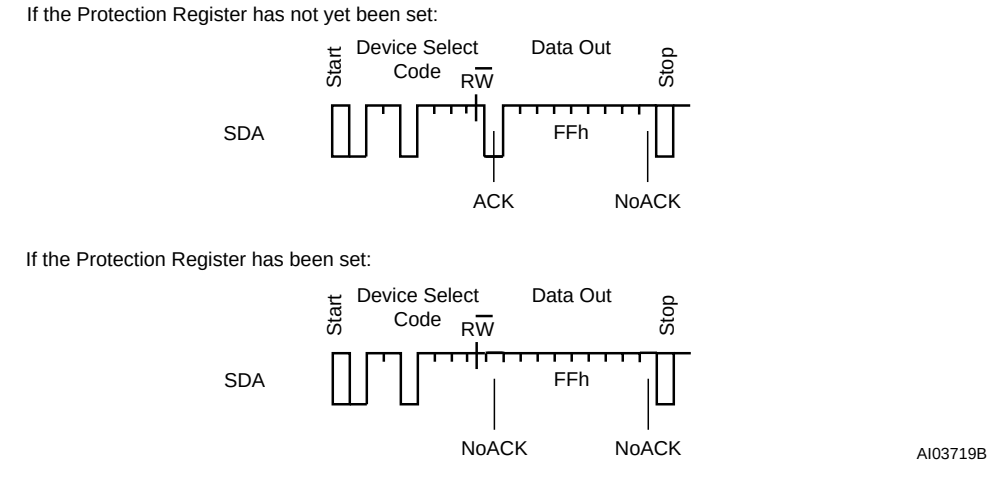


Table 5. DC Characteristics (T_A = –40 to 85 °C; V_{CC} = 2.5 to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current SCL, SDA	0 V ≤ V_{IN} ≤ V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	0 V ≤ V_{OUT} ≤ V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =5.5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{IN} = V_{SS} or V_{CC} , V_{CC} = 5.5 V		2	µA
		V_{IN} = V_{SS} or V_{CC} , V_{CC} = 2.5 V		1	µA
V_{IL}	Input Low Voltage SCL, SDA		–0.3	0.3V_{CC}	V
V_{IH}	Input High Voltage SCL, SDA		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V

Table 6. AC Characteristics

Symbol	Alt.	Parameter	M34C00 V_{CC}=2.5 to 5.5V T_A = –40 to 85°C		Unit
			Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} [2]	t_R	SDA Rise Time	20	300	ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{CHDX} [1]	$t_{SU:STA}$	START Set-up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	START Hold Time	600		ns
t_{DXCX}	$t_{SU:DAT}$	SDA In Set-up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	SDA In Hold Time	0		µs
t_{CHDH}	$t_{SU:STO}$	STOP Set-up Time	600		ns
t_{DHDL}	t_{BUF}	Time the bus must be free between STOP and next START	1.3		µs
t_{CLQV} [3]	t_{AA}	Clock Low to SDA Out Valid	200	900	ns
t_{CLQX}	t_{DH}	SDA Out Hold Time after Clock Low	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Note: 1. For a reStart condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

Figure 11. AC Measurement Conditions

Input Rise and Fall Times	<= 50 ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

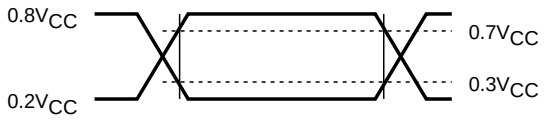


Table 7. Input Parameters [1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch	100	500	ns

Note: 1. Sampled only, not 100% tested.

Figure 12. AC Waveforms

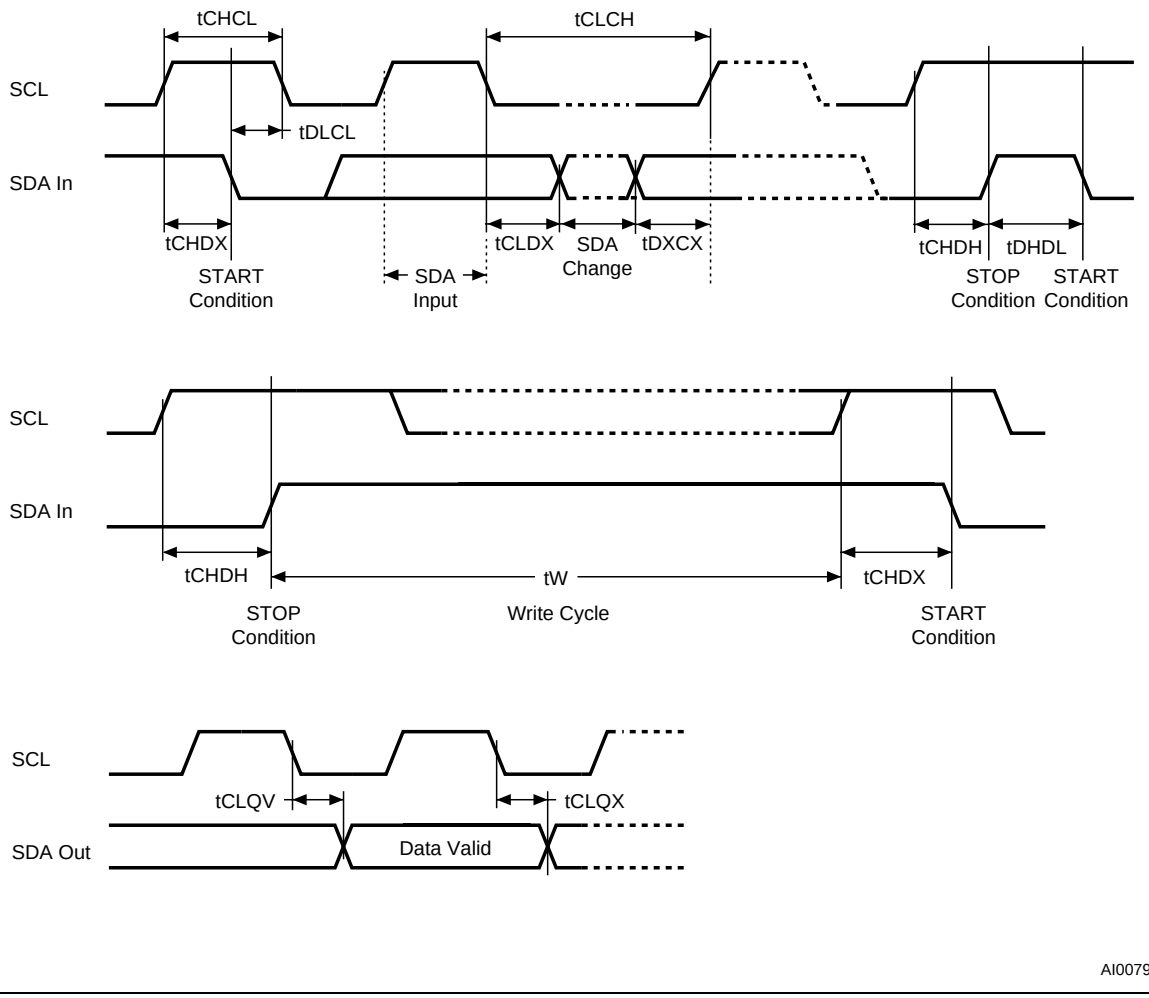


Table 8. Ordering Information Scheme

Example: M34C00 – W MN 6 T

Operating Voltage

W 2.5 V to 5.5 V

Package

MN SO8 (150 mil width)

DW TSSOP8 (169 mil width)

Option

T Tape and Reel Packing

Temperature Range

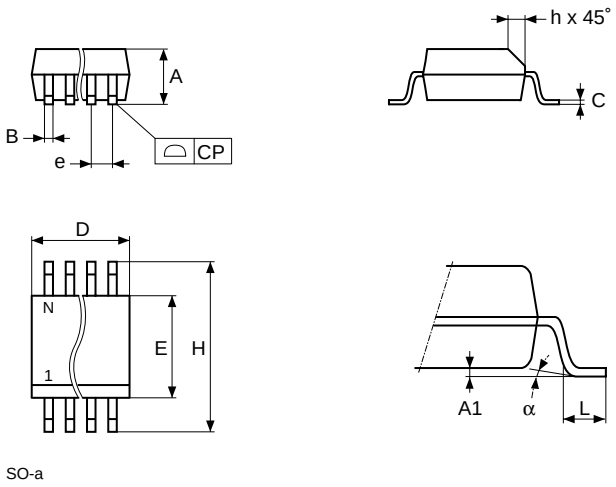
6 –40 °C to 85 °C

ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all 1s (FFh), and the Protection Register set at all 0s (00h).

The notation used for the device number is as shown in Table 8. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width



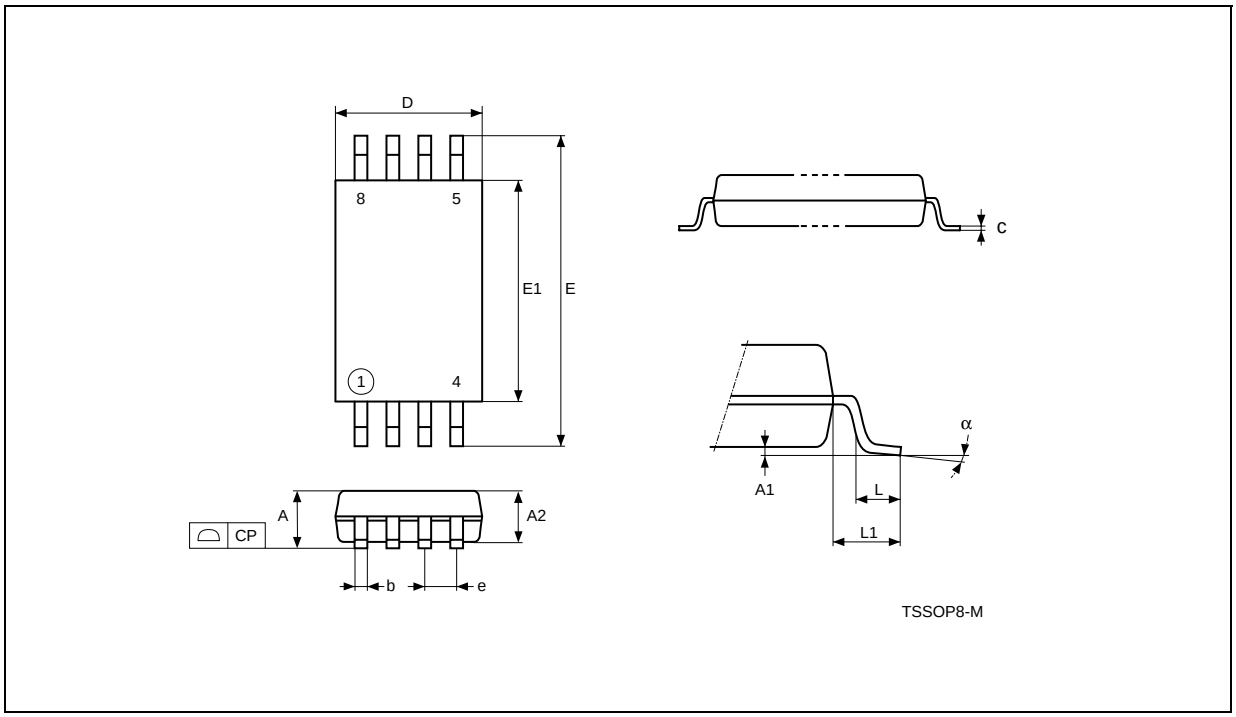
SO-a

Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

TSSOP8 – 8 lead Thin Shrink Small Outline



Note: 1. Drawing is not to scale.

TSSOP8 – 8 lead Thin Shrink Small Outline

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

Table 9. Revision History

Date	Rev	Description of Revision
05-Jan-2000	1.0	Document written
16-Oct-2000	1.1	Wording changes, according to the standard glossary Explanation of Writing to the Protection Register, and Reading from it Addition of the SOT23-5 package on pp 1, 2, ordering info, and mechanical data
26-Feb-2001	1.2	SOT23 Connections modified Paragraphs added on Don't Care bits in the address byte, and the effect of address in the Invalid array Attempts to read beyond the end of the memory cause roll-over to occur Reading the protection register does not involve sending an address byte
08-Jun-2001	1.3	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated Package mechanical data updated for TSSOP8 package according to JEDEC\MO-153
27-Aug-2001	1.4	Document promoted from "Product Preview" to "Preliminary Data" status SOT23-5 package removed