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# 74AC/ACT11471

## Octal transceiver/register with dual enable, INV (3-State)

### FEATURES

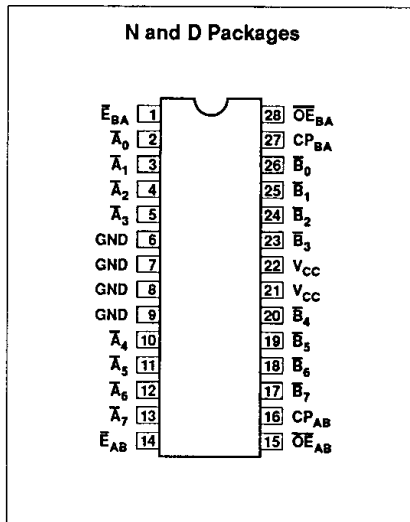
- Combines '245 and '374 type functions in one chip
- 8-bit octal transceiver with D-type flip-flops
- 3-State buffers
- Output capability:  $\pm 24$  mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 $\Omega$  incident wave switching
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: MSI

### DESCRIPTION

The 74AC/ACT11471 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11471 Octal Transceiver/ Register contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Dual Enable ( $\overline{E}_{AB}$ ,  $\overline{E}_{BA}$ ) and Output Enable ( $\overline{OE}_{AB}$ ,  $\overline{OE}_{BA}$ ) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

### PIN CONFIGURATION



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS		TYPICAL		UNIT
		$T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}; V_{CC} = 5.0\text{V}$		AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay $CP_{XX}$ to $\overline{A}_n$ or $\overline{B}_n$	$C_L = 50\text{pF}$		5.7	7.1	ns
$C_{PD}$	Power dissipation capacitance per register <sup>1</sup>	$f = 1\text{MHz}; C_L = 50\text{pF}$	Enabled	36	42	pF
			Disabled	23	28	
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$		4.5	4.5	pF
$C_{VO}$	I/O capacitance	$V_{VO} = 0\text{V}$ or $V_{CC}$ ; Disabled		12.0	12.0	pF
$I_{LATCH}$	Latch-up current	Per Jeduc JC40.2 Standard 17		500	500	mA
$f_{MAX}$	Maximum clock frequency	$C_L = 50\text{pF}$		135	125	MHz

#### Note:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

$f_I$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,

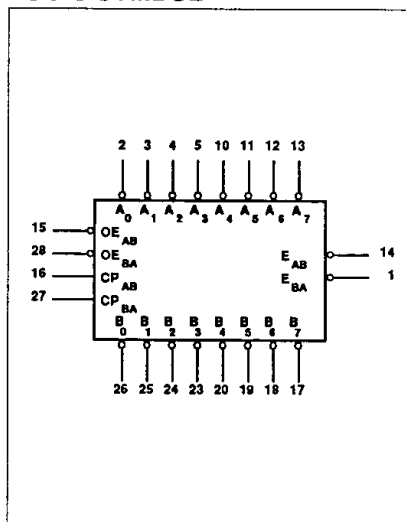
$f_O$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$  = sum of outputs

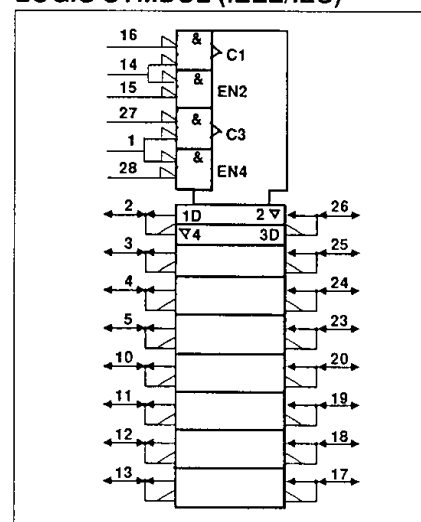
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11471N 74ACT11471N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11471D 74ACT11471D

### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



# Octal transceiver/register with dual enable, INV (3-State)

74AC/ACT11471

## PIN DESCRIPTION

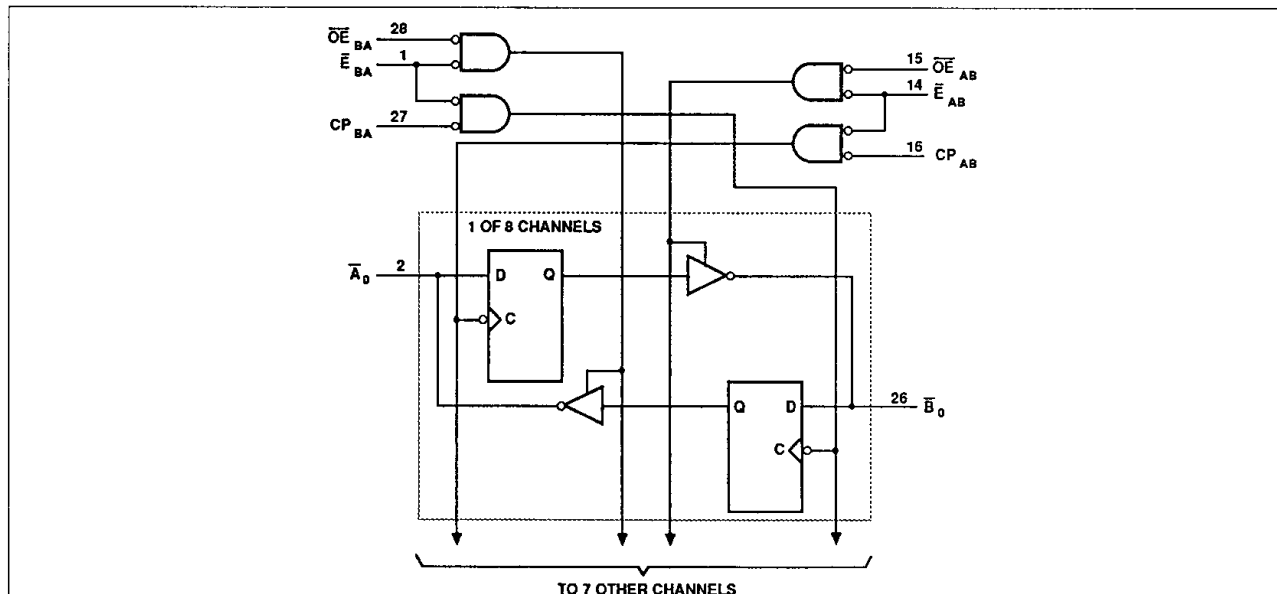
PIN NUMBER	SYMBOL	NAME AND FUNCTION
16	$CP_{AB}$	A-to-B clock input (active Low)
27	$CP_{BA}$	B-to-A clock input (active Low)
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0 - \overline{A}_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0 - \overline{B}_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	$V_{CC}$	Positive supply voltage

## FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{xx}$	$\overline{E}_{xx}$	$CP_{xx}$	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs and clock disabled
L	L	↑	l h	H L	Load register
X	↑	L	l h	Z	Load register and disable outputs

- H = High voltage level
- h = High state present one setup time before the Low-to-High transition
- L = Low voltage level
- l = Low state present one setup time before the Low-to-High transition
- ↑ = Low-to-High transition
- X = Don't care
- Z = High-impedance state

## LOGIC DIAGRAM



# Octal transceiver/register with dual enable, INV (3-State)

## 74AC/ACT11471

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11471			74ACT11471			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40		+85	-40		+85	°C

**NOTE:**

1. No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 TO +7.0	V
$I_{IK}$ or $V_I$	DC input diode current <sup>2</sup>	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_O$	DC output diode current <sup>2</sup>	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current per output pin	$V_O = 0$ to $V_{CC}$	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		$\pm 400$	mA
	DC ground current		$\pm 400$	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# Octal transceiver/register with dual enable, INV (3-State)

## 74AC/ACT11471

### DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> V	74AC11471				74ACT11471				UNIT	
				T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C		T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
I <sub>OH</sub> = -75mA <sup>1</sup>	5.5			3.85				3.85					
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
			I <sub>OL</sub> = 24mA	4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I <sub>OL</sub> = 75mA <sup>1</sup>	5.5				1.65				1.65				
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I <sub>OZ</sub>	3-State output off-state current	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> , V <sub>O</sub> = V <sub>CC</sub> or GND	5.5		±0.5		5.0		±0.5		5.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA	

#### NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

# Octal transceiver/register with dual enable, INV (3-State)

## 74AC/ACT11471

### AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11471					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	75	100		75		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagaion delay, CP <sub>BA</sub> to $\overline{A}_n$ or CP <sub>AB</sub> to $\overline{B}_n$	1	4.7 5.2	7.7 8.3	9.1 9.9	4.7 5.2	10.2 11.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	5.1 6.3	8.2 9.6	9.6 11.2	5.1 6.3	10.6 12.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	5.8 6.9	8.9 10.4	10.4 12.1	5.8 6.9	11.4 13.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	4.9 4.9	7.3 7.1	8.8 8.4	4.9 4.9	9.4 9.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	5.2 5.3	7.7 7.7	9.2 9.2	5.2 5.3	9.9 9.8	ns
t <sub>S</sub>	Setup time, High or Low $\overline{A}_n$ to CP <sub>AB</sub> or $\overline{B}_n$ to CP <sub>BA</sub>	3	1.5			1.5		ns
t <sub>H</sub>	Hold time, High or Low CP <sub>BA</sub> to $\overline{A}_n$ or CP <sub>AB</sub> to $\overline{B}_n$	3	2.0			2.0		ns
t <sub>S</sub>	Setup time, High or Low $\overline{A}_n$ to $\overline{E}_{AB}$ or $\overline{B}_n$ to $\overline{E}_{BA}$	3	2.0			2.0		ns
t <sub>H</sub>	Hold time, High or Low $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	2.0			2.0		ns
t <sub>W</sub>	Clock pulse width High or Low	1	6.5			6.5		ns

# Octal transceiver/register with dual enable, INV (3-State)

## 74AC/ACT11471

### AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11471					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	110	135		110		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay, CP <sub>BA</sub> to $\overline{A}_n$ or CP <sub>AB</sub> to $\overline{B}_n$	1	2.6 3.2	5.2 6.1	6.9 8.0	2.6 3.2	7.6 8.8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	2.9 4.1	5.7 7.2	7.2 9.1	2.9 4.1	7.9 10.2	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	3.4 4.5	6.1 7.6	7.8 9.7	3.4 4.5	8.6 10.8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	3.6 3.6	5.8 5.7	7.3 7.1	3.6 3.6	7.8 7.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	3.8 3.9	6.0 6.0	7.7 7.7	3.8 3.9	8.2 8.1	ns
t <sub>S</sub>	Setup time, High or Low $\overline{A}_n$ to CP <sub>AB</sub> or $\overline{B}_n$ to CP <sub>BA</sub>	3	1.5			1.5		ns
t <sub>H</sub>	Hold time, High or Low CP <sub>BA</sub> to $\overline{A}_n$ or CP <sub>AB</sub> to $\overline{B}_n$	3	1.5			1.5		ns
t <sub>S</sub>	Setup time, High or Low $\overline{A}_n$ to $\overline{E}_{AB}$ or $\overline{B}_n$ to $\overline{E}_{BA}$	3	2.0			2.0		ns
t <sub>H</sub>	Hold time, High or Low $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	1.5			1.5		ns
t <sub>W</sub>	Clock pulse width High or Low	1	4.5			4.5		ns

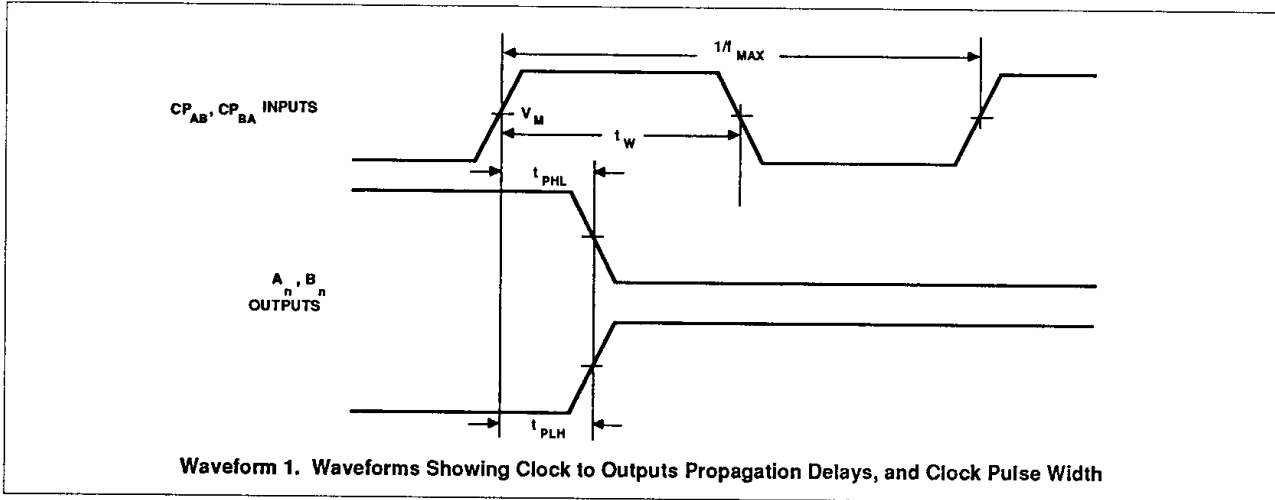
# Octal transceiver/register with dual enable, INV (3-State)

## 74AC/ACT11471

### AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11471					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	90	125		90		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagaion delay, CP <sub>BA</sub> to $\bar{A}_n$ or CP <sub>AB</sub> to $\bar{B}_n$	1	4.0 4.5	6.9 7.7	8.5 9.5	4.0 4.5	9.4 10.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{OE}_{BA}$ to $\bar{A}_n$ or $\overline{OE}_{AB}$ to $\bar{B}_n$	2	3.4 4.6	6.6 8.2	9.0 10.8	3.4 4.6	9.9 11.9	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\bar{E}_{BA}$ to $\bar{A}_n$ or $\bar{E}_{AB}$ to $\bar{B}_n$	2	3.7 4.7	7.0 8.5	9.3 11.2	3.7 4.7	10.3 12.4	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{OE}_{BA}$ to $\bar{A}_n$ or $\overline{OE}_{AB}$ to $\bar{B}_n$	2	5.0 5.2	7.5 7.5	9.0 8.9	5.0 5.2	9.7 9.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\bar{E}_{BA}$ to $\bar{A}_n$ or $\bar{E}_{AB}$ to $\bar{B}_n$	2	5.1 5.3	7.6 7.7	9.2 9.3	5.1 5.3	10.0 10.0	ns
t <sub>S</sub>	Setup time, High or Low $\bar{A}_n$ to CP <sub>AB</sub> or $\bar{B}_n$ to CP <sub>BA</sub>	3	1.5			1.5		ns
t <sub>H</sub>	Hold time, High or Low CP <sub>BA</sub> to $\bar{A}_n$ or CP <sub>AB</sub> to $\bar{B}_n$	3	2.5			2.5		ns
t <sub>S</sub>	Setup time, High or Low $\bar{A}_n$ to $\bar{E}_{AB}$ or $\bar{B}_n$ to $\bar{E}_{BA}$	3	2.0			2.0		ns
t <sub>H</sub>	Hold time, High or Low $\bar{E}_{BA}$ to $\bar{A}_n$ or $\bar{E}_{AB}$ to $\bar{B}_n$	3	2.5			2.5		ns
t <sub>W</sub>	Clock pulse width High or Low	1	5.5			5.5		ns

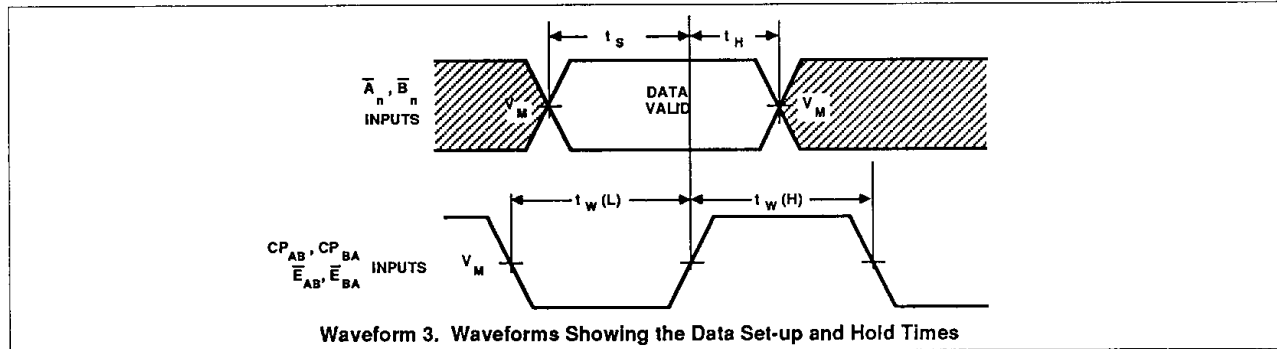
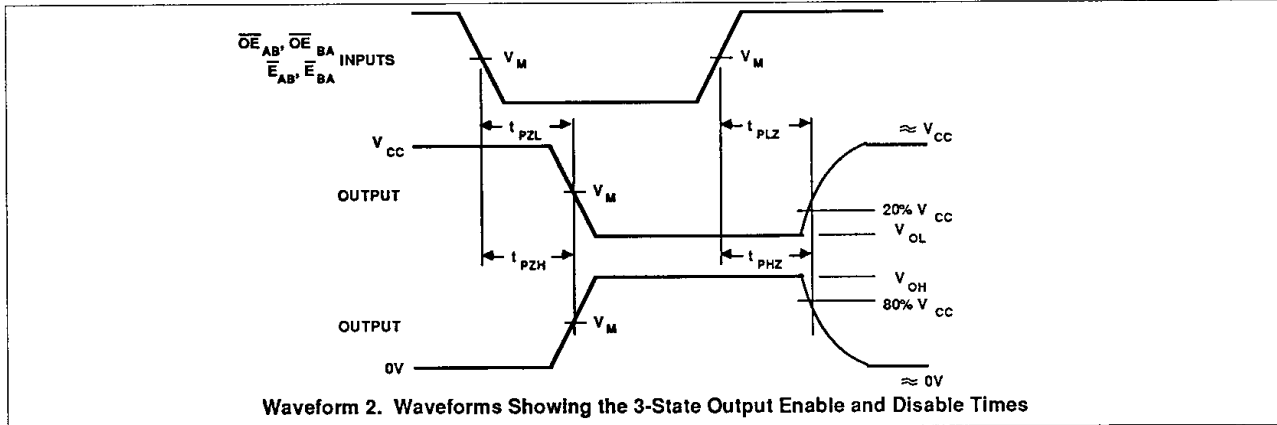
### AC WAVEFORMS



# Octal transceiver/register with dual enable, INV (3-State)

## 74AC/ACT11471

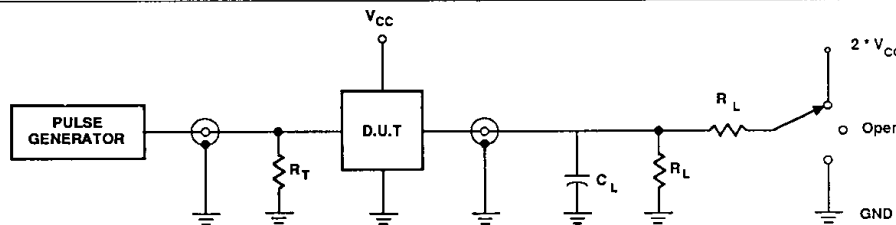
### AC WAVEFORMS (Continued)



### WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

### TEST CIRCUIT



Test Circuit

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \cdot V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

#### SWITCH POSITION

#### DEFINITIONS

$C_L$  = Load capacitance, 50pF; includes jig and probe capacitance  
 $R_L$  = Load resistor, 500Ω  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators  
 Input pulses:  $PRR \leq 10\text{MHz}$   
 $t_r = t_f = 3\text{ns}$