

Document No.	853-1491
ECN No.	00730
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11175

Quad D-type flip-flop with reset, positive-edge trigger

FEATURES

- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11175 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11175 provides four D-type flip-flops with independent Data inputs, shared Clock and Master Reset inputs, and complementary Q and \bar{Q} outputs.

Master Reset (\overline{MR}) is an asynchronous active-Low input and operates independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering is threshold voltage dependent. The

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n or \bar{Q}_n	$C_L = 50\text{pF}$	5.5	6.3	ns
C_{PD}	Power dissipation capacitance per flip-flop ¹	$f = 1\text{MHz}; C_L = 50\text{pF}$	47	42	pF
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	$C_L = 50\text{pF}$	150	130	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

f_O = output frequency in MHz, V_{CC} = supply voltage in V,

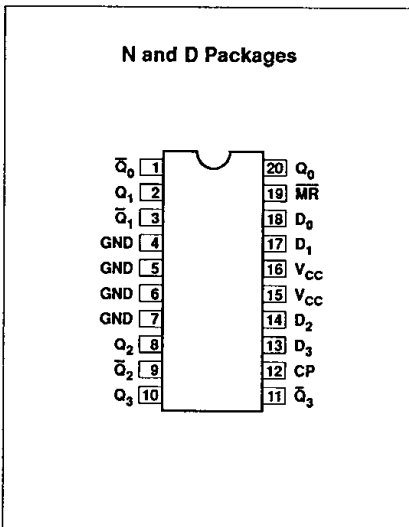
$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

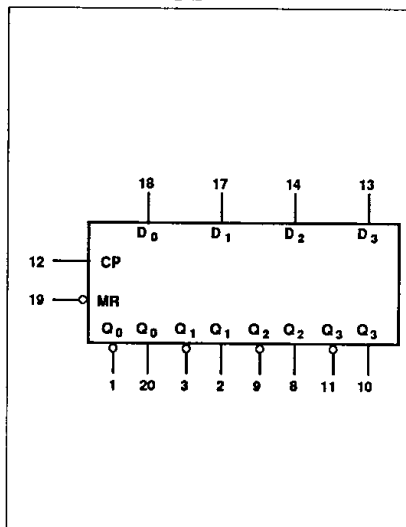
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11175N 74ACT11175N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11175D 74ACT11175D

D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

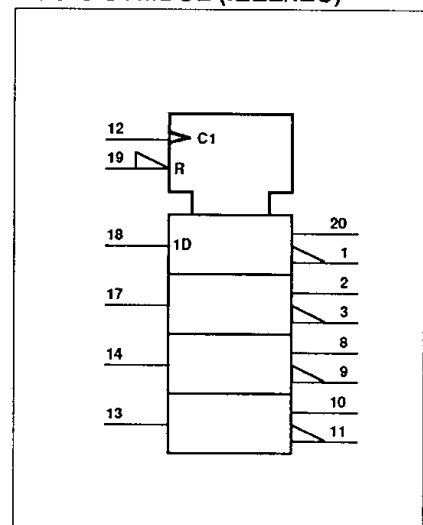
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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PIN DESCRIPTION

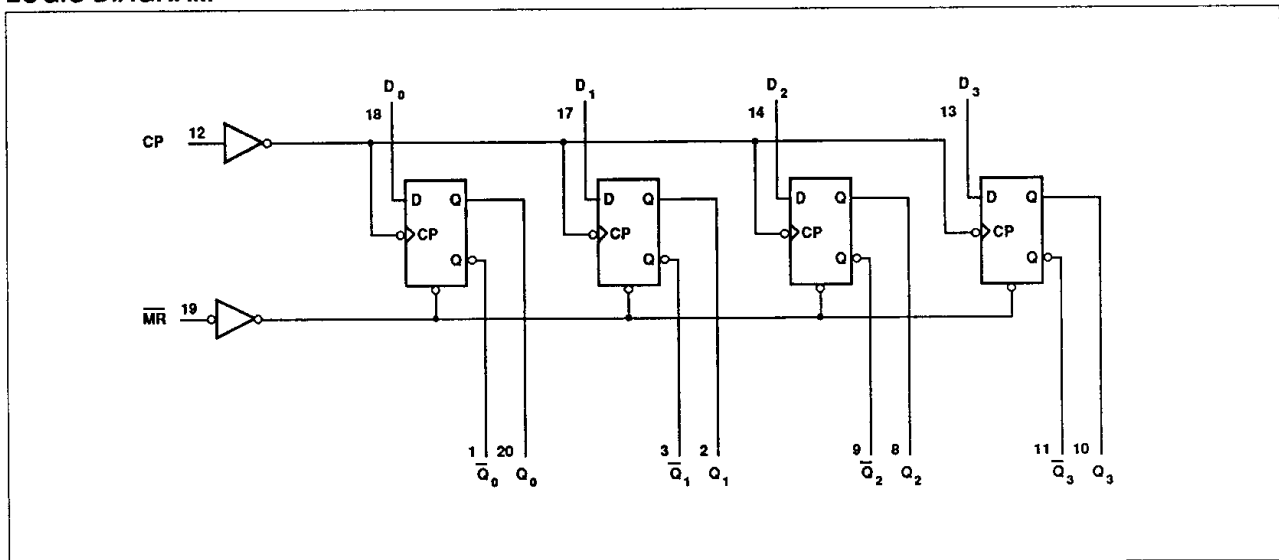
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	$D_0 - D_3$	Data inputs
20, 2, 8, 10	$Q_0 - Q_3$	Data outputs
1, 3, 9, 11	$\bar{Q}_0 - \bar{Q}_3$	Data outputs (complements of Q_n outputs)
19	\overline{MR}	Master reset input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	\overline{MR}	CP	D_n	Q_n	\bar{Q}_n
Asynchronous reset	L	X	X	L	H
Load "1" (set)	H	↑	h	H	L
Load "0" (reset)	H	↑	l	L	H

H = High voltage level steady state
 h = High voltage level one set-up time prior to the Low-to-High clock transition
 L = Low voltage level steady state
 l = Low voltage level one set-up time prior to the Low-to-High clock transition
 X = Don't care
 ↑ = Low-to-High clock transition

LOGIC DIAGRAM



Quad D-type flip-flop with reset, positive-edge trigger

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11175			74ACT11175			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:

- No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} V	74AC11175				74ACT11175				UNIT	
				T _{amb} = +25°C		T _{amb} = -40°C to +85°C		T _{amb} = +25°C		T _{amb} = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
I _{OH} = -75mA ¹	5.5			3.85				3.85					
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I _{OL} = 75mA ¹	5.5				1.65				1.65				
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V $\pm 0.3V$

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			$T_{amb} = +25^{\circ}C$			$T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n , \bar{Q}_n	1	2.4 1.7	6.8 9.4	8.7 11.7	2.4 1.7	9.4 12.5	ns
t_{PLH} t_{PHL}	Propagation delay \overline{MR} to Q_n , \bar{Q}_n	2	2.6 2.5	7.0 10.0	8.7 11.6	2.6 2.5	9.3 12.4	ns
t_S	Setup time, High or Low D_n to CP	1	8.0			8.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	5.5			5.5		ns
t_W	\overline{MR} pulse width Low	2	3.5			3.5		ns
t_{REC}	Recovery time \overline{MR} to CP	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			$T_{amb} = +25^{\circ}C$			$T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n , \bar{Q}_n	1	2.2 1.9	4.5 6.4	6.3 8.5	2.2 1.8	6.9 9.3	ns
t_{PLH} t_{PHL}	Propagation delay \overline{MR} to Q_n , \bar{Q}_n	2	2.2 2.4	4.5 6.7	6.3 8.5	2.2 2.4	6.8 9.3	ns
t_S	Setup time, High or Low D_n to CP	1	5.5			5.5		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	\overline{MR} pulse width Low	2	2.5			2.5		ns
t_{REC}	Recovery time \overline{MR} to CP	3	1.0			1.0		ns

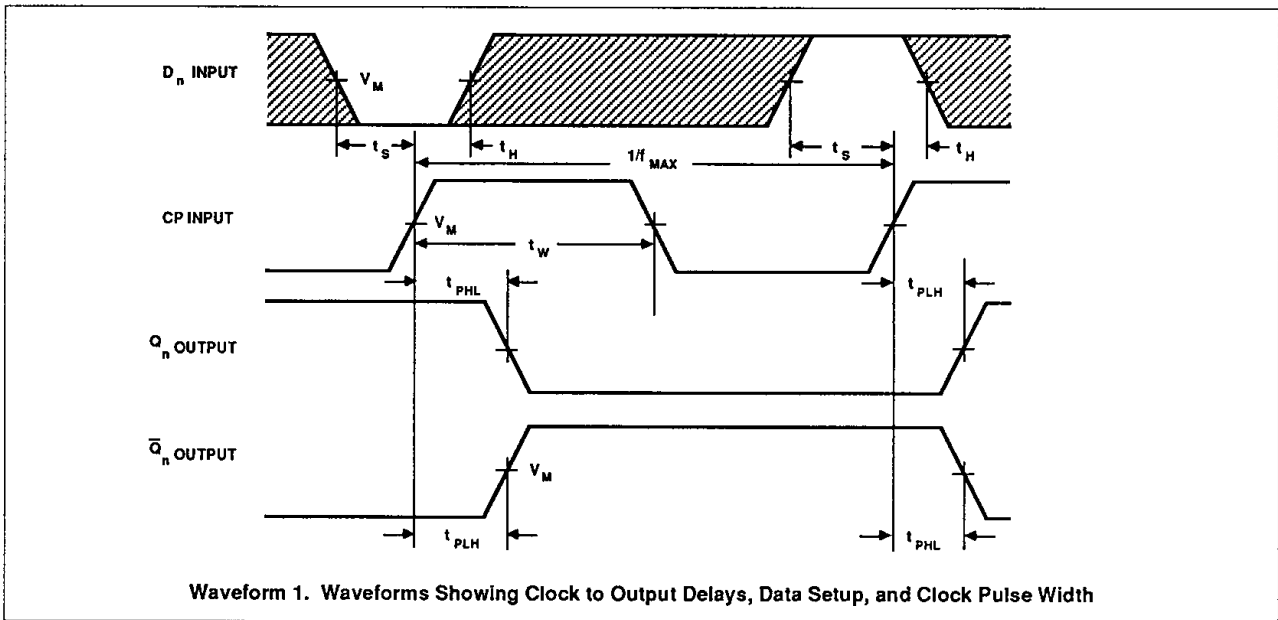
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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11175					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	100	130		100		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Q _n , \bar{Q}_n	1	3.0 3.3	5.3 7.2	6.9 9.2	3.0 3.3	7.5 10.1	ns
t _{PLH} t _{PHL}	Propagation delay MR to Q _n , \bar{Q}_n	2	2.5 3.1	5.4 7.6	7.4 9.9	2.5 3.1	8.1 10.9	ns
t _S	Setup time, High or Low D _n to CP	1	5.0			5.0		ns
t _H	Hold time, High or Low CP to D _n	1	0.5			0.5		ns
t _W	Clock pulse width High or Low	1	5.0			5.0		ns
t _W	\bar{MR} pulse width Low	2	4.0			4.0		ns
t _{REC}	Recovery time MR to CP	3	1.5			1.5		ns

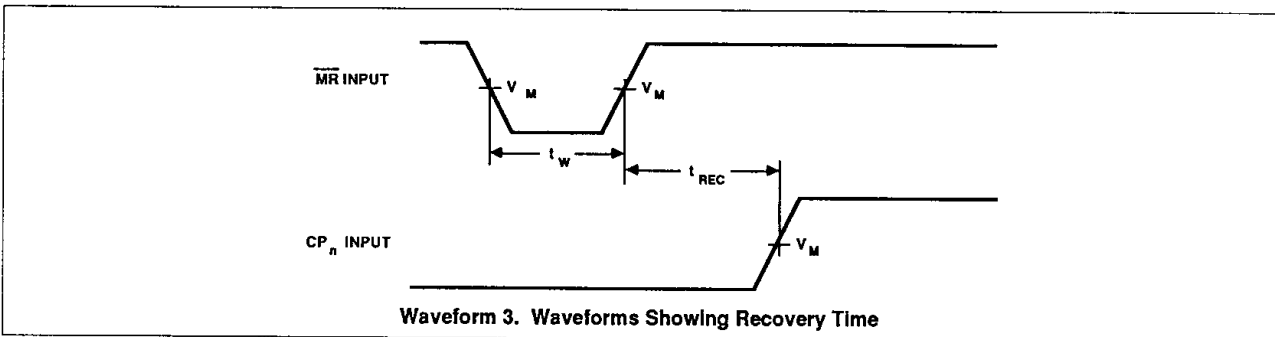
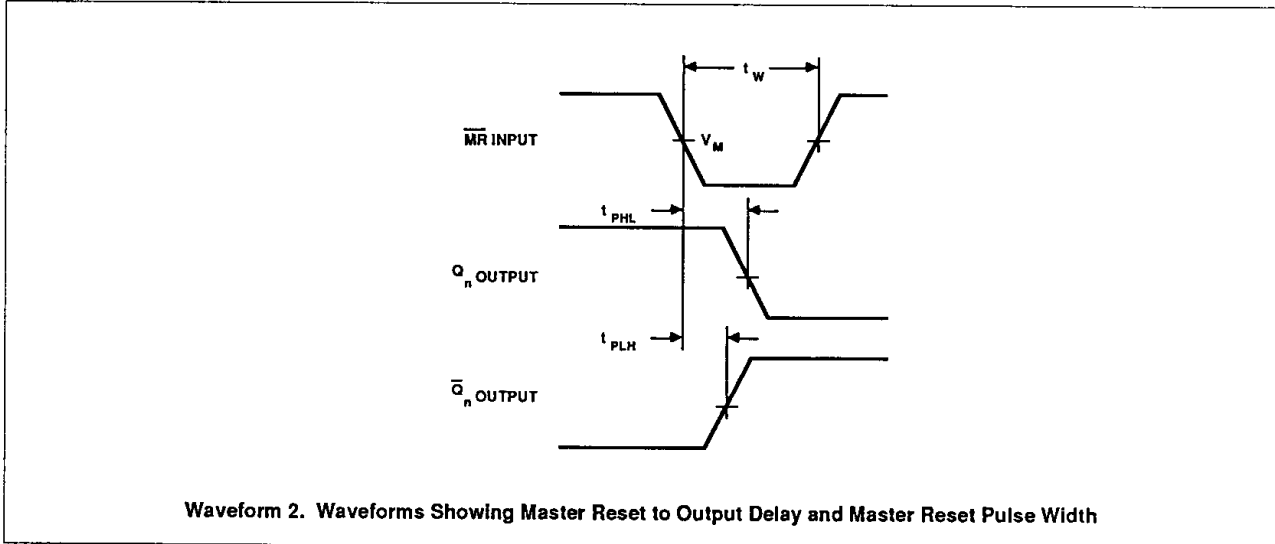
AC WAVEFORMS



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AC WAVEFORMS (Continued)



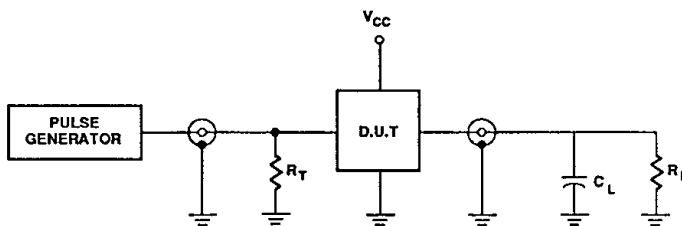
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC},$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V,$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

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TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$