

Document No.	853-1490
ECN No.	00730
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

# 74AC/ACT11174

## Hex D-type flip-flop with reset, positive-edge trigger

### FEATURES

- Output capability:  $\pm 24$  mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- $50\Omega$  incident wave switching
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: MSI

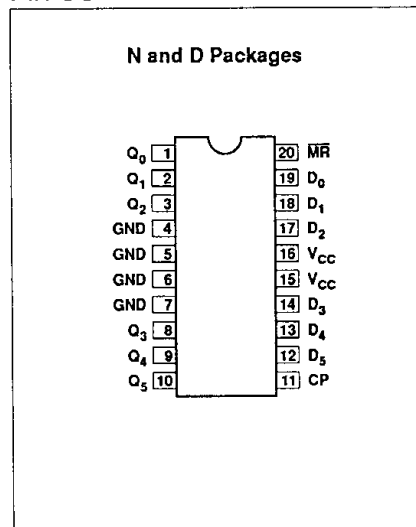
### DESCRIPTION

The 74AC/ACT11174 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11174 provides six D-type flip-flops with independent Data inputs, shared Clock and Master Reset inputs, and Q outputs.

Master Reset ( $\overline{MR}$ ) is an asynchronous active-Low input and operates independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering is threshold voltage dependent. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

### PIN CONFIGURATION



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$ ; GND = 0V $V_{CC} = 5.0V$	TYPICAL		UNIT
			AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay CP to $Q_n$	$C_L = 50pF$	5.6	6.5	ns
$C_{PD}$	Power dissipation capacitance per flip-flop <sup>1</sup>	$f = 1MHz$ ; $C_L = 50pF$	29	30	pF
$C_{IN}$	Input capacitance	$V_I = 0V$ or $V_{CC}$	4.0	4.0	pF
$I_{LATCH}$	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
$f_{MAX}$	Maximum clock frequency	$C_L = 50 pF$	125	135	MHz

#### Note:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

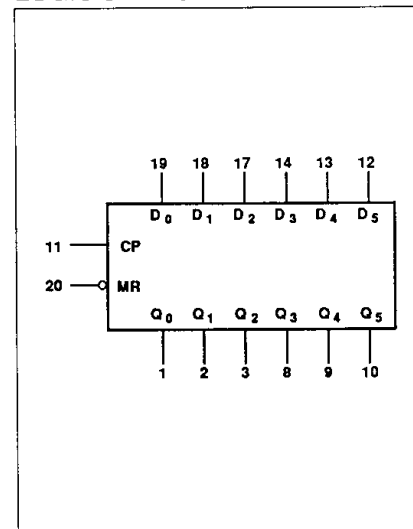
$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

$f_I$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,  
 $f_O$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,  
 $\sum (C_L \times V_{CC}^2 \times f_O)$  = sum of outputs

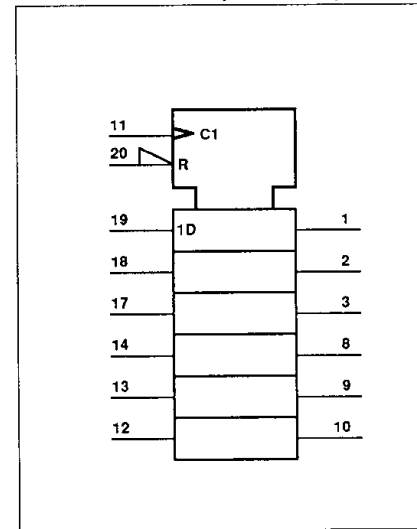
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11174N 74ACT11174N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11174D 74ACT11174D

### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



# Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

## PIN DESCRIPTION

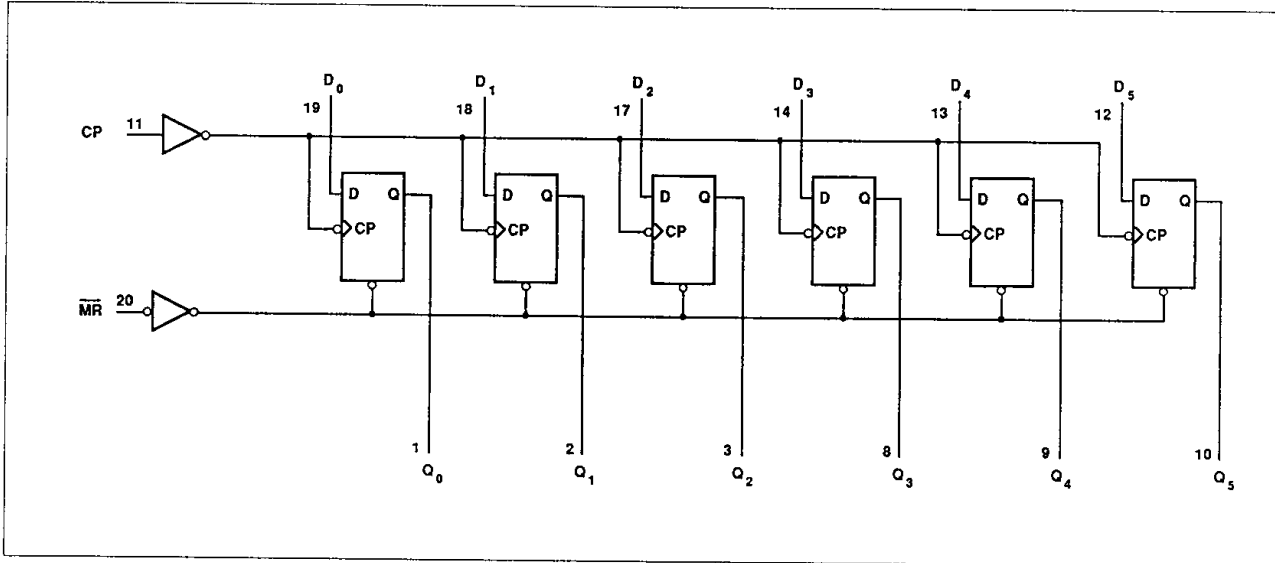
PIN NUMBER	SYMBOL	NAME AND FUNCTION
19, 18, 17, 14, 13, 12	D <sub>0</sub> - D <sub>5</sub>	Data inputs
1, 2, 3, 8, 9, 10	Q <sub>0</sub> - Q <sub>5</sub>	Data outputs
20	$\overline{MR}$	Master reset input (active Low)
11	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D <sub>n</sub>	Q <sub>n</sub>
Asynchronous reset	L	X	X	L
Load "1" (set)	H	↑	h	H
Load "0" (reset)	H	↑	l	L

H = High voltage level steady state  
 h = High voltage level one set-up time prior to the Low-to-High clock transition  
 L = Low voltage level steady state  
 l = Low voltage level one set-up time prior to the Low-to-High clock transition  
 X = Don't care  
 ↑ = Low-to-High clock transition

## LOGIC DIAGRAM



# Hex D-type flip-flop with reset, positive-edge trigger

## 74AC/ACT11174

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11174			74ACT11174			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta V/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40		+85	-40		+85	°C

#### NOTE:

- No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 TO +7.0	V
$I_{IK}$ or $V_I$	DC input diode current <sup>2</sup>	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_O$	DC output diode current <sup>2</sup>	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current per output pin	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		±150	mA
	DC ground current		±150	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

#### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Hex D-type flip-flop with reset,  
positive-edge trigger

74AC/ACT11174

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> V	74AC11174				74ACT11174				UNIT	
				T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C		T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
I <sub>OH</sub> = -75mA <sup>1</sup>	5.5			3.85				3.85					
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I <sub>OL</sub> = 75mA <sup>1</sup>	5.5				1.65				1.65				
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA	

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

## Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

### AC ELECTRICAL CHARACTERISTICS AT 3.3V $\pm$ 0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11174					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	80	105		80		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	2.4 3.4	7.5 9.6	9.2 12.7	2.4 3.4	10.6 14.0	ns
t <sub>PHL</sub>	Propagation delay MR to Q <sub>n</sub>	2	3.9	10.0	13.5	3.9	14.8	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> to CP	1	7.0			7.0		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub>	1	0.0			0.0		ns
t <sub>W</sub>	Clock pulse width High or Low	1	6.0			6.0		ns
t <sub>W</sub>	MR pulse width Low	2	4.5			4.5		ns
t <sub>REC</sub>	Recovery time MR to CP	3	1.5			1.5		ns

### AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm$ 0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11174					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	100	125		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	2.1 2.7	4.9 6.2	6.8 9.2	2.1 2.7	7.6 10.1	ns
t <sub>PHL</sub>	Propagation delay MR to Q <sub>n</sub>	2	2.9	6.5	9.8	2.9	10.7	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> to CP	1	4.5			4.5		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub>	1	0.0			0.0		ns
t <sub>W</sub>	Clock pulse width High or Low	1	5.0			5.0		ns
t <sub>W</sub>	MR pulse width Low	2	4.0			4.0		ns
t <sub>REC</sub>	Recovery time MR to CP	3	1.5			1.5		ns

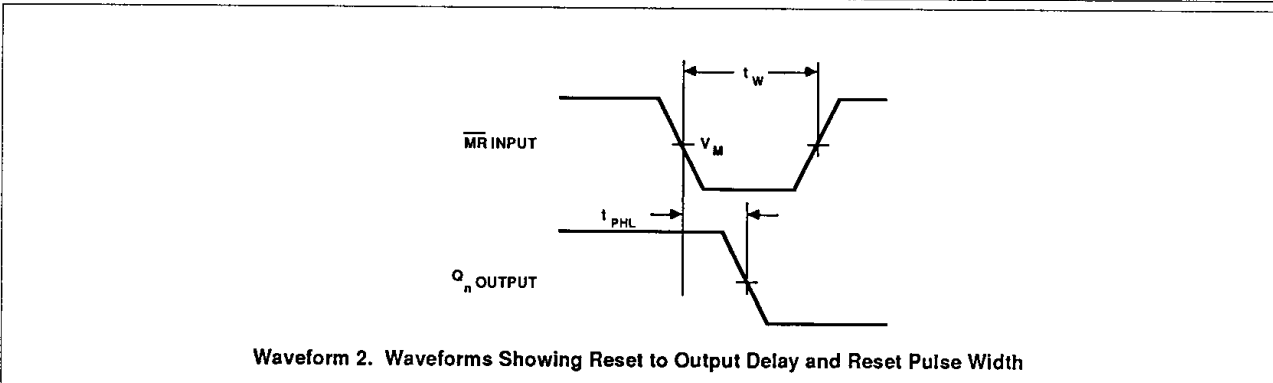
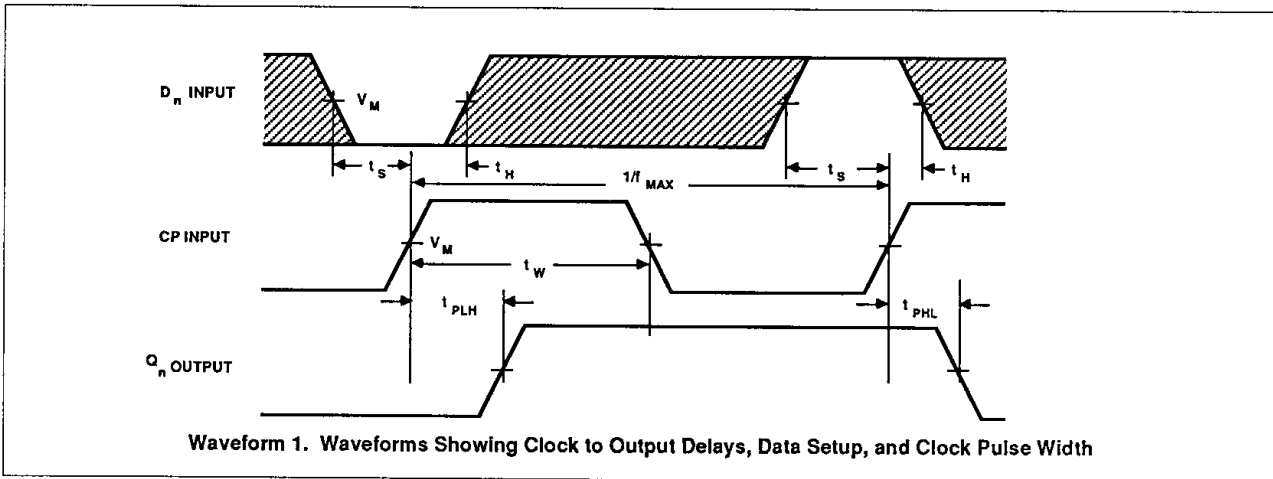
# Hex D-type flip-flop with reset, positive-edge trigger

## 74AC/ACT11174

### AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11174					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	110	135		110		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	3.1 3.7	5.8 7.2	7.9 9.9	3.1 3.7	8.7 11.0	ns
t <sub>PHL</sub>	Propagation delay $\overline{MR}$ to Q <sub>n</sub>	2	3.4	7.5	11.4	3.4	12.6	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> to CP	1	4.0			4.0		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub>	1	0.5			0.5		ns
t <sub>W</sub>	Clock pulse width High or Low	1	4.5			4.5		ns
t <sub>W</sub>	$\overline{MR}$ pulse width Low	2	4.0			4.0		ns
t <sub>REC</sub>	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

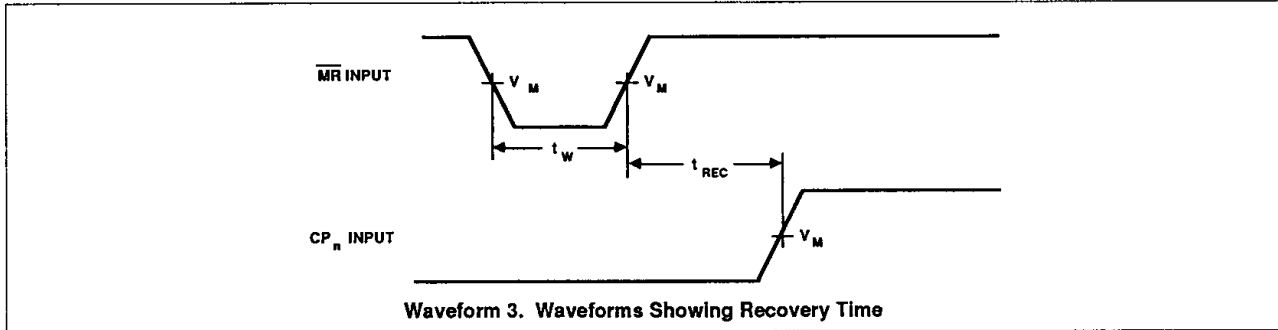
### AC WAVEFORMS



# Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

## AC WAVEFORMS (Continued)



## WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

## TEST CIRCUIT

