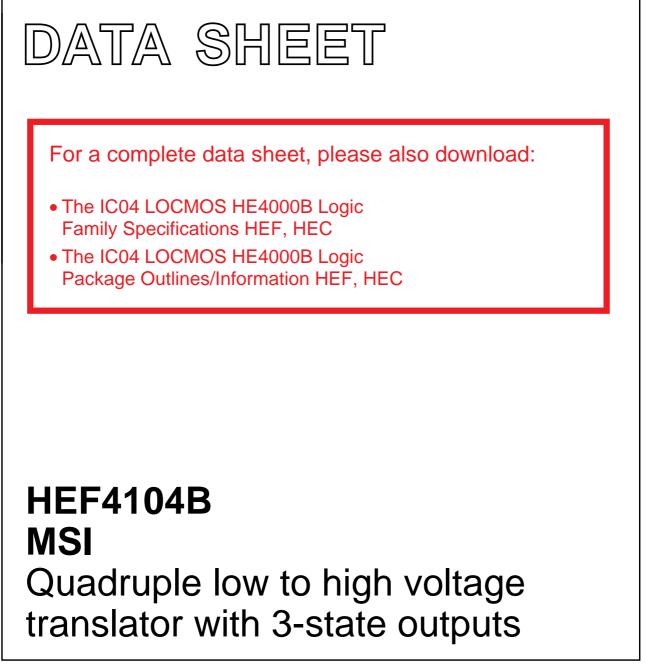
## INTEGRATED CIRCUITS



Product specification File under Integrated Circuits, IC04 January 1995



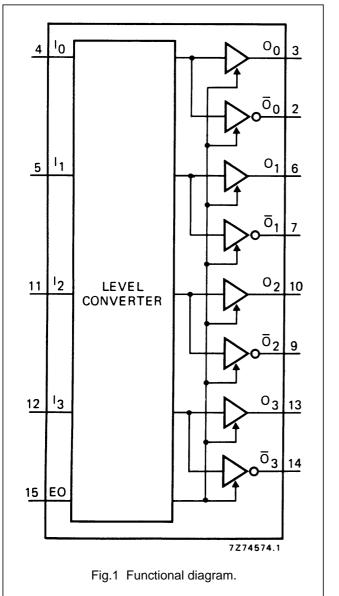
#### DESCRIPTION

The HEF4104B quadruple low voltage to high voltage translator with 3-state outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage LOCMOS and TTL to high voltage LOCMOS. It has four data inputs ( $I_0$  to  $I_3$ ), an active HIGH output enable input (EO), four data outputs ( $O_0$  to  $O_3$ ) and their complements ( $\overline{O}_0$  to  $\overline{O}_3$ ).

With EO HIGH,  $O_0$  to  $O_3$  and  $\overline{O}_0$  to  $\overline{O}_3$  are in the low impedance ON-state, either HIGH or LOW as determined by  $I_0$  to  $I_3$ ; with EO LOW,  $O_0$  to  $O_3$  and  $\overline{O}_0$  to  $\overline{O}_3$  are in the high impedance OFF-state.

The device uses a common negative supply (V<sub>SS</sub>) and separate positive supplies for inputs (V<sub>DDI</sub>) and outputs (V<sub>DD0</sub>). V<sub>DDI</sub> must always be less than or equal to V<sub>DD0</sub>, even during power turn-on and turn-off. For the permissible operating range of V<sub>DDI</sub> and V<sub>DD0</sub> see graph Fig.4.

Each input protection circuit is terminated between  $V_{DDO}$  and  $V_{SS}$ . This allows the input signals to be driven from any potential between  $V_{DDO}$  and  $V_{SS}$ , without regard to current limiting. When driving from potentials greater than  $V_{DDO}$  or less than  $V_{SS}$ , the current at each input must be limited to 10 mA.



13 12 11 16 10 9 ō3 ΕO 03  $\overline{0}_{2}$ 13 12 וחס 0, HEF 4104B Õ1 DDO 00 00 11 VSS 10  $0_1$ 2 4 5 6 3 8 7Z73709.1 Fig.2 Pinning diagram.

HEF4104BP(N):	16-lead DIL; plastic				
	(SOT38-1)				
HEF4104BD(F):	16-lead DIL; ceramic (cerdip)				
	(SOT74)				
HEF4104BT(D):	16-lead SO; plastic				
	(SOT109-1)				
(), Deckage Decignator North America					

(): Package Designator North America

#### PINNING

$I_0$ to $I_3$	data inputs
EO	output enable input
$O_0$ to $O_3$	data outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary data outputs

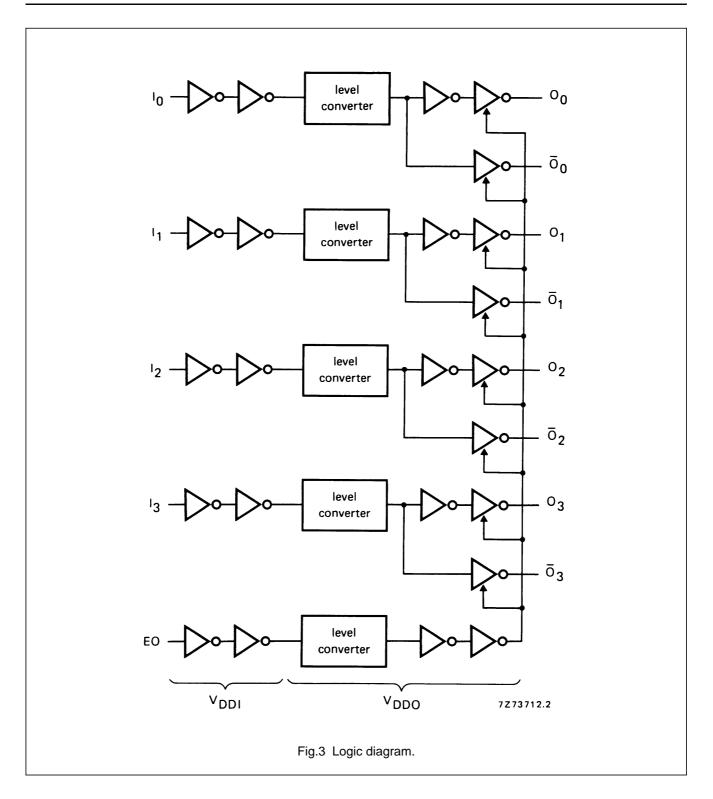
#### FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

### Product specification HEF4104B

MSI

### HEF4104B MSI



#### Product specification

### HEF4104B MSI

#### AC CHARACTERISTICS

 $V_{SS}$  = 0 V;  $T_{amb}$  = 25 °C;  $C_L$  = 50 pF; input transition times  $\leq$  20 ns

	V <sub>DD</sub> V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \rightarrow O_n,  \overline{O}_n$	5		170	340	ns	143 ns + (0,55 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>PHL</sub>	80	160	ns	69 ns + (0,23 ns/pF) C <sub>L</sub>
	15		65	135	ns	57 ns + (0,16 ns/pF) C <sub>L</sub>
	5		170	340	ns	143 ns + (0,55 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>PLH</sub>	80	160	ns	69 ns + (0,23 ns/pF) C <sub>L</sub>
	15		70	140	ns	62 ns + (0,16 ns/pF) C <sub>L</sub>
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>THL</sub>	30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>
	15		20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>
	5		60	120	ns	10 ns + (1,0 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>TLH</sub>	30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>
	15		20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>
3-state propagation						
delays						
Output disable times						
$EO\toO_n,\overline{O}_n$	5		70	135	ns	
HIGH	10	t <sub>PHZ</sub>	55	110	ns	
	15		60	120	ns	
	5		70	135	ns	
LOW	10	t <sub>PLZ</sub>	55	105	ns	
	15		55	110	ns	
Output enable times						
$EO \rightarrow O_n, \overline{O}_n$	5		195	395	ns	
HIGH	10	t <sub>PZH</sub>	95	195	ns	
	15		80	165	ns	
	5		195	395	ns	
LOW	10	t <sub>PZL</sub>	95	190	ns	
	15		80	160	ns	

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power	5	$3~000~f_i + \Sigma~(f_o C_L) \times V_{DD}{}^2$	where
dissipation per	10	12 200 f <sub>i</sub> + $\Sigma$ (f <sub>o</sub> C <sub>L</sub> ) $ imes$ V <sub>DD</sub> <sup>2</sup>	f <sub>i</sub> = input freq. (MHz)
package (P)	15	31 000 f <sub>i</sub> + $\Sigma$ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	f <sub>o</sub> = output freq. (MHz)
			$C_L$ = load capacitance (pF)
			$\Sigma$ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs
			V <sub>DD</sub> = supply voltage (V)

### HEF4104B MSI

