DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4049B
buffers
HEX inverting buffers

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

DESCRIPTION

The HEF4049B provides six inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table below.

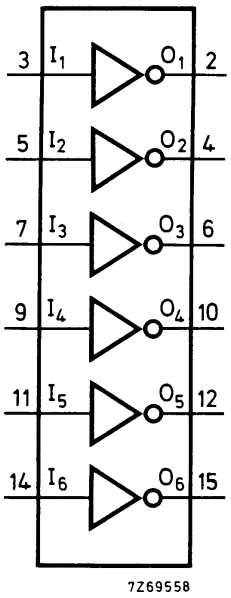

Fig.1 Functional diagram.

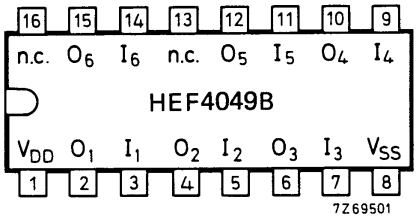

Fig.2 Pinning diagram.

HEF4049BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4049BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4049BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

Guaranteed fan-out in common logic families

DRIVEN ELEMENT	GUARANTEED FAN-OUT
standard TTL	2
74 LS	9
74 L	16

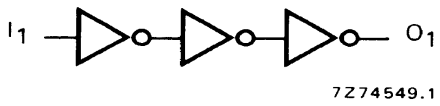

Fig.3 Logic diagram (one gate).

APPLICATION INFORMATION

Some examples of applications for the HEF4049B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

Input protection

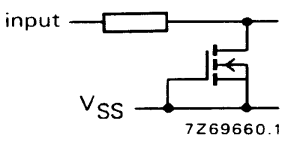

Fig.4 Input protection circuit that allows input voltages in excess of V_{DD}.

FAMILY DATA, I_{DD} LIMITS category BUFFERS

See Family Specifications

DC CHARACTERISTICS

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}

HEF	V_{DD} V	V_O V	SYMBOL	T_{amb} (°C)						
				−40		+25		+85		
				MIN.	MAX.	MIN.	MAX.	MN.	MAX.	
Output (sink)	4,75	0,4		3,5	–	2,9	–	2,3	–	mA
current LOW	10	0,5	I_{OL}	12,0	–	10,0	–	8,0	–	mA
	15	1,5		24,0	–	20,0	–	16,0	–	mA
Output (source)	5	4,6		0,52	–	0,44	–	0,36	–	mA
current HIGH	10	9,5	—I_{OH}	1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA
Output (source)										
current HIGH	5	2,5	—I_{OH}	1,7	–	1,4	–	1,1	–	mA

HEC	V_{DD} V	V_O V	SYMBOL	T_{amb} (°C)						
				−55		+25		+125		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (sink)	4,75	0,4		3,6	–	2,9	–	1,9	–	mA
current LOW	10	0,5	I_{OL}	12,5	–	10,0	–	6,7	–	mA
	15	1,5		25,0	–	20,0	–	13,0	–	mA
Output (source)	5	4,6		0,52	–	0,44	–	0,36	–	mA
current HIGH	10	9,5	—I_{OH}	1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays	5		35	70	ns	26 ns + (0,18 ns/pF) C_L
$I_n \rightarrow O_n$	10	t_{PHL}	15	30	ns	11 ns + (0,08 ns/pF) C_L
HIGH to LOW	15		12	25	ns	9 ns + (0,05 ns/pF) C_L
	5		50	100	ns	23 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition	5		20	40	ns	3 ns + (0,35 ns/pF) C_L
times	10	t_{THL}	10	20	ns	3 ns + (0,14 ns/pF) C_L
HIGH to LOW	15		7	14	ns	2 ns + (0,09 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$2\,500\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
	10	$11\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$35\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)