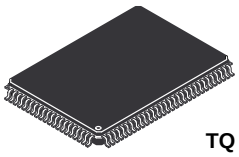
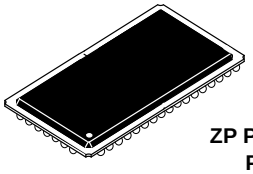
MCM63P736
MCM63P818

Product Preview

128K x 36 and 256K x 18 Bit Pipelined BurstRAM Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01



ZP PACKAGE
PBGA
CASE 999–01

The MCM63P736 and MCM63P818 are 4M bit synchronous fast static RAMs designed to provide a burstable, high performance, secondary cache for the PowerPC™ and other high performance microprocessors. The MCM63P736 is organized as 128K words of 36 bits each and the MCM63P818 is organized as 256K words of 18 bits each. These devices integrate input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K).

Addresses (SA), data inputs (DQx), and all control signals except output enable (G), sleep mode (ZZ), and linear burst order (LBO) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either ADSP or ADSC input pins. Subsequent burst addresses can be generated internally by the MCM63P736 and MCM63P818 (burst sequence operates in linear or interleaved mode dependent upon the state of LBO) and controlled by the burst address advance (ADV) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write (SBx), synchronous global write (SGW), and synchronous write enable (SW) are provided to allow writes to either individual bytes or to all bytes. The bytes are designated as “a”, “b”, etc. SBa controls DQa, SBb controls DQb, etc. Individual bytes are written if the selected byte writes SBx are asserted with SW. All bytes are written if either SGW is asserted or if all SBx and SW are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM63P736 and MCM63P818 operate from a 3.3 V core power supply and all outputs operate on a 2.5 V or 3.3 V power supply. All inputs and outputs are JEDEC standard JESD8–5 compatible.

- MCM63P736/MCM63P818–133 = 4 ns Access/7.5 ns Cycle (133 MHz)
  MCM63P736/MCM63P818–100 = 5 ns Access/10 ns Cycle (100 MHz)
  MCM63P736/MCM63P818–66 = 7 ns Access/15 ns Cycle (66 MHz)
- 3.3 V + 10%, – 5% Core Power Supply, 2.5 V or 3.3 V I/O Supply
- ADSP, ADSC, and ADV Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Two–Cycle Deselect Timing
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- Sleep Mode (ZZ)
- PB1 Version 2.0 Compatible
- JEDEC Standard 119–Pin PBGA and 100–Pin TQFP Packages

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10/8/97

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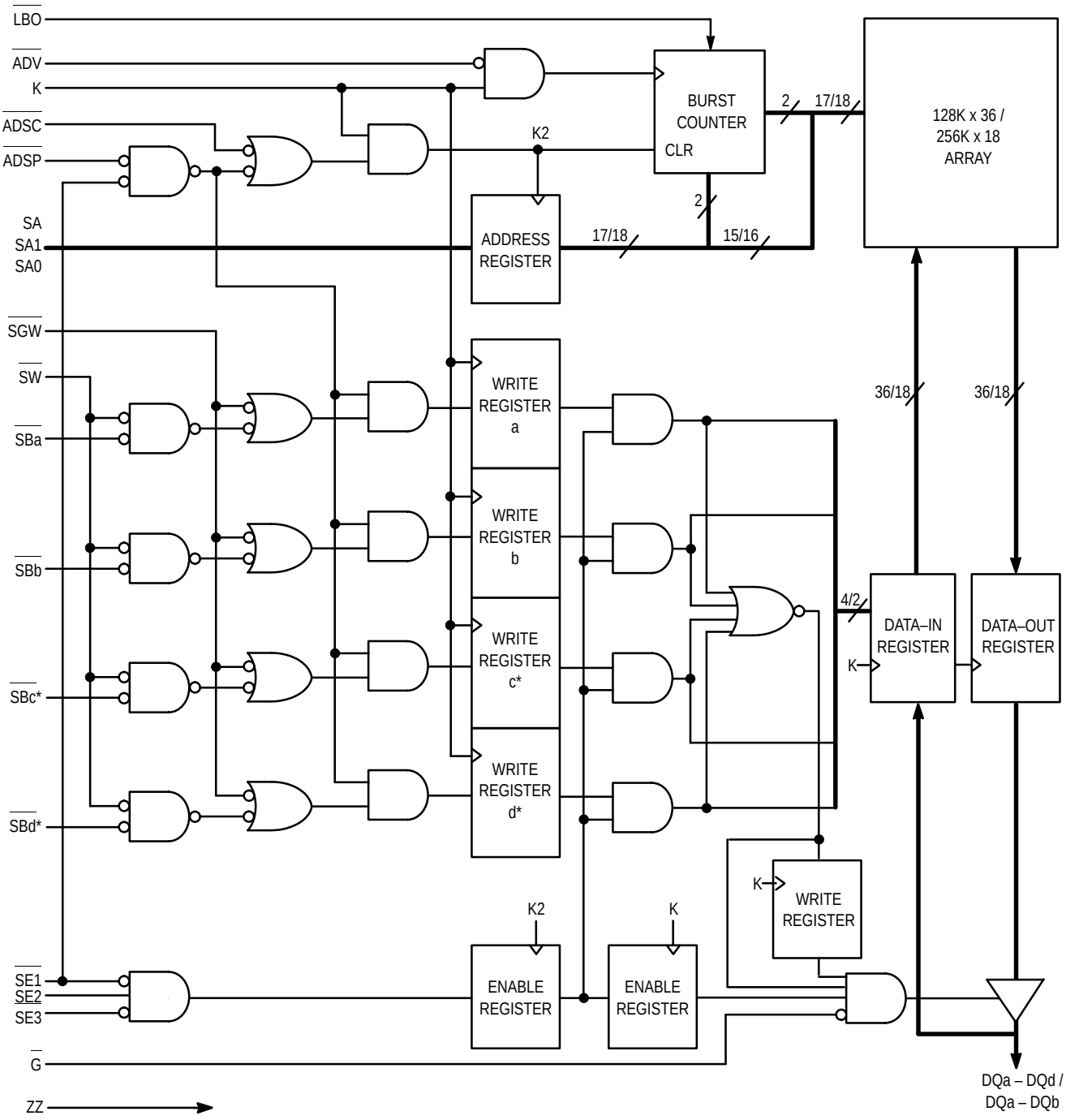
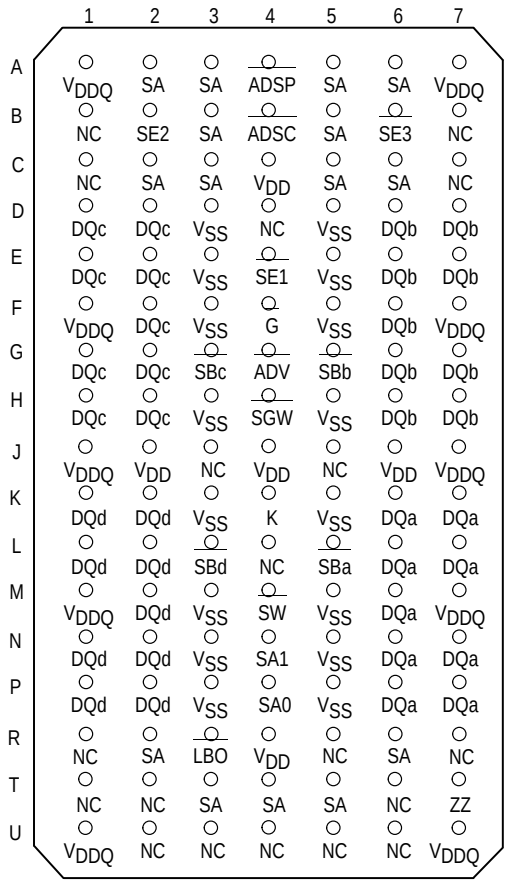
FUNCTIONAL BLOCK DIAGRAM

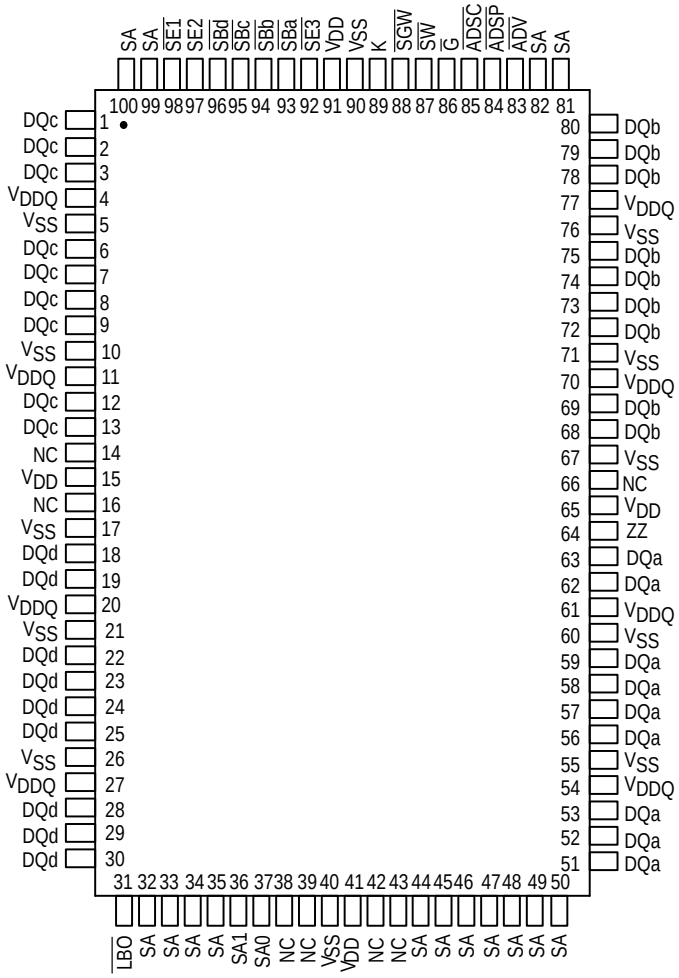


*Valid only for MCM63P736.

MCM63P736 PIN ASSIGNMENTS



TOP VIEW 119 BUMP PBGA



TOP VIEW 100 PIN TQFP

Not to Scale

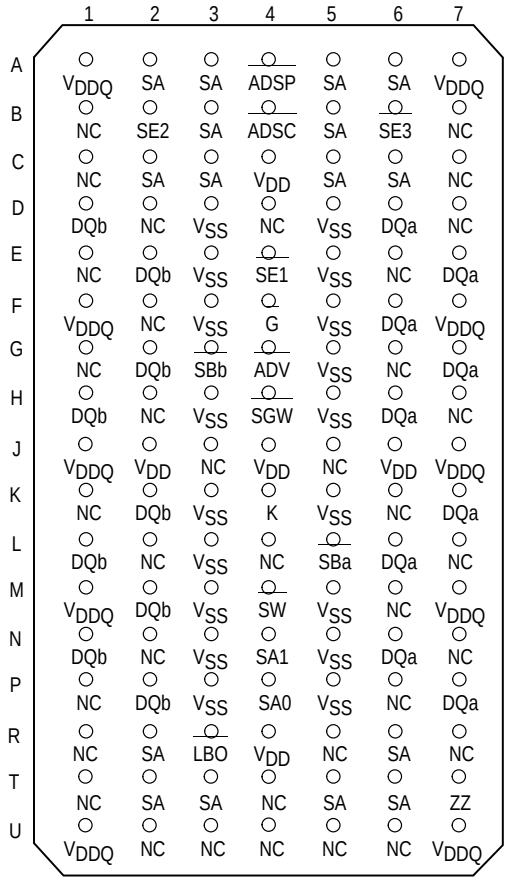
MCM63P736 PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	$\overline{\text{ADSC}}$	Input	Synchronous Address Status Controller: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a READ, WRITE, or chip deselect.
4A	ADSP	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when ADSP is asserted and SE1 is high).
4G	$\overline{\text{ADV}}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b, c, d).
4F	$\overline{\text{G}}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
4K	K	Input	Clock: This signal registers the address, data in, and all control signals except G, LBO, and ZZ.
3R	LBO	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
5L, 5G, 3G, 3L (a) (b) (c) (d)	SBx	Input	Synchronous Byte Write Inputs: “x” refers to the byte being written (byte a, b, c, d). SGW overrides SBx.
4E	SE1	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks $\overline{\text{ADSP}}$ or deselects chip when $\overline{\text{ADSC}}$ is asserted.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	$\overline{\text{SE3}}$	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	$\overline{\text{SGW}}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the SBx and SW signals. If only byte write signals SBx are being used, tie this pin high.
4M	$\overline{\text{SW}}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins. If only byte write signals SBx are being used, tie this pin low.
7T	ZZ	Input	Sleep Mode: This active high asynchronous signal places the RAM into the lowest power mode. The ZZ pin disables the RAMs internal clock when placed in this mode. When ZZ is negated, the RAM remains in low power mode until it is commanded to READ or WRITE. Data integrity is maintained upon returning to normal operation.
4C, 2J, 4J, 6J, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 5R, 7R, 1T, 2T, 6T, 2U, 3U, 4U, 5U, 6U	NC	—	No Connection: There is no connection to the chip.

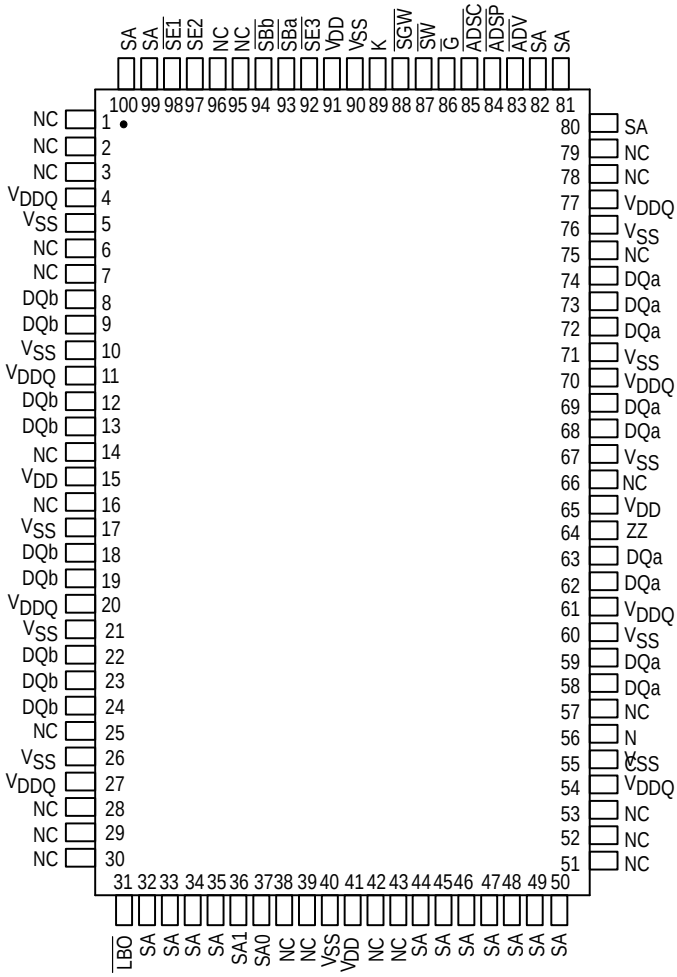
MCM63P736 TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{\text{ADSC}}$	Input	Synchronous Address Status Controller: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a READ, WRITE, or chip deselect.
84	ADSP	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when ADSP is asserted and SE1 is high).
83	$\overline{\text{ADV}}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b, c, d).
86	G	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except G, LBO, and ZZ.
31	LBO	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: these pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	SBx	Input	Synchronous Byte Write Inputs: “x” refers to the byte being written (byte a, b, c, d). SGW overrides SBx.
98	SE1	Input	Synchronous Chip Enable: Active low to enable chip. $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ Negated high — blocks ADSP or deselects chip when ADSC is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{\text{SE3}}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{\text{SGW}}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the SBx and SW signals. If only byte write signals SBx are being used, tie this pin high.
87	$\overline{\text{SW}}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins. If only byte write signals SBx are being used, tie this pin low.
64	ZZ	Input	Sleep Mode: This active high asynchronous signal places the RAM into the lowest power mode. The ZZ pin disables the RAMs internal clock when placed in this mode. When ZZ is negated, the RAM remains in low power mode until it is commanded to READ or WRITE. Data integrity is maintained upon returning to normal operation.
15, 41, 65, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
14, 16, 38, 39, 42, 43, 66	NC	—	No Connection: There is no connection to the chip.

MCM63P818 PIN ASSIGNMENTS



TOP VIEW 119 BUMP PBGA



TOP VIEW 100 PIN TQFP

Not to Scale

MCM63P818 PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	$\overline{\text{ADSC}}$	Input	Synchronous Address Status Controller: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a READ, WRITE, or chip deselect.
4A	$\overline{\text{ADSP}}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when ADSP is asserted and SE1 is high).
4G	$\overline{\text{ADV}}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b).
4F	$\overline{\text{G}}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
4K	K	Input	Clock: This signal registers the address, data in, and all control signals except G, LBO, and ZZ.
3R	$\overline{\text{LBO}}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
5L, 3G (a) (b)	SBx	Input	Synchronous Byte Write Inputs: “x” refers to the byte being written (byte a, b). SGW overrides SBx.
4E	SE1	Input	Synchronous Chip Enable: Active low to enable chip. $\overline{\text{SE1}}$ Negated high — blocks ADSP or deselects chip when ADSC is asserted.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	$\overline{\text{SE3}}$	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	$\overline{\text{SGW}}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the SBx and SW signals. If only byte write signals SBx are being used, tie this pin high.
4M	$\overline{\text{SW}}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins. If only byte write signals SBx are being used, tie this pin low.
7T	ZZ	Input	Sleep Mode: This active high asynchronous signal places the RAM into the lowest power mode. The ZZ pin disables the RAMs internal clock when placed in this mode. When ZZ is negated, the RAM remains in low power mode until it is commanded to READ or WRITE. Data integrity is maintained upon returning to normal operation.
4C, 2J, 4J, 6J, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 5R, 7R, 1T, 4T, 2U, 3U, 4U, 5U, 6U	NC	—	No Connection: There is no connection to the chip.

MCM63P818 TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a READ, WRITE, or chip deselect.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ or chip deselect (exception — chip deselect does not occur when ADSP is asserted and SE1 is high).
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: “x” refers to the byte being read or written (byte a, b).
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except G, LBO, and ZZ.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: “x” refers to the byte being written (byte a, b). SGW overrides SBx.
98	SE1	Input	Synchronous Chip Enable: Active low to enable chip. $\overline{}$ Negated high — blocks ADSP or deselects chip when ADSC is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the SBx and SW signals. If only byte write signals SBx are being used, tie this pin high.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins. If only byte write signals SBx are being used, tie this pin low.
64	ZZ	Input	Sleep Mode: This active high asynchronous signal places the RAM into the lowest power mode. The ZZ pin disables the RAMs internal clock when placed in this mode. When ZZ is negated, the RAM remains in low power mode until it is commanded to READ or WRITE. Data integrity is maintained upon returning to normal operation.
15, 41, 65, 91	V_{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground.
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 Through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	X[5]
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any SBx and SW low or 2) SGW is low.
3. G is an asynchronous signal and is not sampled by the clock K. G drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This read assumes the RAM was previously deselected.

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{G}$	I/O Status
Read	L	L	Data Out (DQx)
Read	L	H	High–Z
Write	L	X	High–Z
Deselected	L	X	High–Z
Sleep	H	X	High–Z

LINEAR BURST ADDRESS TABLE ($\overline{LBO}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO}$ = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$ (See Note 1)	$\overline{SBd}$ (See Note 1)
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c (See Note 1)	H	L	L	H	L	H
Write Byte d (See Note 1)	H	L	H	L	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

NOTE:
1. Valid only for MCM63P736.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit	Notes
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to + 4.6	V	
I/O Supply Voltage	V_{DDQ}	V_{SS} – 0.5 to V_{DD}	V	2
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	V_{SS} – 0.5 to V_{DD} + 0.5	V	2
Input Voltage (Three–State I/O)	V_{IT}	V_{SS} – 0.5 to V_{DDQ} + 0.5	V	2
Output Current (per I/O)	I_{out}	± 20	mA	
Package Power Dissipation	P_D	1.6	W	3
Ambient Temperature	T_A	0 to 70	°C	
Die Temperature	T_J	110	°C	3
Temperature Under Bias	T_{bias}	– 10 to 85	°C	
Storage Temperature	T_{stg}	– 55 to 125	°C	

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	38 22	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS: 2.5 V I/O SUPPLY (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
I/O Supply Voltage	V_{DDQ}	2.375	2.5	2.9	V
Input Low Voltage	V_{IL}	– 0.3	—	0.7	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input High Voltage I/O Pins	V_{IH2}	1.7	—	V_{DDQ} + 0.3	V

RECOMMENDED OPERATING CONDITIONS: 3.3 V I/O SUPPLY (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
I/O Supply Voltage	V_{DDQ}	3.135	3.3	V_{DD}	V
Input Low Voltage	V_{IL}	– 0.5	—	0.8	V
Input High Voltage	V_{IH}	2	—	V_{DD} + 0.5	V
Input High Voltage I/O Pins	V_{IH2}	2	—	V_{DDQ} + 0.5	V

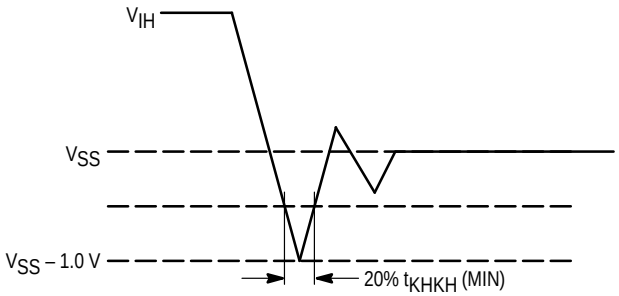


Figure 1. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})		$I_{lkg(I)}$	—	—	± 1	µA	1
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DDQ})		$I_{lkg(O)}$	—	—	± 1	µA	
AC Supply Current (Device Selected, All Outputs Open, Freq = Max) Includes V_{DD} and V_{DDQ}	MCM63P736/818–133 MCM63P736/818–100 MCM63P736/818–66	I_{DDA}	—	—	TBD	mA	2, 3, 4
CMOS Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, V_{DDQ} = Max, All Inputs Static at CMOS Levels)		I_{SB2}	—	—	TBD	mA	5, 6
Sleep Mode Standby Current (Device Deselected, Freq = Max, V_{DD} = Max, V_{DDQ} = Max, All Other Inputs Static at CMOS Levels, ZZ ≥ V_{DD} – 0.2 V.		I_{ZZ}	—	—	2	mA	1, 5, 6
TTL Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, V_{DDQ} = Max, All Inputs Static at TTL Levels)		I_{SB3}	—	—	TBD	mA	5, 7
Clock Running (Device Deselected, Freq = Max, V_{DD} = Max, V_{DDQ} = Max, All Inputs Toggling at CMOS Levels)	MCM63P736/818–133 MCM63P736/818–100 MCM63P736/818–66	I_{SB4}	—	—	TBD	mA	5, 6
Static Clock Running (Device Deselected, Freq = Max,V_{DD} = Max, V_{DDQ} = Max, All Inputs Static at TTL Levels)	MCM63P736/818–166 MCM63P736/818–150 MCM63P736/818–133	I_{SB5}	—	—	TBD	mA	5, 6
Output Low Voltage (I_{OL} = 2 mA) V_{DDQ} = 2.5 V		V_{OL}	—	—	0.7	V	
Output High Voltage (I_{OL} = – 2 mA) V_{DDQ} = 2.5 V		V_{OH}	1.7	—	—	V	
Output Low Voltage (I_{OL} = 8 mA) V_{DDQ} = 3.3 V		V_{OL2}	—	—	0.4	V	
Output High Voltage (I_{OL} = – 4 mA) V_{DDQ} = 3.3 V		V_{OH2}	2.4	—	—	V	

NOTES:

1. LBO and ZZ pins have an internal pullup and will exhibit leakage currents of ± 5 µA.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. All addresses transition simultaneously low (LSB) then high (MSB).
4. Data states are all zero.
5. Device is deselected as defined by the Truth Table.
6. CMOS levels for I/O's are V_{IT} ≤ V_{SS} + 0.2 V or ≥ V_{DDQ} – 0.2 V. CMOS levels for other inputs are V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V.
7. TTL levels for I/O's are V_{IT} ≤ V_{IL} or ≥ V_{IH2}. TTL levels for other inputs are V_{in} ≤ V_{IL} or ≥ V_{IH}.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.25 V
Input Pulse Levels . . . . . 0 to 2.5 V
Input Rise/Fall Time . . . . . 1.0 V/ns (20 to 80%)

Output Timing Reference Level . . . . . 1.25 V
Output Load . . . . . See Figure 2 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM63P736–133 MCM63P818–133		MCM63P736–100 MCM63P818–100		MCM63P737–66 MCM63P819–66		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	7.5	—	10	—	15	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	4	—	6	—	ns	3
Clock Low Pulse Width	t_{KLKH}	3	—	4	—	6	—	ns	3
Clock Access Time	t_{KHQV}	—	4	—	5	—	7	ns	
Output Enable to Output Valid	t_{GLQV}	—	3.8	—	4	—	6	ns	
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4, 5
Clock High to Output Change	t_{KHQX2}	1.5	—	1.5	—	1.5	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5
Output Disable to Q High–Z	t_{GHQZ}	—	3.8	—	4	—	6	ns	4, 5
Clock High to Q High–Z	t_{KHQZ}	1.5	7.5	1.5	10	1.5	15	ns	4, 5
Setup Times: Address ADSP, ADSC, ADV Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2	—	2	—	2	—	ns	
Hold Times: Address ADSP, ADSC, ADV Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at $V_{DDQ}/2$. In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC Test Conditions section of the data sheet as 1 V/ns, one can easily interpolate timing values to other reference levels.
4. This parameter is sampled and not 100% tested.
5. Measured at ± 200 mV from steady state.

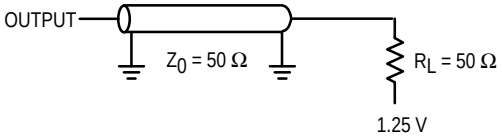


Figure 2. AC Test Load

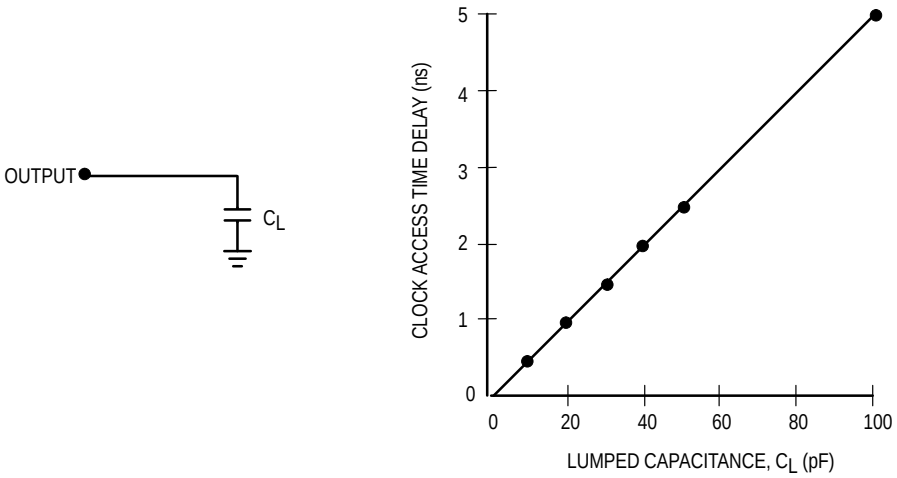
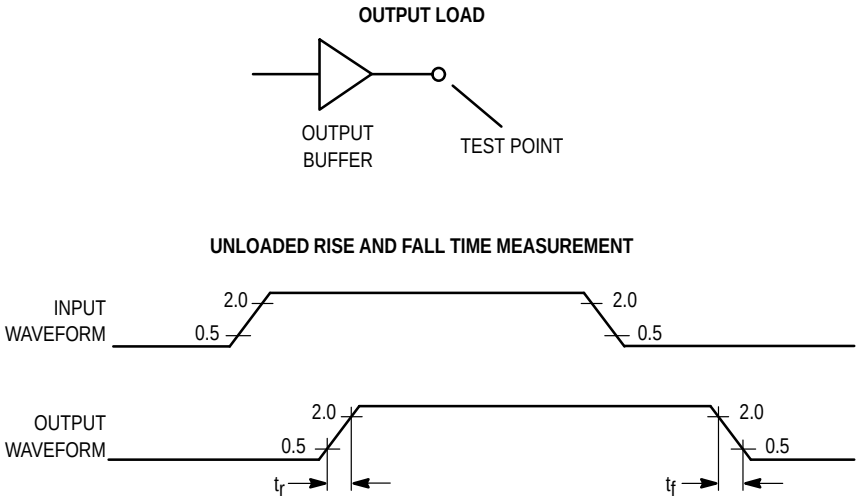


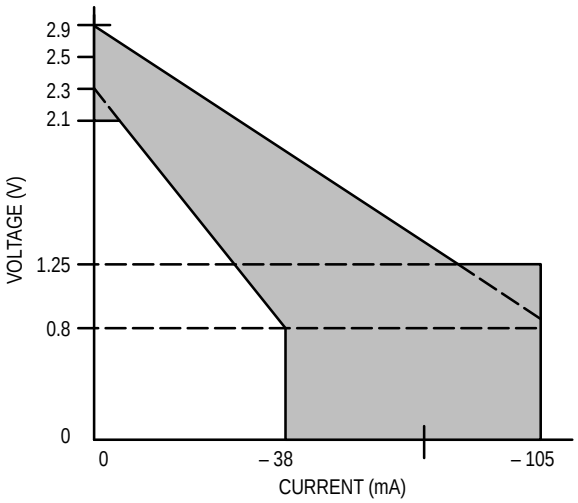
Figure 3. Lumped Capacitive Load and Typical Derating Curve



NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.5 to 2.0 V unloaded.
3. Fall time is measured from 2.0 to 0.5 V unloaded.

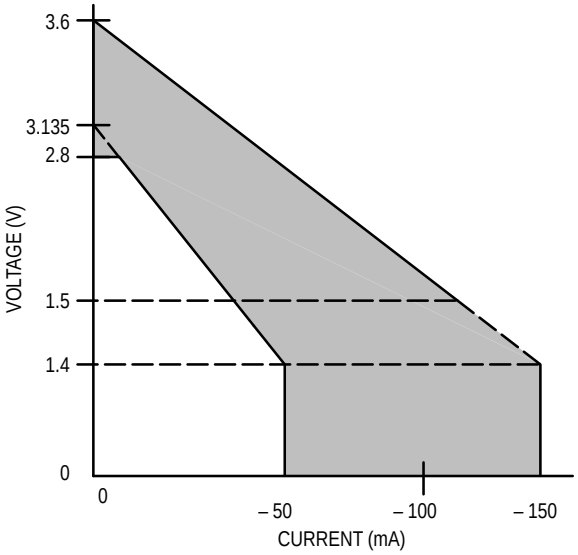
Figure 4. Unloaded Rise and Fall Time Characterization

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	– 38	– 105
0	– 38	– 105
0.8	– 38	– 105
1.25	– 26	– 83
1.5	– 20	– 70
2.3	0	– 30
2.7	0	– 10
2.9	0	0



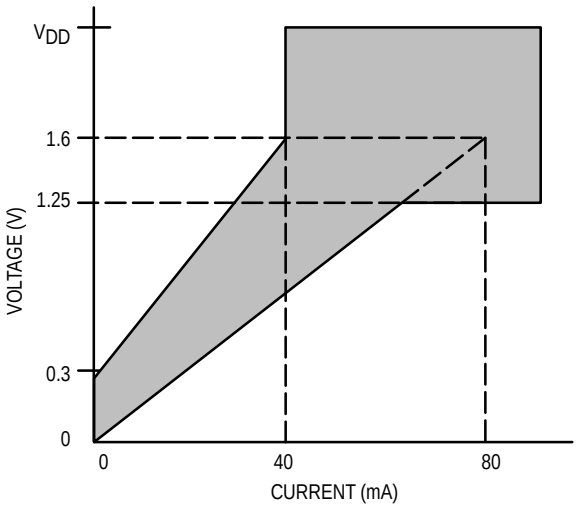
(a) Pull–Up for 2.5 V I/O Supply

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	– 50	– 150
0	– 50	– 150
1.4	– 50	– 150
1.65	– 46	– 130
2.0	– 35	– 101
3.135	0	– 25
3.6	0	0



(b) Pull–Up for 3.3 V I/O Supply

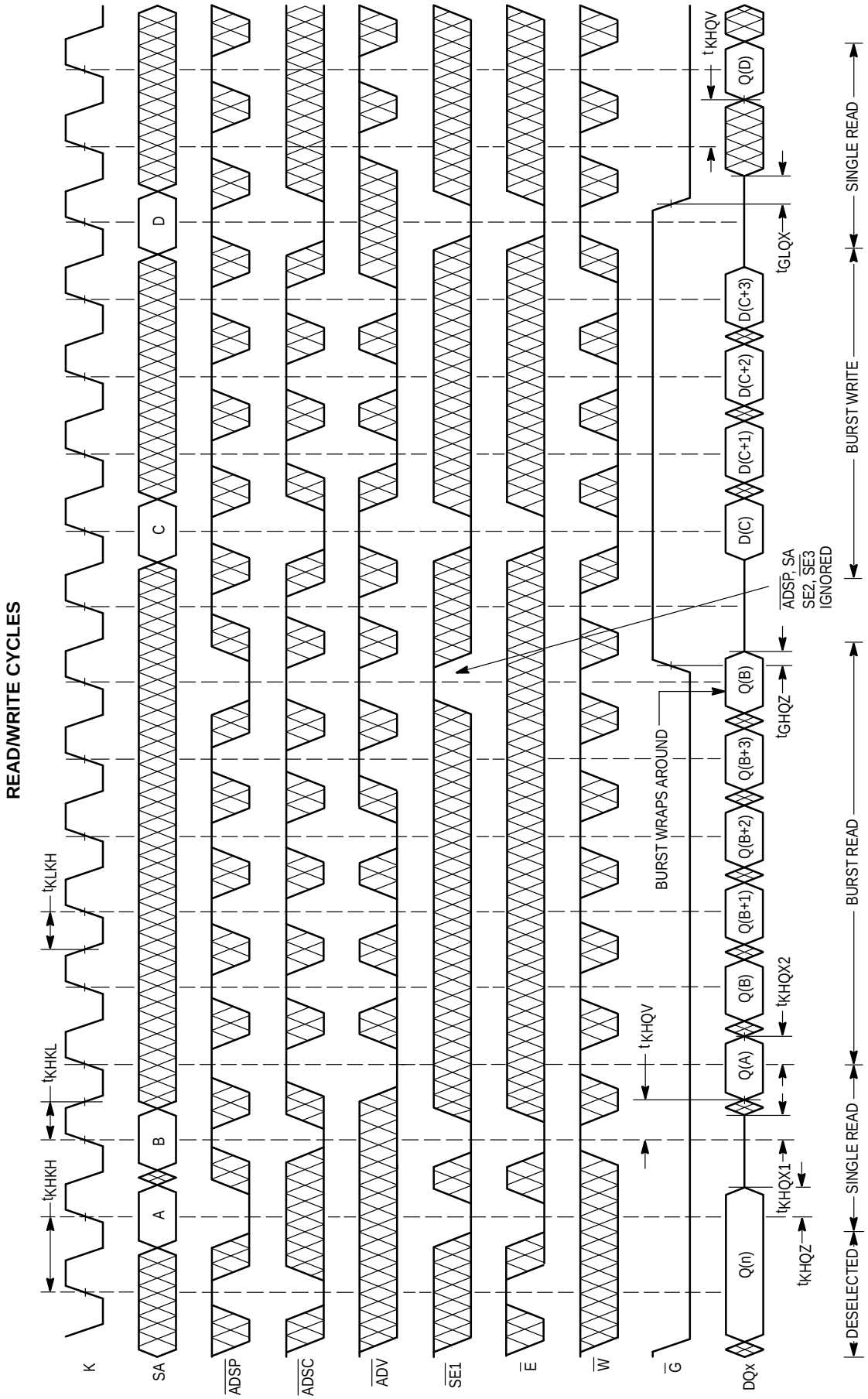
PULL–DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80



(c) Pull–Down

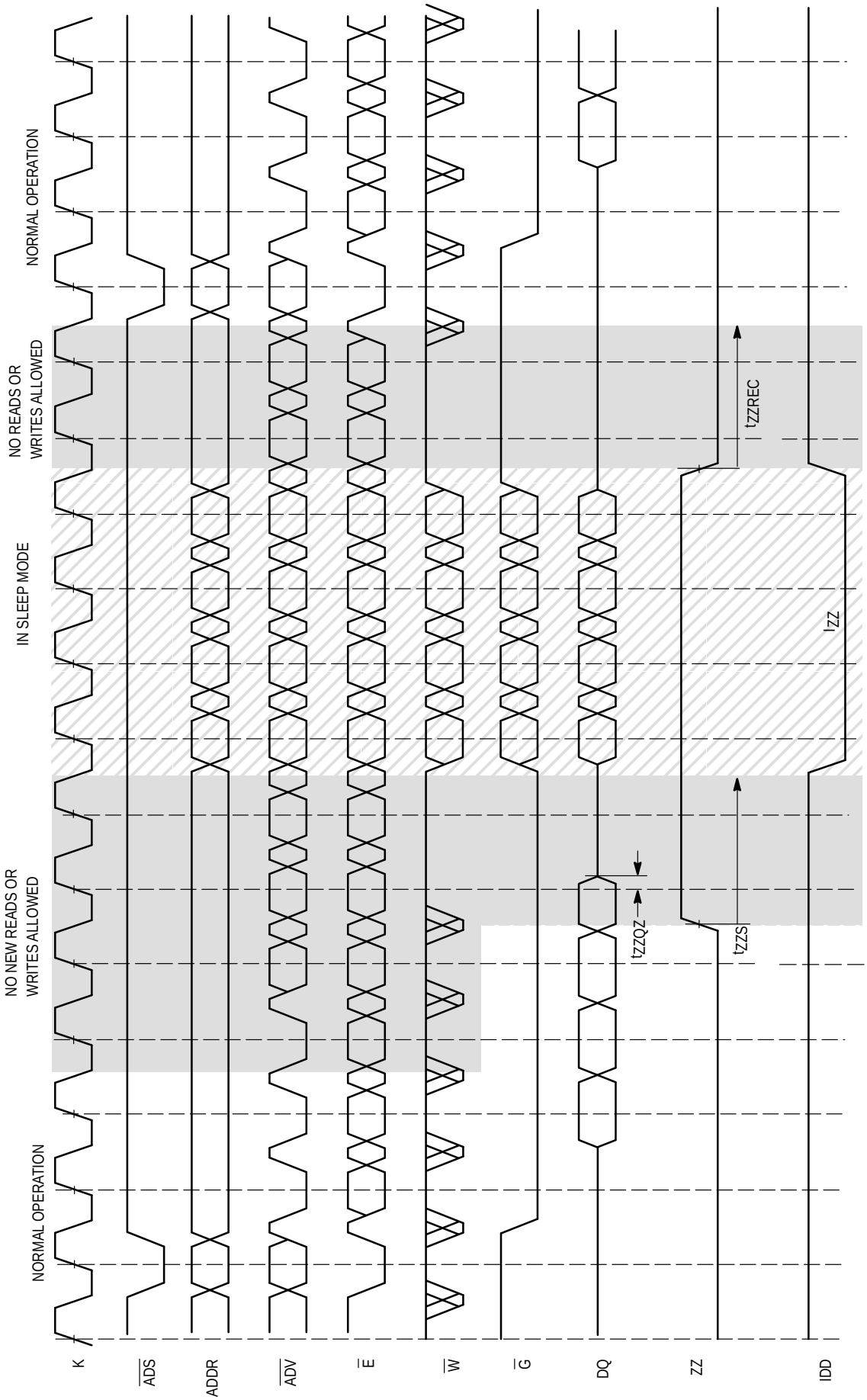
Figure 5. Typical Output Buffer Characteristics

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

SLEEP MODE TIMING



NOTE: $\overline{ADS}$ low = $\overline{ADSC}$ low or $\overline{ADSP}$ low.
$\overline{ADS}$ high = both $\overline{ADSC}$, $\overline{ADSP}$ high.
$\overline{E}$ low = $\overline{SE1}$ low, SE2 high, $\overline{SE3}$ low.
I_{ZZ} (max) specifications will not be met if inputs toggle.

APPLICATION INFORMATION

SLEEP MODE

A sleep mode feature, the ZZ pin, has been implemented on the MCM63P736 and MCM63P818. It allows the system designer to place the RAM in the lowest possible power condition by asserting ZZ. The sleep mode timing diagram shows the different modes of operation: Normal Operation, No READ/WRITE Allowed, and Sleep Mode. Each mode has its own set of constraints and conditions that are allowed.

Normal Operation: All inputs must meet setup and hold times prior to sleep and t_{ZZREC} nanoseconds after recovering from sleep. Clock (K) must also meet cycle, high, and low times during these periods. Two cycles prior to sleep, initiation of either a read or write operation is not allowed.

No READ/WRITE: During the period of time just prior to sleep and during recovery from sleep, the assertion of either ADSC, ADSP, or any write signal is not allowed. If a write operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM can not be guaranteed immediately after ZZ is asserted (prior to being in sleep).

Sleep Mode: The RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All inputs are allowed to toggle — the RAM will not be selected and perform any reads or writes. However, if inputs toggle, the I_{ZZ} (max) specification will not be met.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC– and Pentium–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM63P736 and MCM63P818. The burst counter feature of the BurstRAMs can be disabled, and the SRAMs can be configured to act upon a continuous stream of addresses. See Figure 6.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	ADSP	ADSC	ADV	SE1	LBO
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

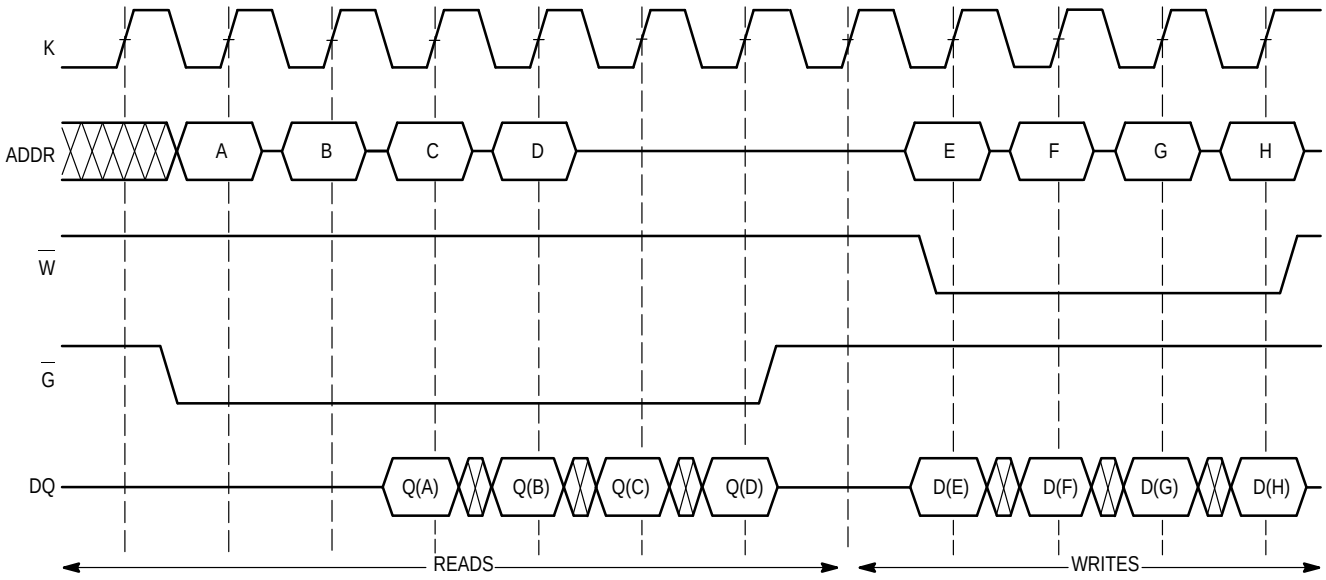


Figure 6. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

MCM	63P736 63P818	XX	X	X

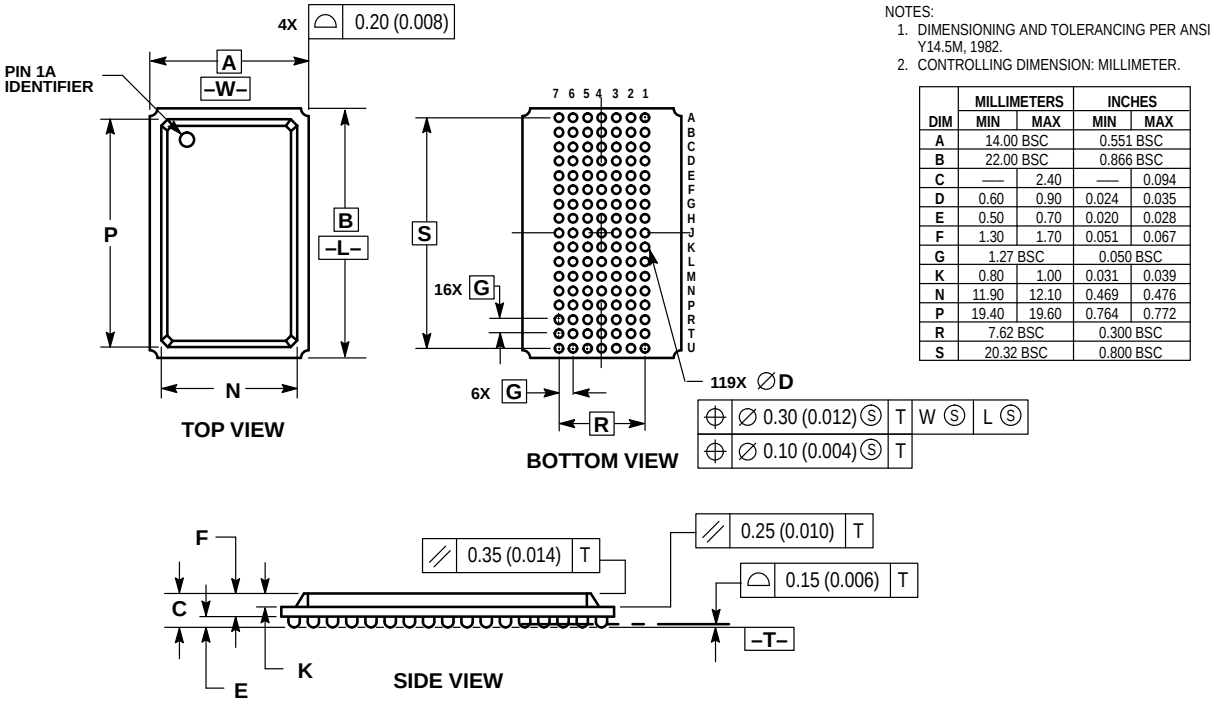
- MCM — Motorola Memory Prefix
- 63P736 / 63P818 — Part Number
- XX — Package (TQ = TQFP, ZP = PBGA)
- X — Speed (133 = 133 MHz, 100 = 100 MHz, 66 = 66 MHz)
- X — Blank = Trays, R = Tape and Reel

Full Part Numbers —

MCM63P736TQ133	MCM63P736TQ100	MCM63P736TQ66
MCM63P736TQ133R	MCM63P736TQ100R	MCM63P736TQ66R
MCM63P736ZP133	MCM63P736ZP100	MCM63P736ZP66
MCM63P736ZP133R	MCM63P736ZP100R	MCM63P736ZP66R
MCM63P818TQ133	MCM63P818TQ100	MCM63P818TQ66
MCM63P818TQ133R	MCM63P818TQ100R	MCM63P818TQ66R
MCM63P818ZP133	MCM63P818ZP100	MCM63P818ZP66
MCM63P818ZP133R	MCM63P818ZP100R	MCM63P818ZP66R

PACKAGE DIMENSIONS

ZP PACKAGE
7 x 17 BUMP PBGA
CASE 999–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	—	2.40	—	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	

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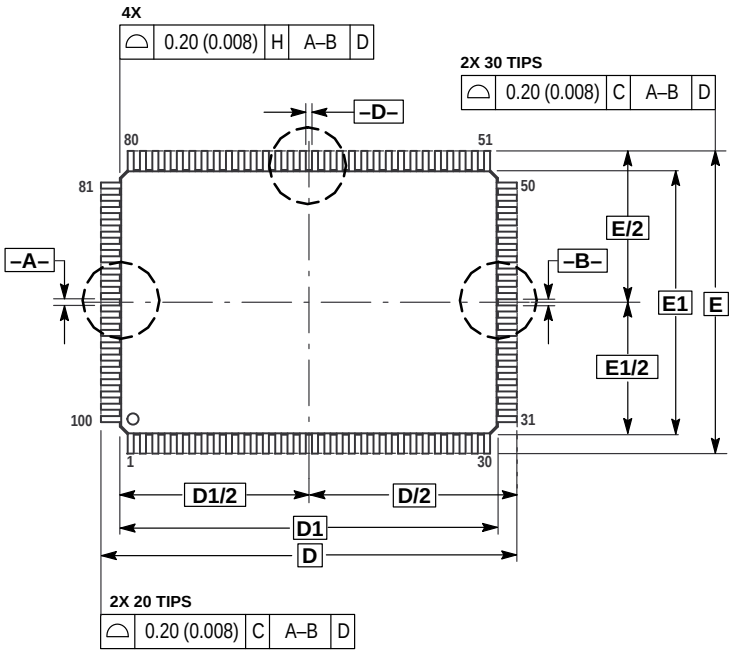
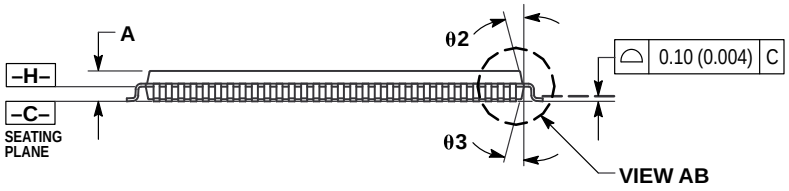
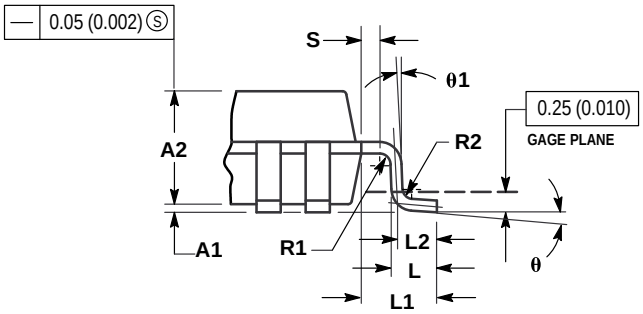
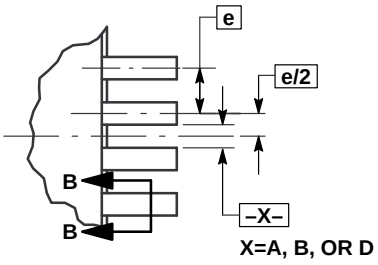
TQ PACKAGE
TQFP
CASE 983A–01



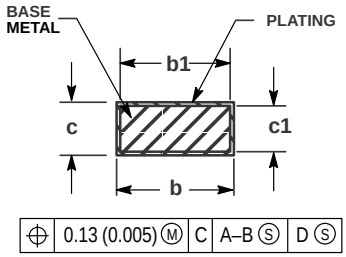




VIEW AB



VIEW Y



SECTION B–B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0 °	7 °	0 °	7 °
θ1	0 °	—	0 °	—
θ2	11 °	13 °	11 °	13 °
θ3	11 °	13 °	11 °	13 °

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