

MITSUBISHI MICROCOMPUTERS

3825 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3825 group is the 8-bit microcomputer based on the 740 family core technology.

The 3825 group has the LCD drive control circuit, an 8-channel A-D converter, and a Serial I/O as additional functions.

The various microcomputers in the 3825 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3825 Group, refer the section on group expansion.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time 0.5 μ s
(at 8 MHz oscillation frequency)
- Memory size
 - ROM 4 K to 60 K bytes
 - RAM 192 to 2048 bytes
- Programmable input/output ports 43
- Software pull-up/pull-down resistors (Ports P0–P8)
- Interrupts 17 sources, 16 vectors
(includes key input interrupt)
- Timers 8-bit X 3, 16-bit X 2

- Serial I/O 8-bit X 1 (UART or Clock-synchronized)
- A-D converter 8-bit X 8 channels
- LCD drive control circuit
 - Bias 1/2, 1/3
 - Duty 1/2, 1/3, 1/4
 - Common output 4
 - Segment output 40
- 2 Clock generating circuits
(connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
 - In high-speed mode 4.0 to 5.5 V
 - In middle-speed mode 2.5 to 5.5 V
(M version: 2.2 to 5.5 V)
 - (Extended operating temperature version: 3.0 to 5.5 V)
 - In low-speed mode 2.5 to 5.5 V
(M version: 2.2 to 5.5 V)
 - (Extended operating temperature version: 3.0 to 5.5 V)
- Power dissipation
 - In high-speed mode 32 mW
(at 8 MHz oscillation frequency, at 5 V power source voltage)
 - In low-speed mode 45 μ W
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range – 20 to 85°C
(Extended operating temperature version: –40 to 85°C)

APPLICATIONS

Camera, household appliances, consumer electronics, etc.

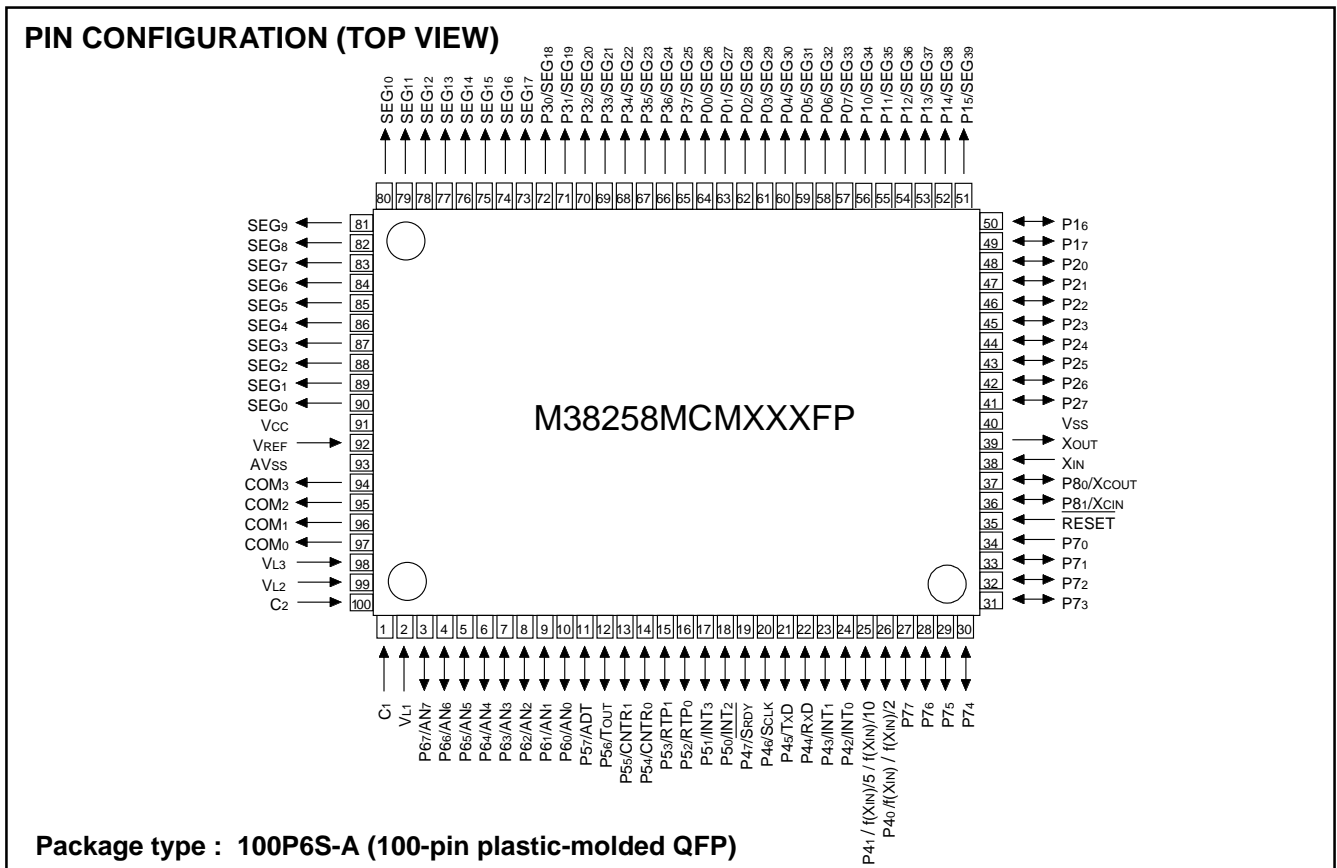
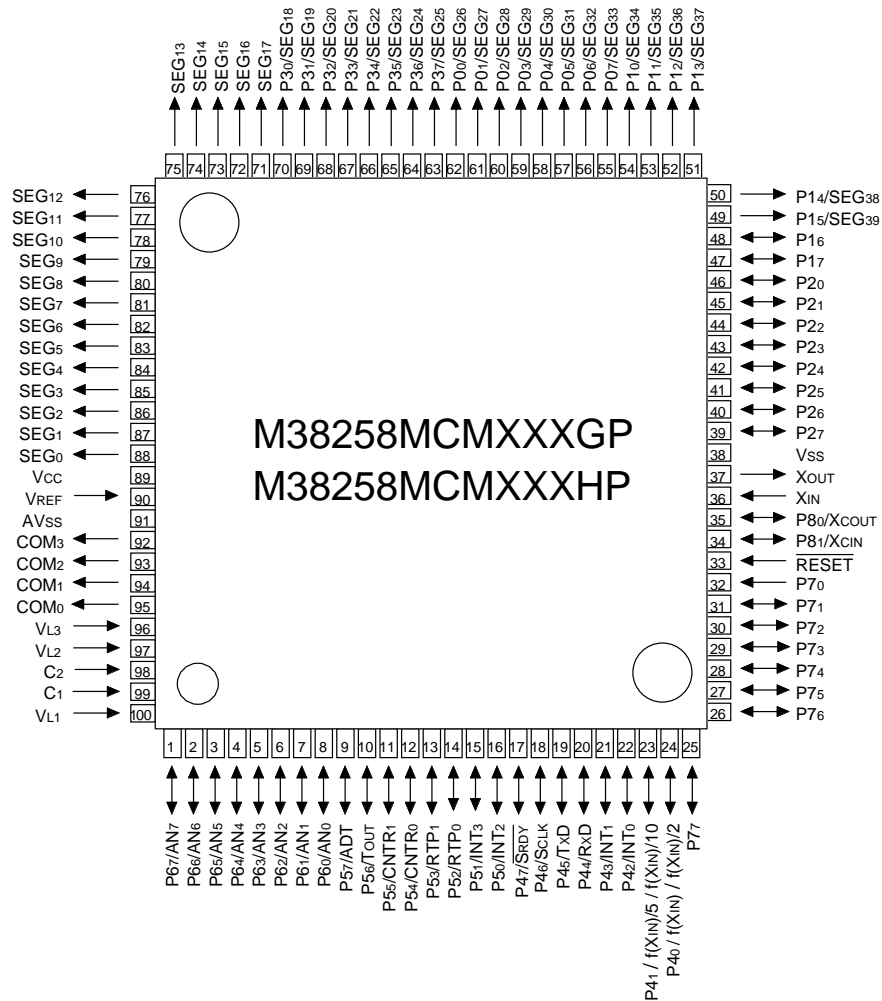


Fig. 1 Pin configuration of M38258MCMXXXFP
(The pin configuration of 100D0 is same as this.)

PIN CONFIGURATION (TOP VIEW)



Package type : GP 100P6Q-A (100-pin plastic-molded LQFP)
 Package type : HP 100PFB-A (100-pin plastic-molded TQFP)

Fig. 2 Pin configuration of M38258MCMXXXGP, M38258MCMXXXHP

FUNCTIONAL BLOCK DIAGRAM (Package : 100P6S-A)

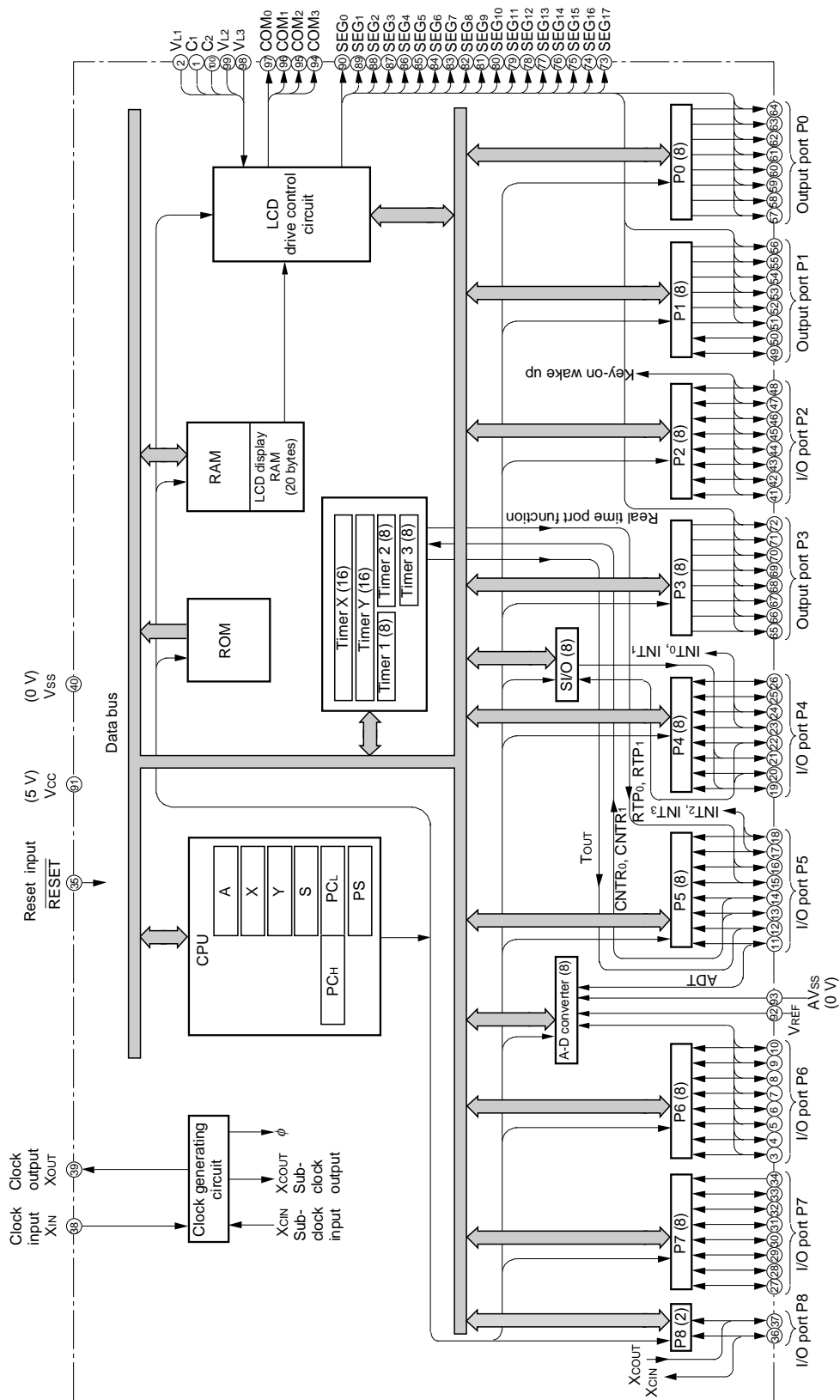


Fig. 3 Functional block diagram

PIN DESCRIPTION

Table 1. Pin description (1)

Pin	Name	Function	
			Function except a port function
Vcc, Vss	Power source	•Apply voltage of power source to Vcc, and 0 V to Vss. (For the limits of Vcc, refer to "Recommended operating conditions".)	
VREF	Analog reference voltage	• Reference voltage input pin for A-D converter.	
AVss	Analog power source	• GND input pin for A-D converter. • Connect to Vss.	
RESET	Reset input	• Reset input pin for active "L"	
XIN	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between XIN pin and XOUT pin. • Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.	
XOUT	Clock output	• If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. • This clock is used as the oscillating source of system clock.	
VL1 – VL3	LCD power source	• Input $0 \leq VL1 \leq VL2 \leq VL3 \leq Vcc$ voltage • Input 0 – VL3 voltage to LCD	
C1, C2	Charge-pump capacitor pin	• External capacitor pins for a voltage multiplier (3 times) of LCD control.	
COM0 – COM3	Common output	• LCD common output pins • COM2 and COM3 are not used at 1/2 duty ratio. • COM3 is not used at 1/3 duty ratio.	
SEG0 – SEG17	Segment output	• LCD segment output pins	
P00/SEG26 – P07/SEG33	Output port P0	• 8-bit output port • CMOS 3-state output structure • Pull-down control is enabled. • Port output control is enabled.	• LCD segment pins
P10/SEG34 – P15/SEG39	Output port P1	• 6-bit output port • CMOS 3-state output structure • Pull-down control is enabled. • Port output control is enabled.	
P16, P17	I/O port P1	• 2-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	
P20 – P27	I/O port P2	• 8-bit Input port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Key input (key-on wake up) interrupt input pins
P30/SEG18 – P37/SEG25	Output port P3	• 8-bit output port • CMOS 3-state output structure • Pull-down control is enabled. • Port output control is enabled.	• LCD segment pins

Table 2. Pin description (2)

Pin	Name	Function	Function except a port function
P40/f(XIN)/ f(XIN)/2, P41/f(XIN)/5/ f(XIN)/10	I/O port P4	<ul style="list-style-type: none"> • 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• Clock output pins
P42/INT0, P43/INT1			• Interrupt input pins
P44/RxD, P45/TxD, P46/SCLK, P47/SRDY			• Serial I/O function pins
P50/INT2, P51/INT3	I/O port P5	<ul style="list-style-type: none"> • 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• Interrupt input pins
P52/RTP0, P53/RTP1			• Real time port function pins
P54/CNTR0, P55/CNTR1			• Timers X, Y functions pins
P56/TOUT			• Timer 2 output pin
P57/ADT			• A-D trigger input pin
P60/AN0– P67/AN7	I/O port P6	<ul style="list-style-type: none"> • 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• A-D conversion input pins
P70	Input port P7	<ul style="list-style-type: none"> • 1-bit input port • CMOS compatible input level 	
P71–P77	I/O port P7	<ul style="list-style-type: none"> • 7-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	
P80/XCOUT, P81/XCIN	I/O port P8	<ul style="list-style-type: none"> • 2-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled. 	• Sub-clock generating circuit I/O pins (Connect a resonator. External clock cannot be used.)

PART NUMBERING

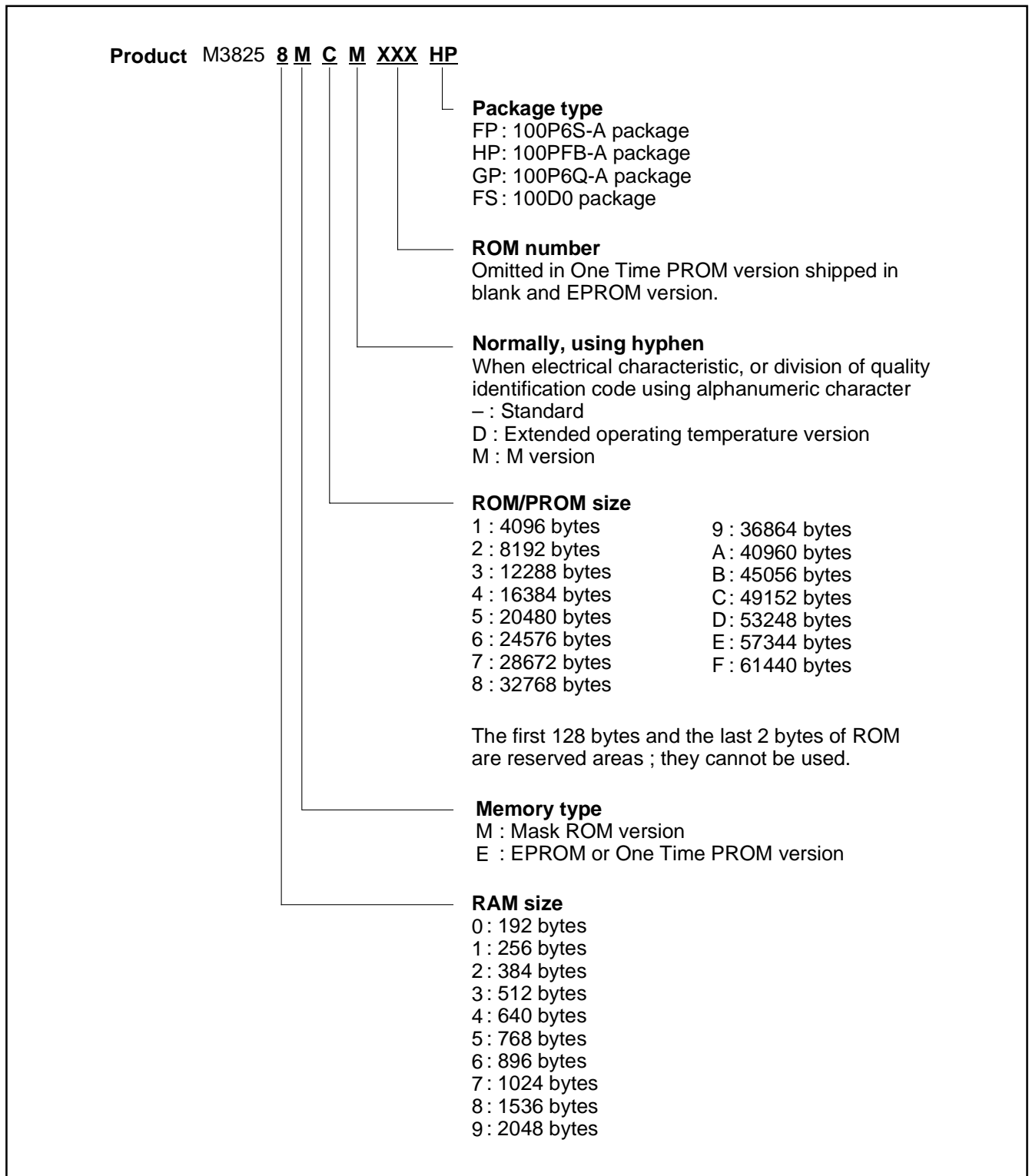


Fig. 4 Part numbering

3825 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

GROUP EXPANSION (STANDARD, ONE TIME PROM VERSION, EPROM VERSION)

Mitsubishi plans to expand the 3825 group(Standard, One Time PROM version, EPROM version) as follows.

Memory Type

Support for mask ROM, One Time PROM, and EPROM versions.

Memory Size

ROM size 16 K to 60 Kbytes

RAM size 640 to 2048 bytes

Packages

100PFB-A 0.4 mm-pitch plastic molded TQFP

100P6Q-A 0.5 mm-pitch plastic molded LQFP

100P6S-A 0.65 mm-pitch plastic molded QFP

100D0 0.65 mm-pitch ceramic LCC (EPROM version)

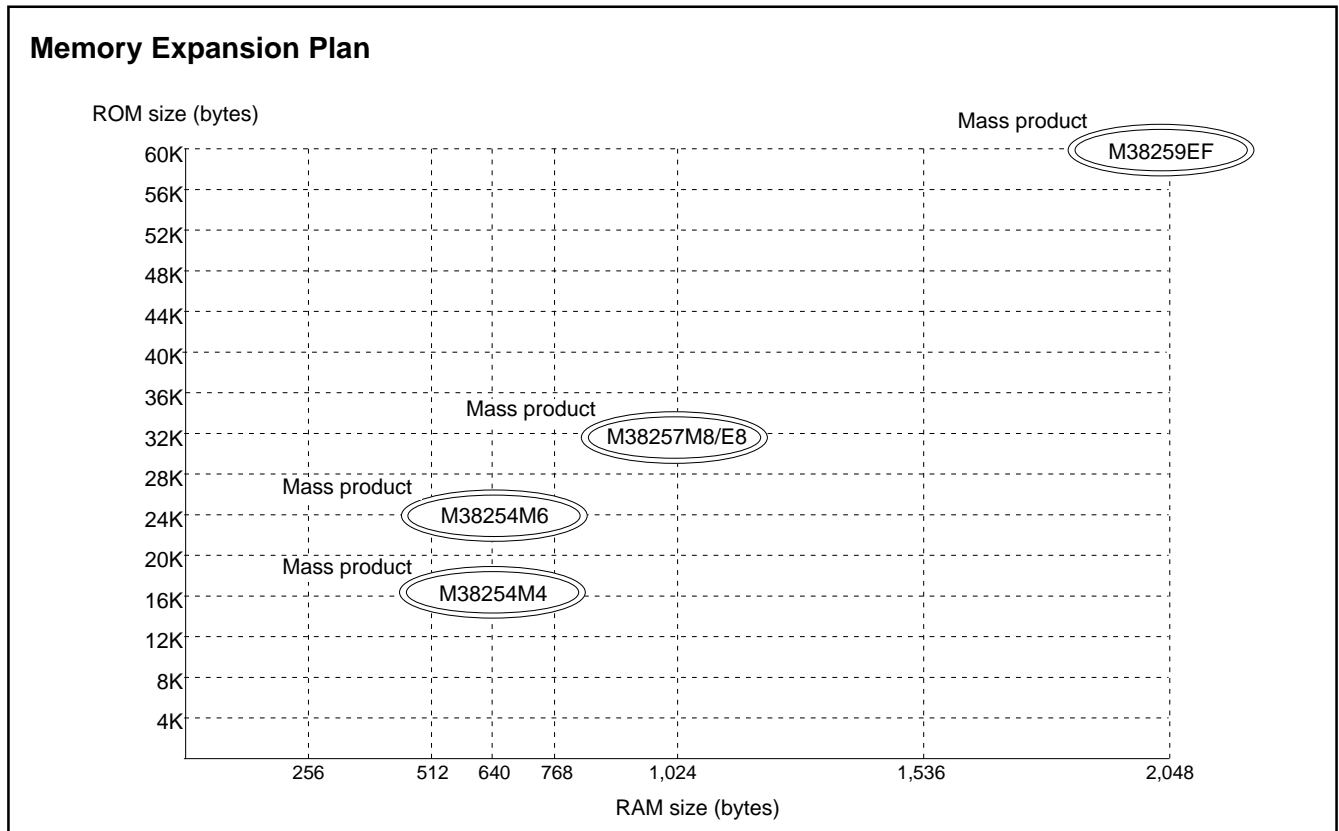


Fig. 5 Memory expansion plan

Currently products are listed below.

Table 3. List of products

As of Dec. 2000

Product	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38254M4-XXXFP	16384 (16254)	640	100P6S-A	Mask ROM version
M38254M4-XXXGP			100P6Q-A	Mask ROM version
M38254M6-XXXFP	24576 (24446)	640	100P6S-A	Mask ROM version
M38254M6-XXXGP			100P6Q-A	Mask ROM version
M38257M8-XXXFP	32768 (32638)	1024	100P6S-A	Mask ROM version
M38257E8FP			100P6S-A	One Time PROM version (blank)
M38257M8-XXXGP			100P6Q-A	Mask ROM version
M38257E8GP			100P6Q-A	One Time PROM version (blank)
M38257E8FS			100D0	EPROM version
M38259E8FP			100P6S-A	One Time PROM version (blank)
M38259EFHP	61440 (61310)	2048	100PFB-A	One Time PROM version (blank)
M38259EFGP			100P6Q-A	One Time PROM version (blank)
M38259E8FS			100D0	EPROM version

**GROUP EXPANSION
(EXTENDED OPERATING TEMPERATURE VERSION)**

Mitsubishi plans to expand the 3825 group (Extended operating temperature version) as follows.

Memory Type

Support for mask ROM, one time PROM version.

Memory Size

ROM size 16 K to 60 Kbytes
RAM size 640 to 2048 bytes

Packages

100P6S-A 0.65 mm-pitch plastic molded QFP

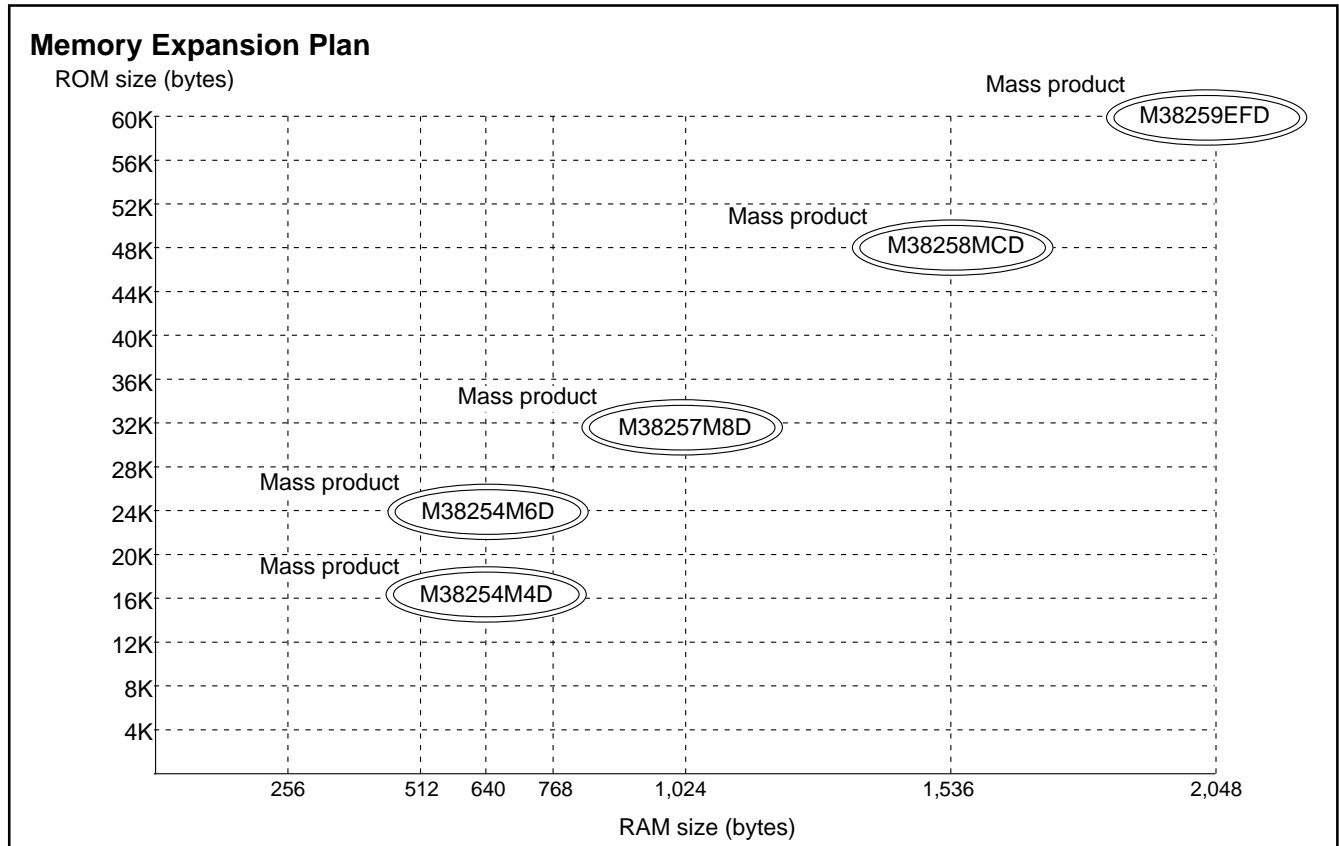


Fig. 6 Memory expansion plan for extended operating temperature version

Currently products are listed below.

Table 4. List of products for extended operating temperature version

As of Dec. 2000

Product	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38254M4DXXXFP	16384 (16254)	640	100P6S-A	Mask ROM version
M38254M6DXXXFP	24576 (24446)	640	100P6S-A	Mask ROM version
M38257M8DXXXFP	32768 (32638)	1024	100P6S-A	Mask ROM version
M38258MCDXXXFP	49152 (49022)	1536	100P6S-A	Mask ROM version
M38259EFDFFP	61440 (61310)	2048	100P6S-A	One Time PROM version (blank)

GROUP EXPANSION (M VERSION)

Mitsubishi plans to expand the 3825 group (M version) as follows.

Memory Type

Support for mask ROM version.

Memory Size

ROM size 48 Kbytes
 RAM size 1536 bytes

Packages

100PFB-A 0.4 mm-pitch plastic molded TQFP
 100P6Q-A 0.5 mm-pitch plastic molded LQFP
 100P6S-A 0.65 mm-pitch plastic molded QFP

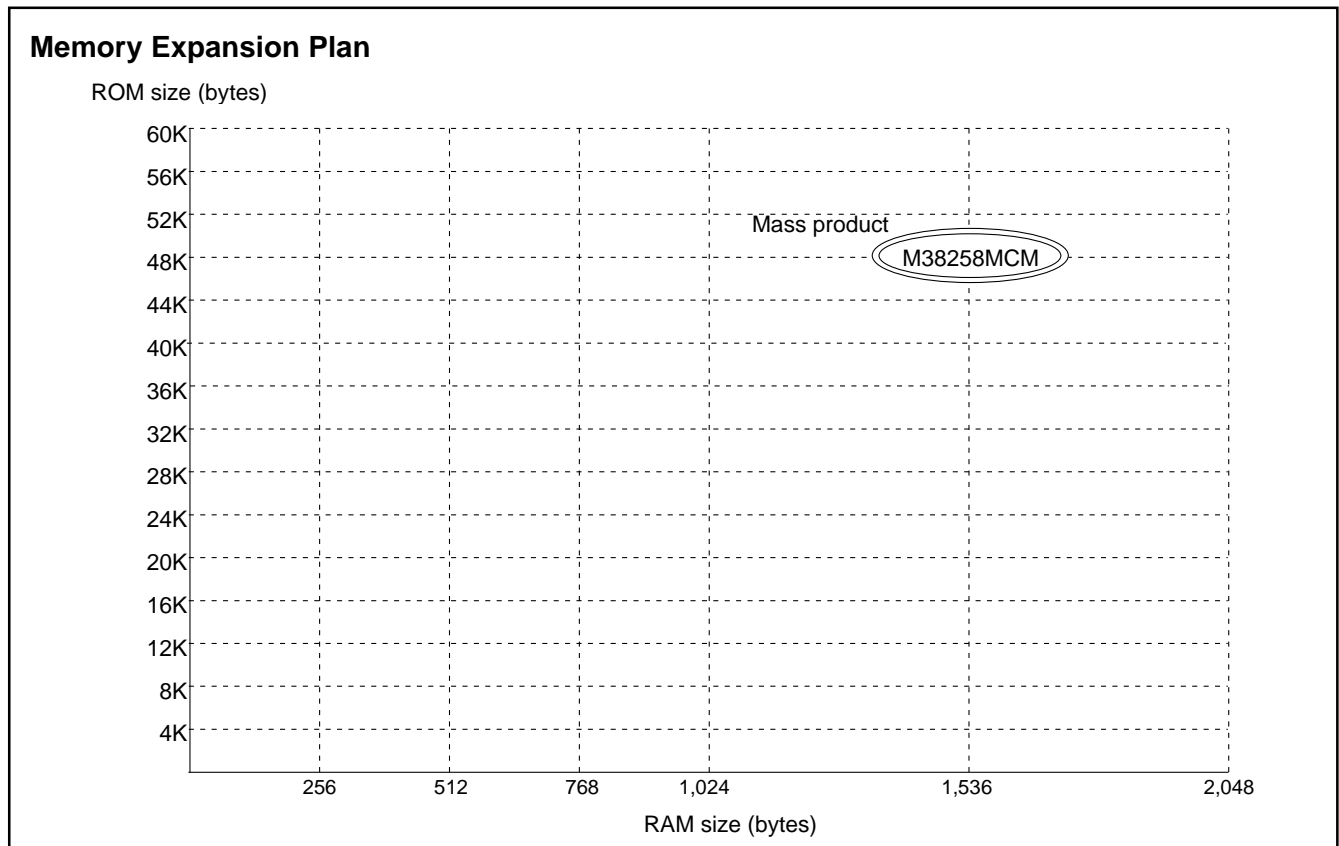


Fig. 7 Memory expansion plan for M version

Currently products are listed below.

Table 5. List of products for low power source version

As of Dec. 2000

Product	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38258MCMXXXFP	49152 (49022)	1536	100P6S-A	Mask ROM version
M38258MCMXXXHP			100PFB-A	Mask ROM version
M38258MCMXXXGP			100P6Q-A	Mask ROM version

**FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)**

The 3825 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:
The FST and SLW instruction cannot be used.
The STP, WIT, MUL, and DIV instruction can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 9.

Store registers other than those described in Figure 9 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

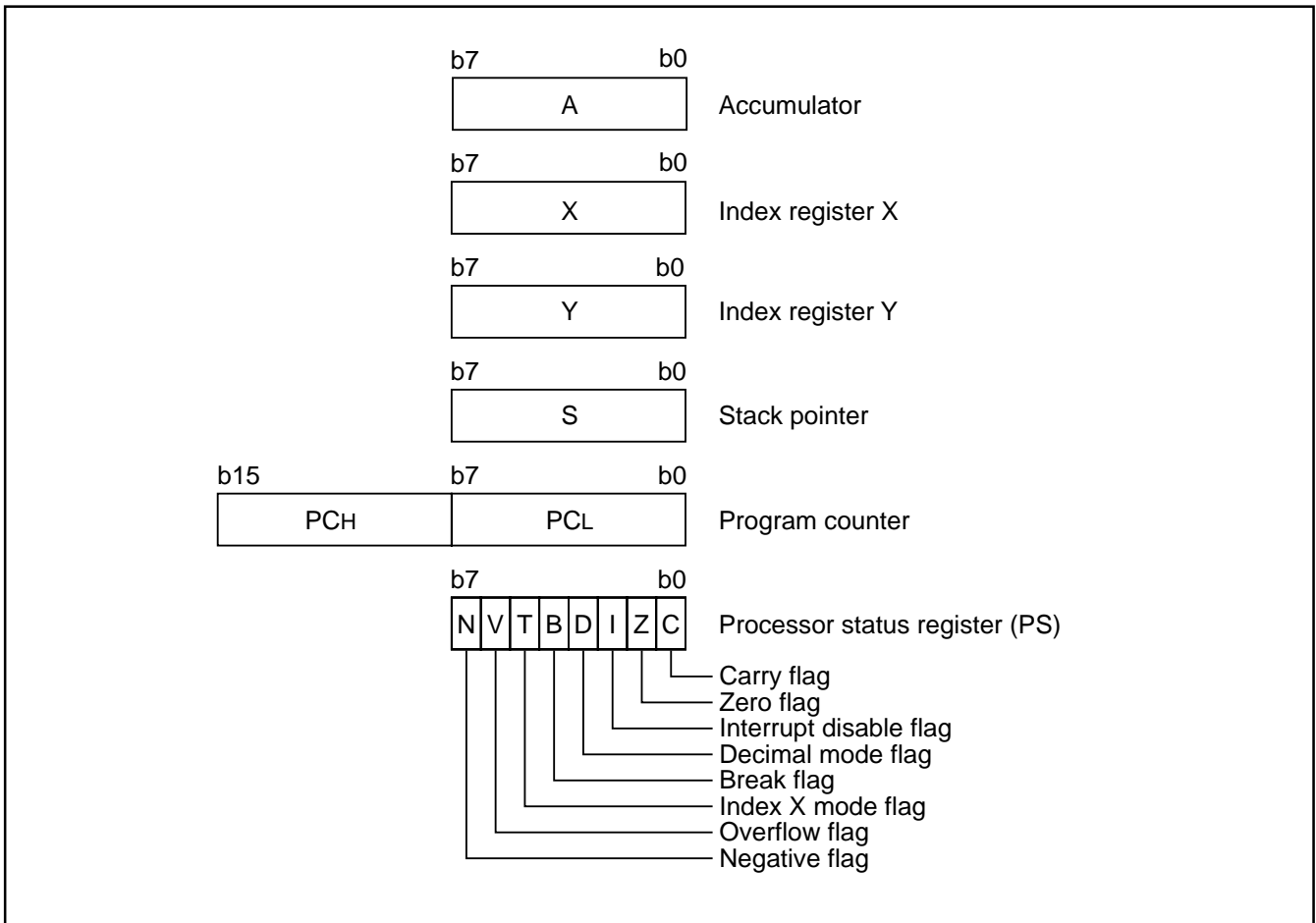


Fig. 8 740 Family CPU register structure

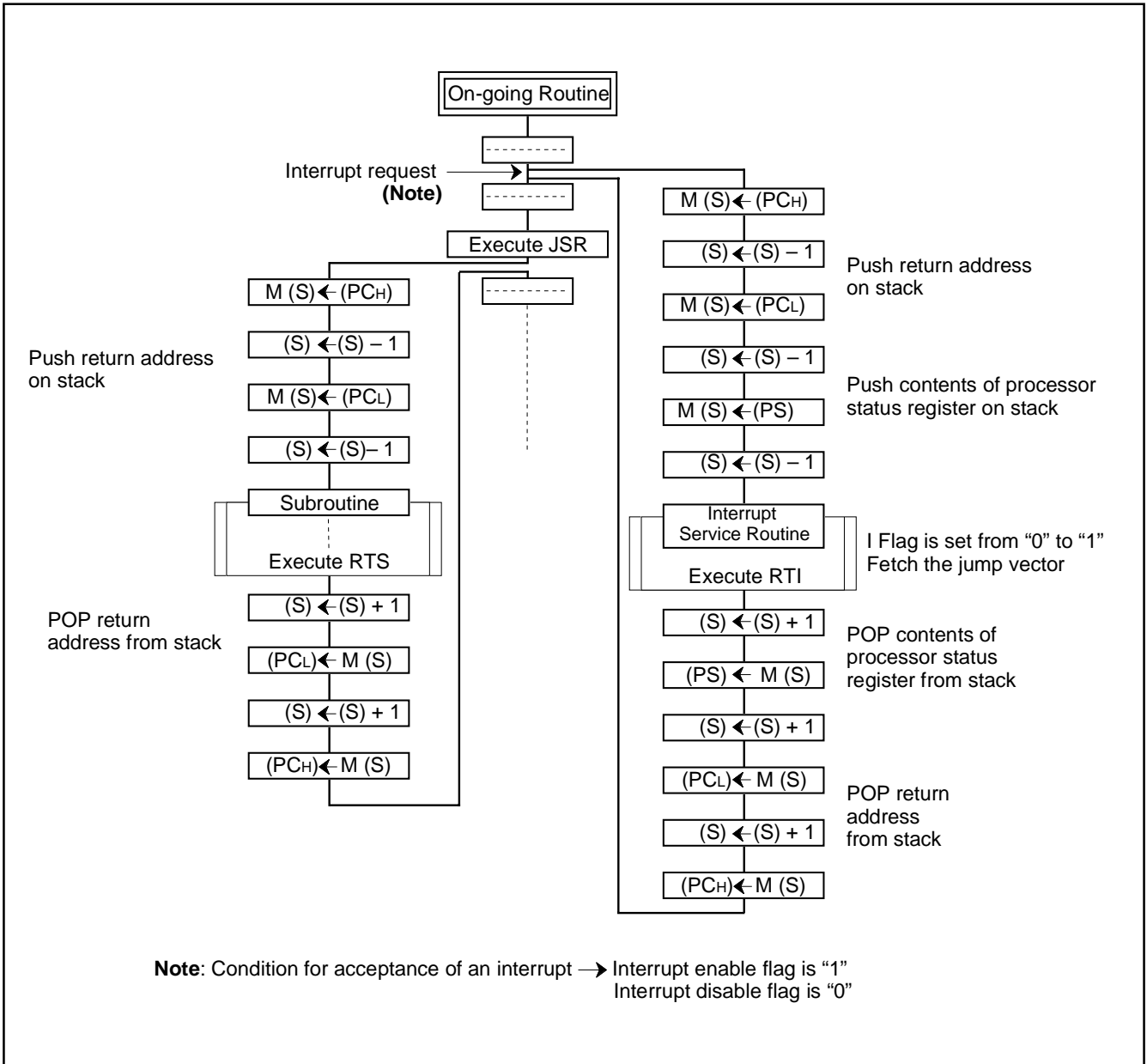


Fig. 9 Register push and pop at interrupt generation and subroutine call

Table 6 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

•Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 7 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

The CPU mode register is allocated at address 003B16.

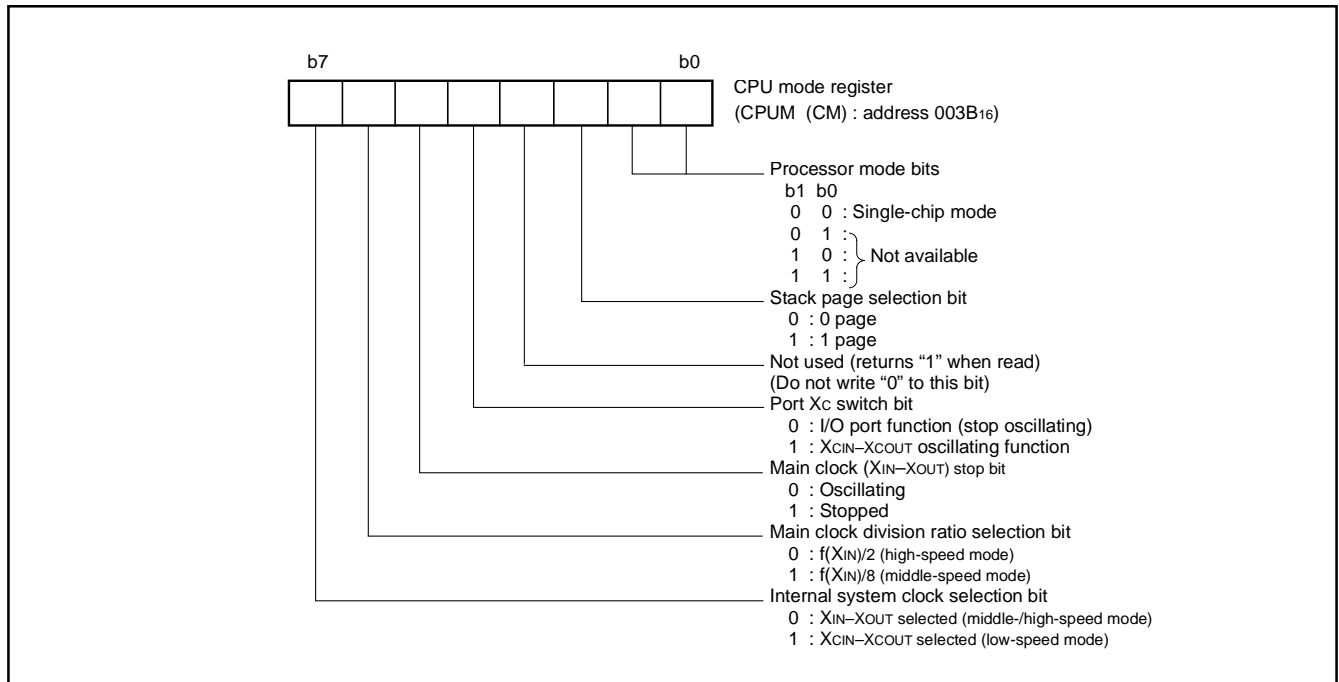


Fig. 10 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

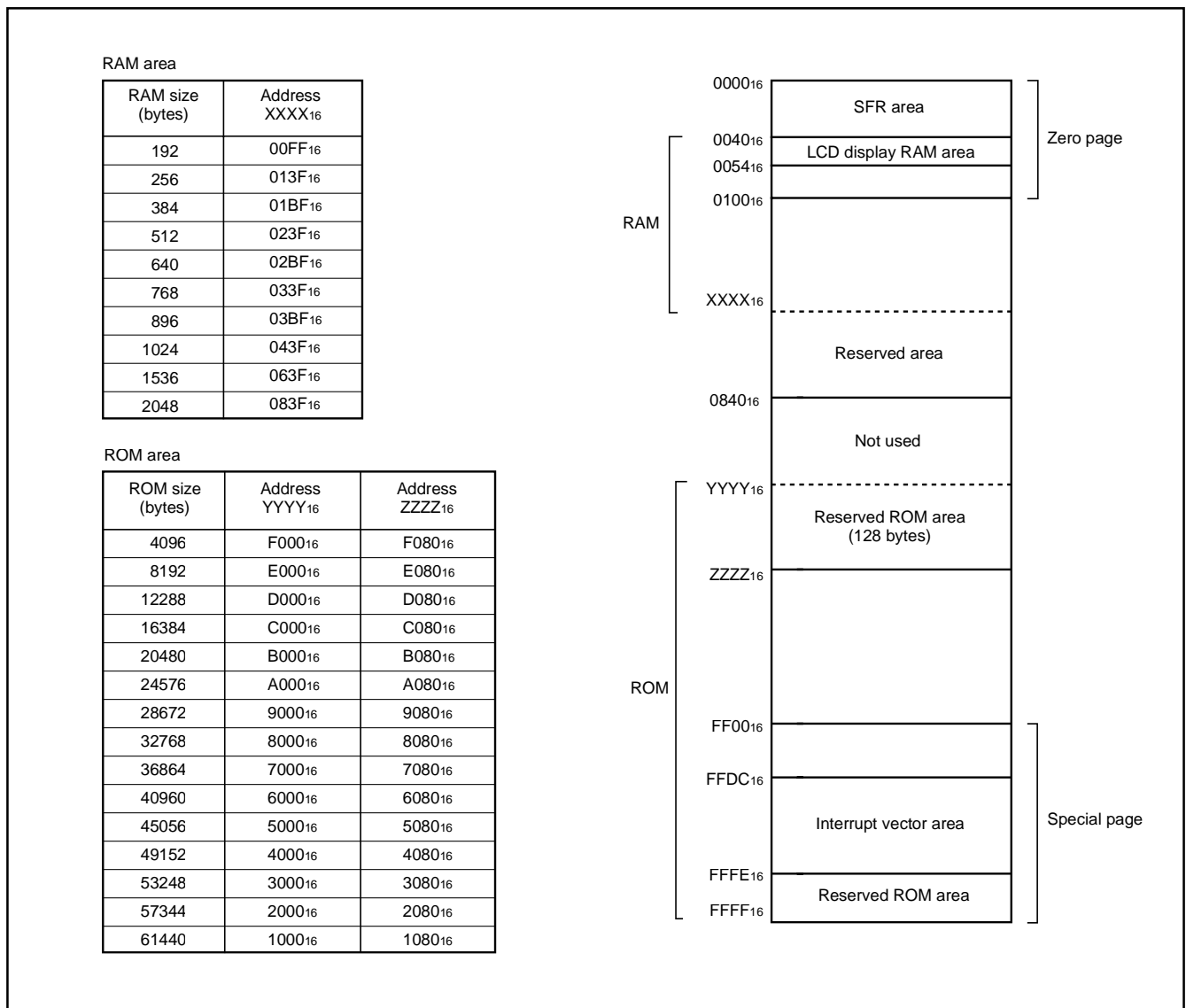


Fig. 11 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer X (low) (TXL)
0001 ₁₆		0021 ₁₆	Timer X (high) (TXH)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer Y (low) (TYL)
0003 ₁₆	Port P1 output control register (P1C)	0023 ₁₆	Timer Y (high) (TYH)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 1 (T1)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 2 (T2)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Timer 3 (T3)
0007 ₁₆		0027 ₁₆	Timer X mode register (TXM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer Y mode register (TYM)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 123 mode register (T123M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Clock output control register (TCON)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	
000C ₁₆	Port P6 (P6)	002C ₁₆	
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	
000E ₁₆	Port P7 (P7)	002E ₁₆	
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	
0010 ₁₆	Port P8 (P8)	0030 ₁₆	
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	
0012 ₁₆		0032 ₁₆	
0013 ₁₆		0033 ₁₆	
0014 ₁₆		0034 ₁₆	A-D control register (ADCON)
0015 ₁₆		0035 ₁₆	A-D conversion register (AD)
0016 ₁₆	PULL register A (PULLA)	0036 ₁₆	
0017 ₁₆	PULL register B (PULLB)	0037 ₁₆	
0018 ₁₆	Transmit/Receive buffer register (TB/RB)	0038 ₁₆	Segment output enable register (SEG)
0019 ₁₆	Serial I/O status register (SIOSTS)	0039 ₁₆	LCD mode register (LM)
001A ₁₆	Serial I/O control register (SIO1CON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART control register (UARTCON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator (BRG)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆		003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆		003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆		003F ₁₆	Interrupt control register 2 (ICON2)

Fig. 12 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The 3825 group has 43 programmable I/O pins arranged in seven I/O ports (ports P16, P17, P2, P4–P6, P71–P77, P80 and P81). The I/O ports have direction registers which determine the input/output direction of each individual pin. (Ports P16 and P17 are shared with bits 6 and 7 of the port P1 output control register). Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Port P1 Output Control Register

Bit 0 of the port P1 output control register (address 000316) enables control of the output of ports P10 to P15.

When the bit is set to “1”, the port output function is valid.

In this case, setting of the PULL register A to ports P10 to P15 is invalid.

When resetting, bit 0 of the port P1 output control register is set to “0” (the port output function is invalid.)

Pull-up/Pull-down Control

By setting the PULL register A (address 001616) or the PULL register B (address 001716), ports P0 to P8 except P70 can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports. (except for ports P0 and P3).

Ports P0 and P3 share the port output control function with bit 0 of the PULL register A. When set to “1”, the port output function is invalid (Pull-down is valid).

When set to “0”, the port output function is valid (Pull-down is invalid).

The PULL register A setting is invalid for pins set to segment output with the segment output enable register.

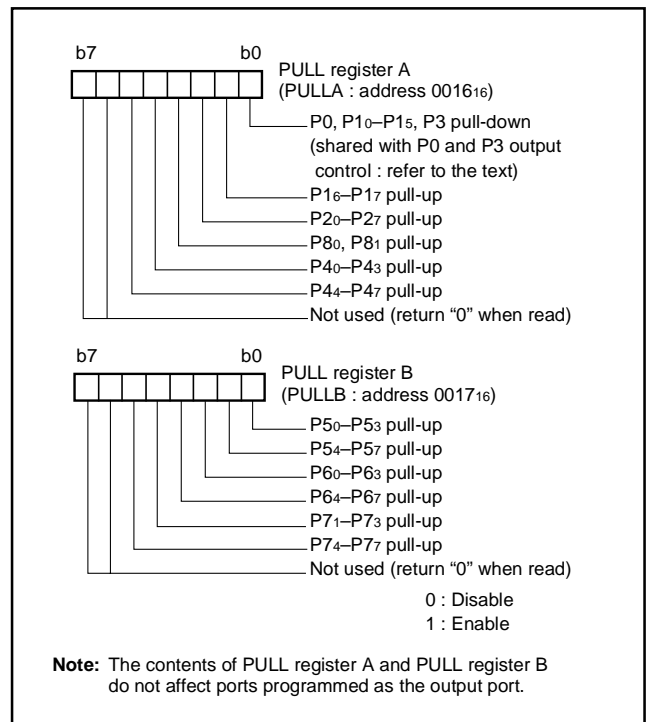


Fig. 13 Structure of PULL register A and PULL register B

Table 8. I/O ports functions

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P00/SEG26– P07/SEG33	Port P0	Output	CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P10/SEG34– P15/SEG39	Port P1	Output	CMOS 3-state output	LCD segment output	PULL register A Segment output enable register Port P1 output control register	(1)
P16, P17		Input/output, individual bits	CMOS compatible input level CMOS 3-state output		PULL register A	(2)
P20–P27	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key-on wake up interrupt input	PULL register A Interrupt control register 2	(2)
P30/SEG18– P37/SEG25	Port P3	Output	CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P40/f(XIN)/ f(XIN)/2, P41/f(XIN)/5/ f(XIN)/10	Port P4	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Clock output	Clock output control register PULL register A	(2)
P42/INT0, P43/INT1				External interrupt input	PULL register A Interrupt edge selection register	
P44/RxD P54/TxD P46/SCLK P47/SRDY				Serial I/O function I/O	PULL register A Serial I/O control register Serial I/O status register UART control register	(3)
						(4)
						(5)
						(6)
P50/INT2, P51/INT3	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input	PULL register B Interrupt edge selection register	(2)
P52/RTP0, P53/RTP1				Real time port function output	PULL register B Timer X mode register	(7)
P54/CNTR0				Timer X function I/O	PULL register B Timer X mode register	(8)
P55/CNTR1				Timer Y function input	PULL register B Timer Y mode register	(9)
P56/TOUT				Timer 2 output	PULL register B Timer 123 mode register	(8)
P57/ADT				A-D trigger input	PULL register B A-D control register	(9)
P60/AN0– P67/AN7	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input	PULL register B A-D control register	(10)
P70	Port P7	Input	CMOS compatible input level			(11)
P71–P77		Input/output, individual bits	CMOS compatible input level CMOS 3-state output		PULL register B	(12)
P80/XCOUT	Port P8	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit	PULL register A CPU mode register	(13)
P81/XCIN						(14)
COM0–COM3	Common	Output	LCD common output		LCD mode register	(15)
SEG0–SEG17	Segment	Output	LCD segment output			(16)

Note 1: When using double-function ports as functional I/O pins, refer the method to the relevant sections.

Note 2: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

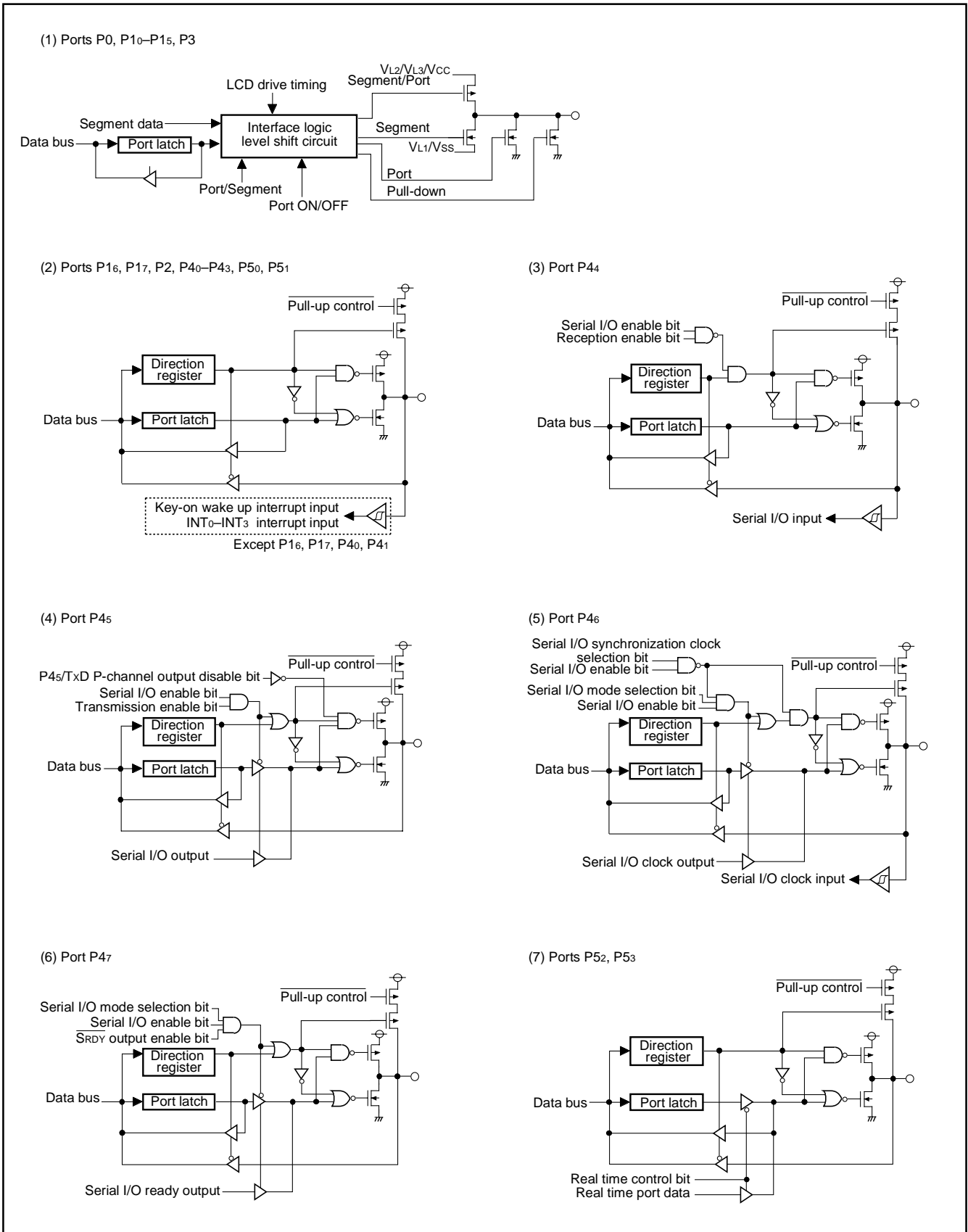


Fig. 14 Port block diagram (1)

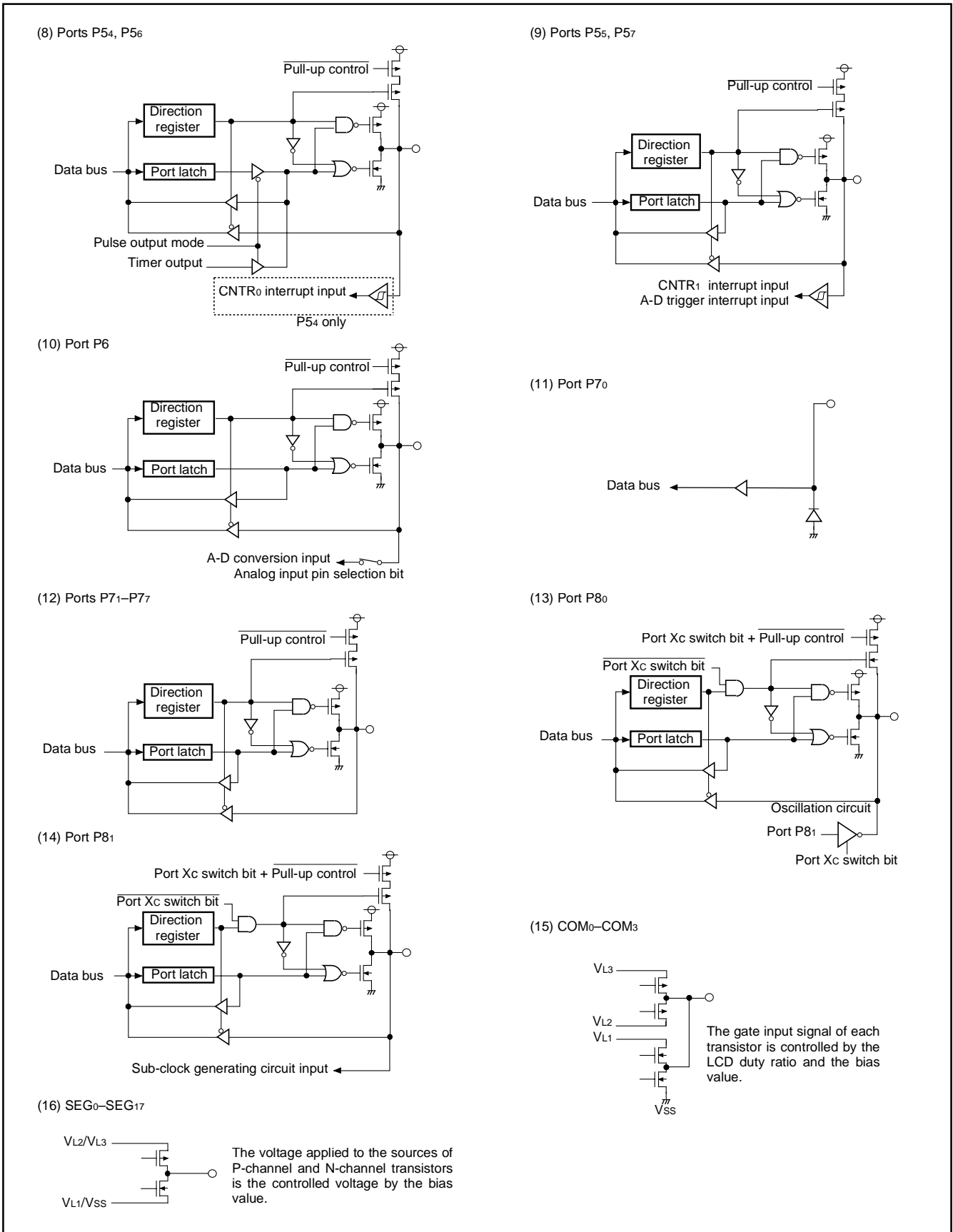


Fig. 15 Port block diagram (2)

INTERRUPTS

Interrupts occur by seventeen sources: eight external, eight internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

Table 9. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT ₀	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
INT ₁	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
Serial I/O reception	4	FFF7 ₁₆	FFF6 ₁₆	At completion of serial I/O data reception	Valid when serial I/O is selected
Serial I/O transmission	5	FFF5 ₁₆	FFF4 ₁₆	At completion of serial I/O transmit shift or when transmission buffer is empty	Valid when serial I/O is selected
Timer X	6	FFF3 ₁₆	FFF2 ₁₆	At timer X underflow	
Timer Y	7	FFF1 ₁₆	FFF0 ₁₆	At timer Y underflow	
Timer 2	8	FFEF ₁₆	FFEE ₁₆	At timer 2 underflow	
Timer 3	9	FFED ₁₆	FFEC ₁₆	At timer 3 underflow	
CNTR ₀	10	FFEB ₁₆	FFEA ₁₆	At detection of either rising or falling edge of CNTR ₀ input	External interrupt (active edge selectable)
CNTR ₁	11	FFE9 ₁₆	FFE8 ₁₆	At detection of either rising or falling edge of CNTR ₁ input	External interrupt (active edge selectable)
Timer 1	12	FFE7 ₁₆	FFE6 ₁₆	At timer 1 underflow	
INT ₂	13	FFE5 ₁₆	FFE4 ₁₆	At detection of either rising or falling edge of INT ₂ input	External interrupt (active edge selectable)
INT ₃	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of INT ₃ input	External interrupt (active edge selectable)
Key input (Key-on wake up)	15	FFE1 ₁₆	FFE0 ₁₆	At falling of conjunction of input level for port P2 (at input mode)	External interrupt (valid when an "L" level is applied)
ADT	16	FFDF ₁₆	FFDE ₁₆	At falling of ADT input	Valid when ADT interrupt is selected
A-D conversion				At completion of A-D conversion	External interrupt (Valid at falling) Valid when A-D interrupt is selected
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge
 Related register: Interrupt edge selection register (address 3A16)
 Timer X mode register (address 2716)
 Timer Y mode register (address 2816)
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
 Related register: A-D control register (address 3416)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

- ①Set the corresponding interrupt enable bit to "0" (disabled).
- ②Set the interrupt edge select bit or the interrupt source select bit to "1".
- ③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④Set the corresponding interrupt enable bit to "1" (enabled).

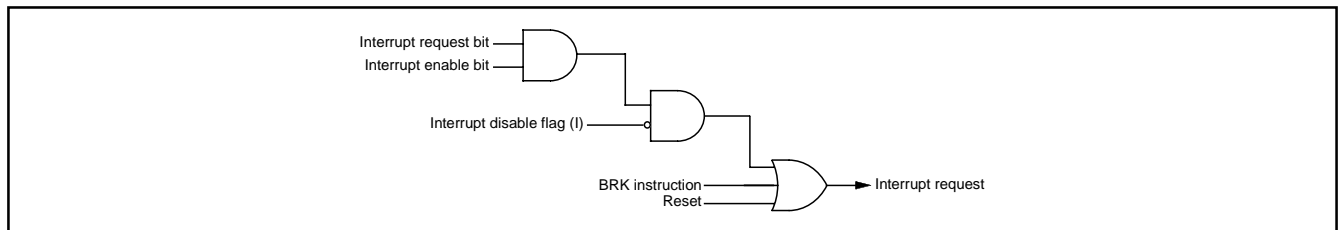


Fig. 16 Interrupt control

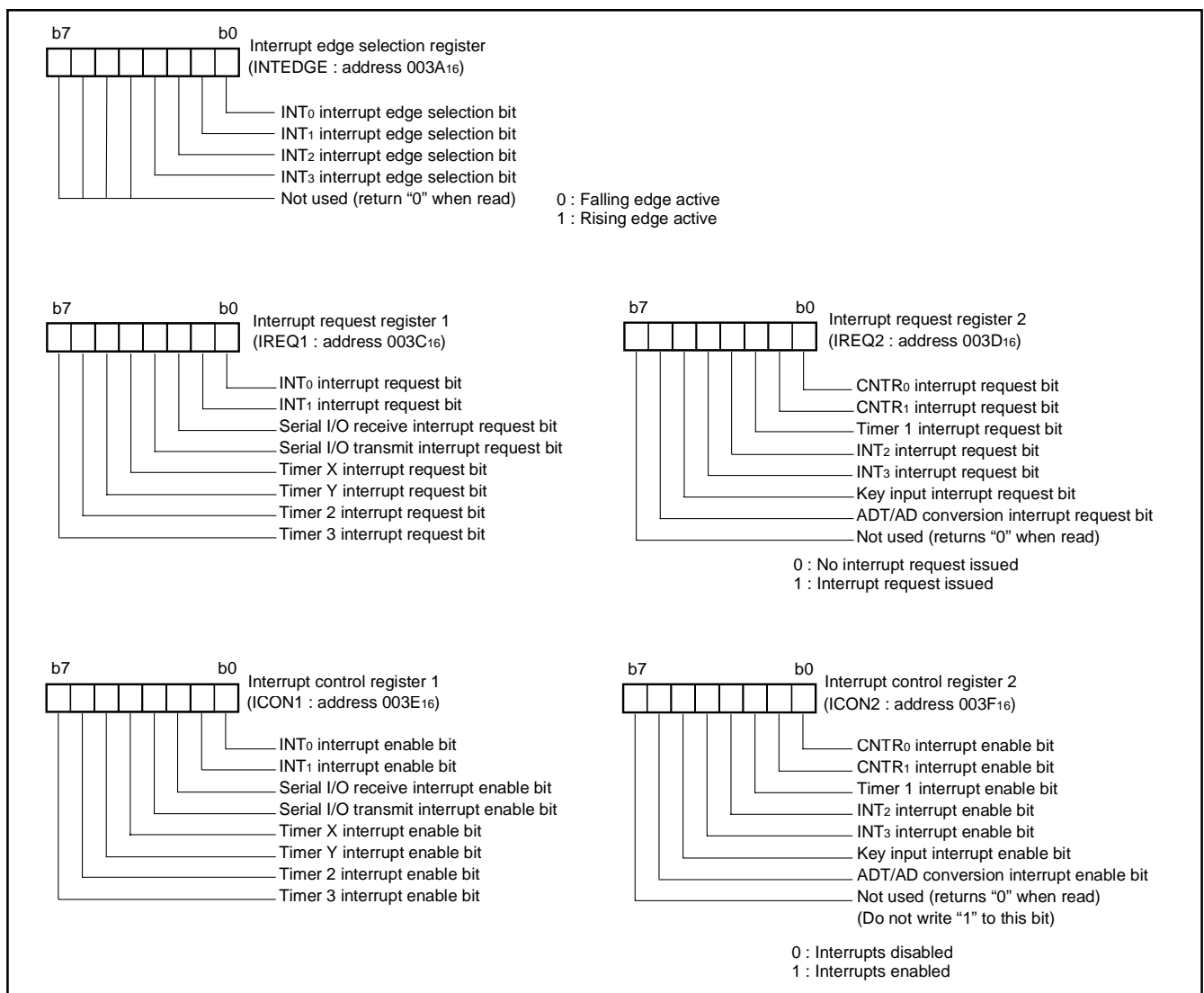


Fig. 17 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake Up)

A Key-on wake up interrupt request is generated by applying a falling edge to any pin of port P2 that have been set to input mode. In other words, it is generated when AND of input level goes from

"1" to "0". An example of using a key input interrupt is shown in Figure 18, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P20–P23.

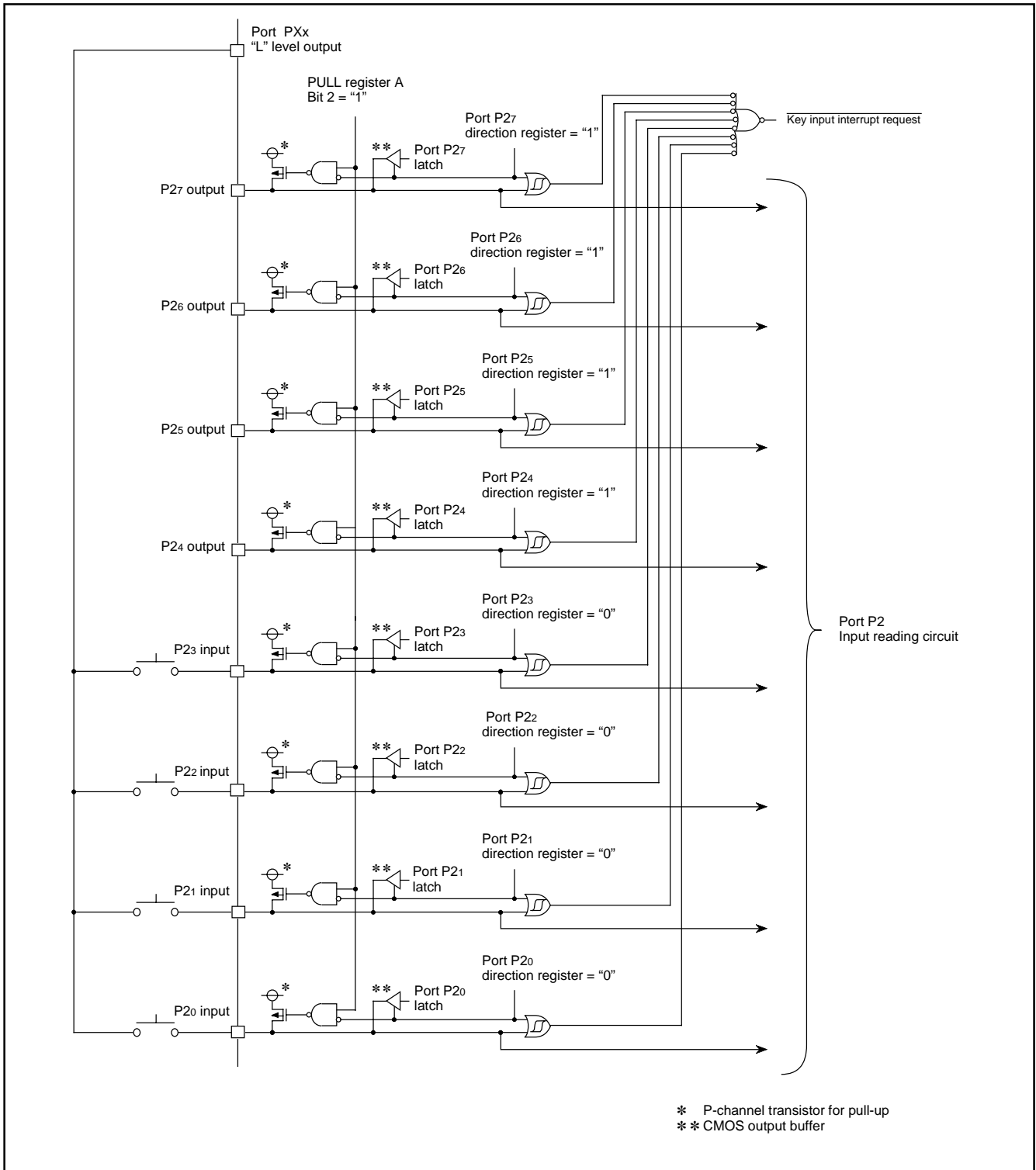


Fig. 18 Connection example when using key input interrupt and port P2 block diagram

TIMERS

The 3825 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

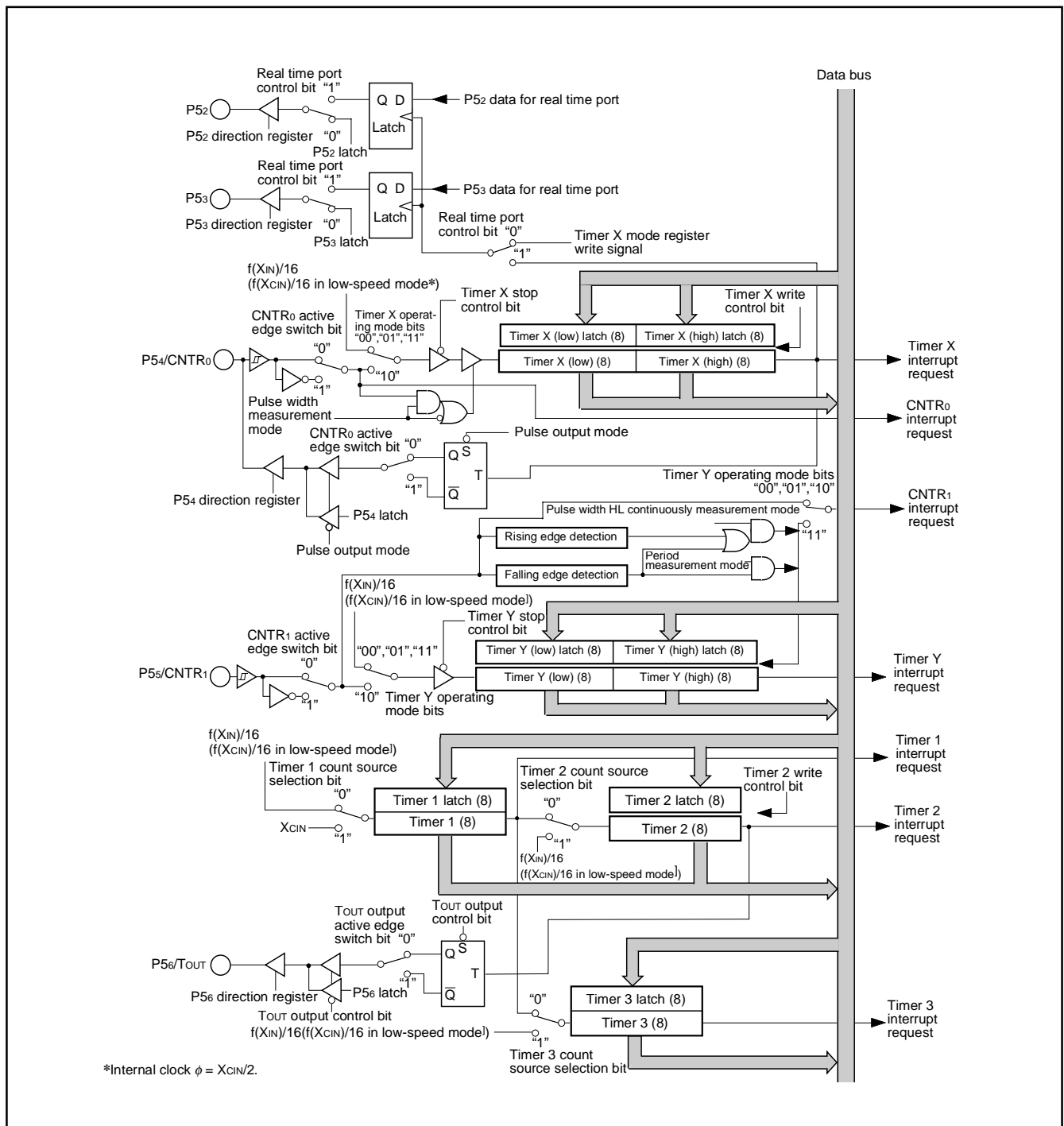


Fig. 19 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Pulse output mode

Each time the timer underflows, a signal output from the CNTR0 pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to output mode.

(3) Event counter mode

The timer counts signals input through the CNTR0 pin. Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

(4) Pulse width measurement mode

The count source is $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode). If CNTR0 active edge switch bit is "0", the timer counts while the input signal of CNTR0 pin is at "H". If it is "1", the timer counts while the input signal of CNTR0 pin is at "L". When using a timer in this mode, set the corresponding port P54 direction register to input mode.

●Timer X Write Control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.

If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.

If the value is written in latch only, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

●Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports P52 and P53 each time the timer X underflows. (However, if the real time port control bit is changed from "0" to "1" after set of the real time port data, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.

Before using this function, set the corresponding port direction registers to output mode.

■Note on CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

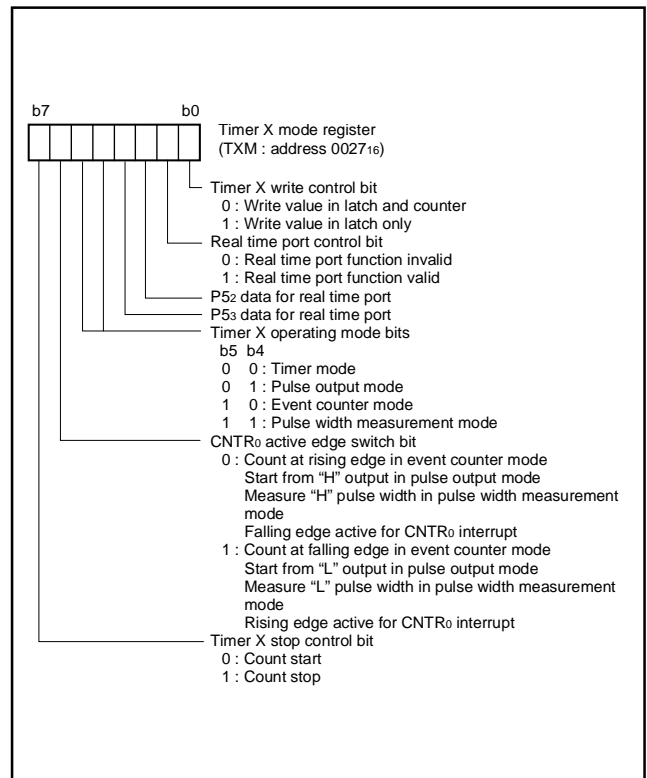


Fig. 20 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Period measurement mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

(3) Event counter mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

(4) Pulse width HL continuously measurement mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

■Note on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

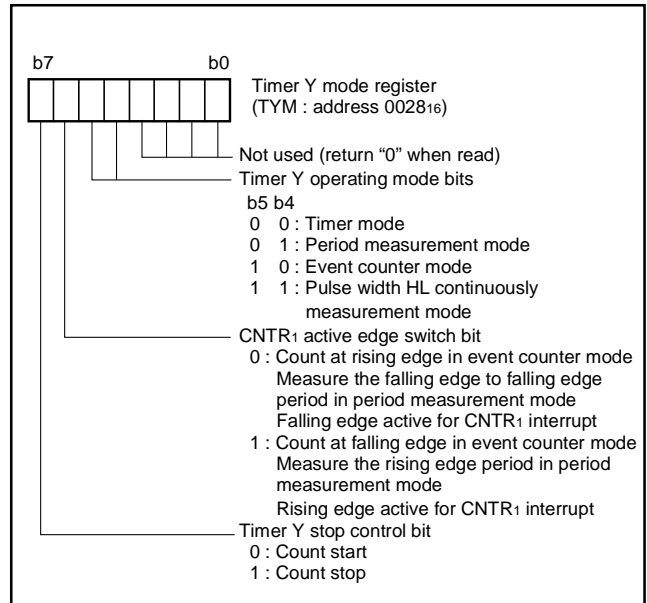


Fig. 21 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer. Therefore, rewrite the value of timer whenever the count source is changed.

●Timer 2 Write Control

If the timer 2 write control bit is "0", when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is "1", when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

●Timer 2 Output Control

When the timer 2 (TOUT) is output enabled, an inversion signal from pin TOUT is output each time timer 2 underflows.

In this case, set the port P5₆ shared with the port TOUT to the output mode.

■Note on Timer 1 to Timer 3

When the count source of timers 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

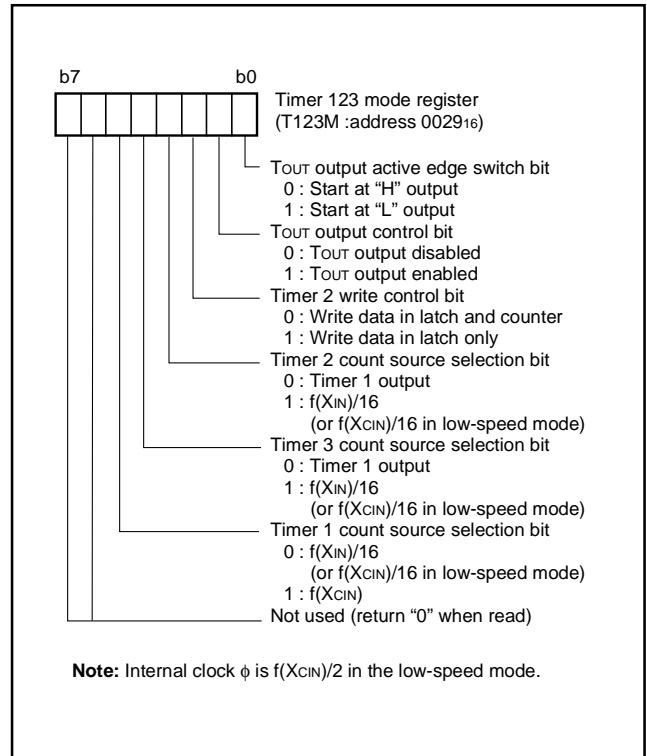


Fig. 22 Structure of timer 123 mode register

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer regis-

ter, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

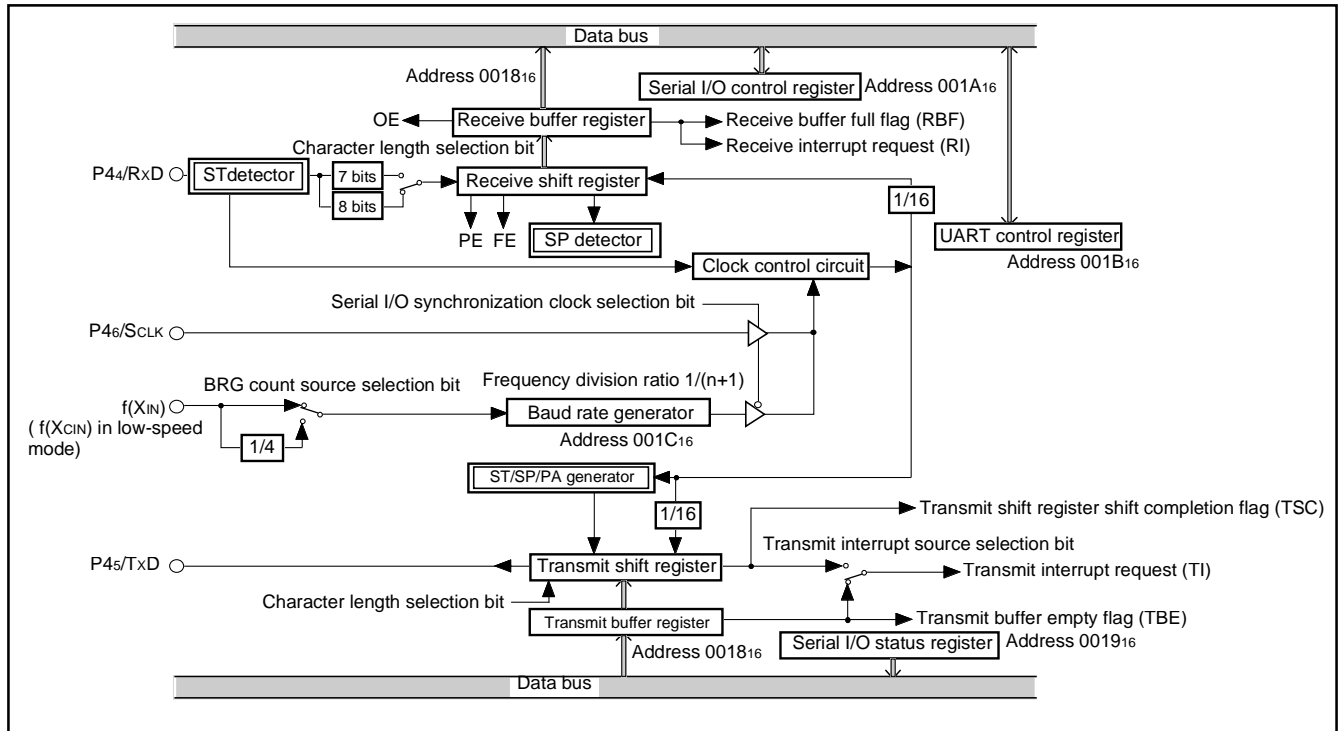
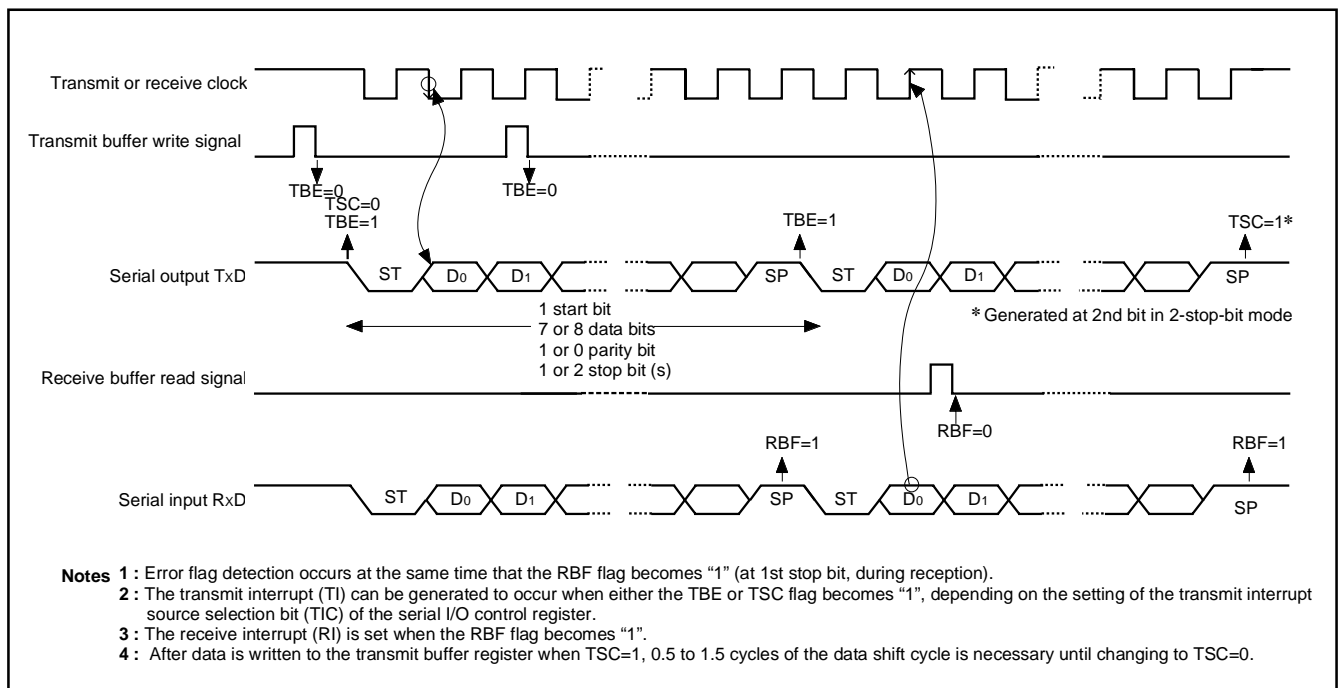


Fig. 25 Block diagram of UART serial I/O



- Notes**
- 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
 - 2 : The transmit interrupt (TI) can be generated to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
 - 3 : The receive interrupt (RI) is set when the RBF flag becomes "1".
 - 4 : After data is written to the transmit buffer register when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 26 Operation of UART serial I/O function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018₁₆

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is "0".

[Serial I/O Status Register (SIOSTS)] 0019₁₆

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O Control Register (SIOCON)] 001A₁₆

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON)] 001B₁₆

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P45/TxD pin.

[Baud Rate Generator (BRG)] 001C₁₆

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

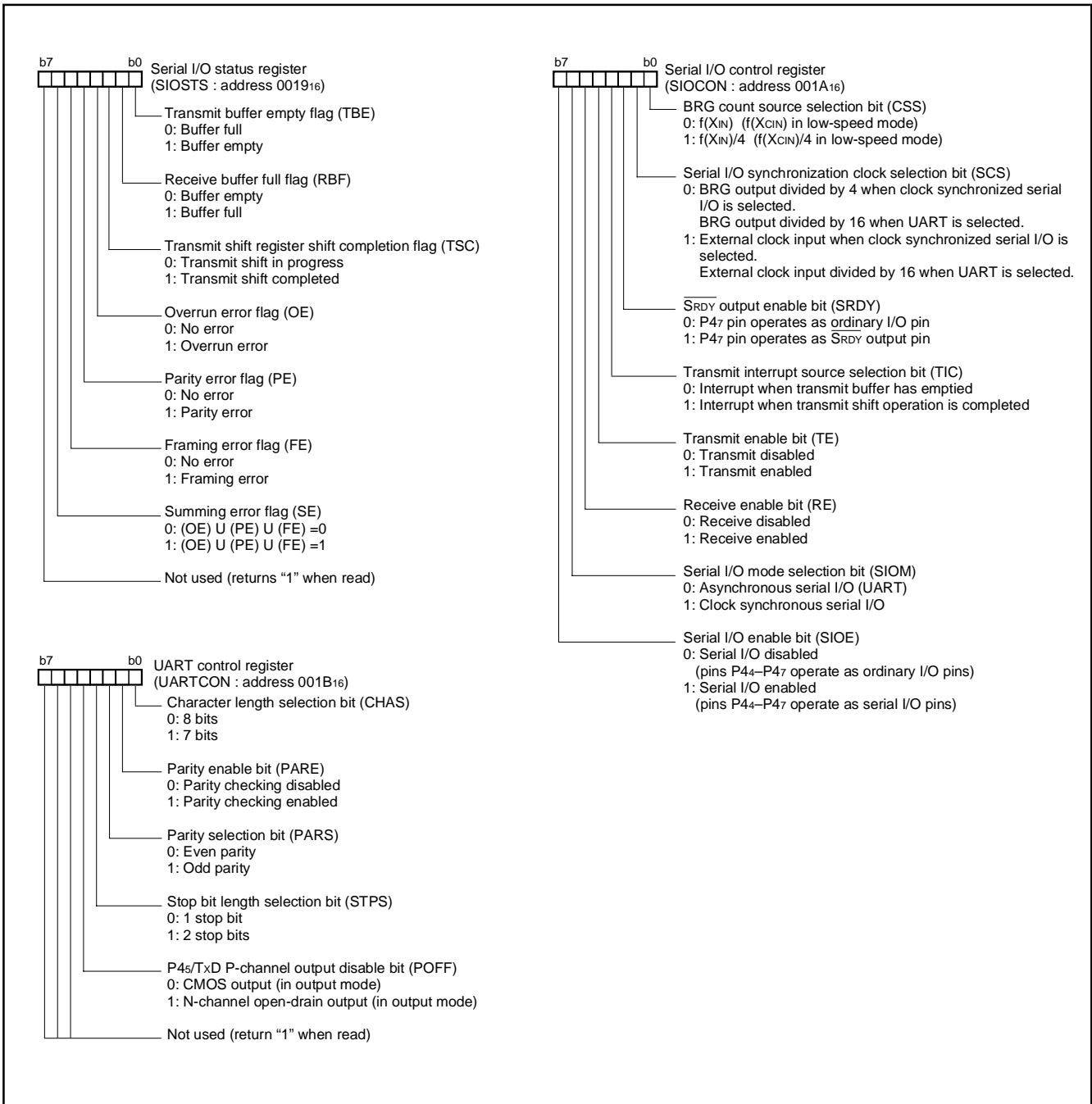


Fig. 27 Structure of serial I/O control registers

A-D CONVERTER

The functional blocks of the A-D converter are described below.

[A-D Conversion Register (AD)] 003516

The A-D conversion register is a read-only register that contains the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

[A-D Control Register (ADCON)] 003416

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion. Bit 4 controls the transistor which breaks the through current of the resistor ladder. When bit 5, which is the AD external trigger valid bit, is set to "1", this bit enables A-D conversion even by a falling edge of an ADT input. Set ports which share with ADT pins to input when using an A-D external trigger.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports P67/AN7–P60/AN0.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f(XIN) to at least 500kHz during A-D conversion.

Use the clock divided from the main clock XIN as the internal clock ϕ .

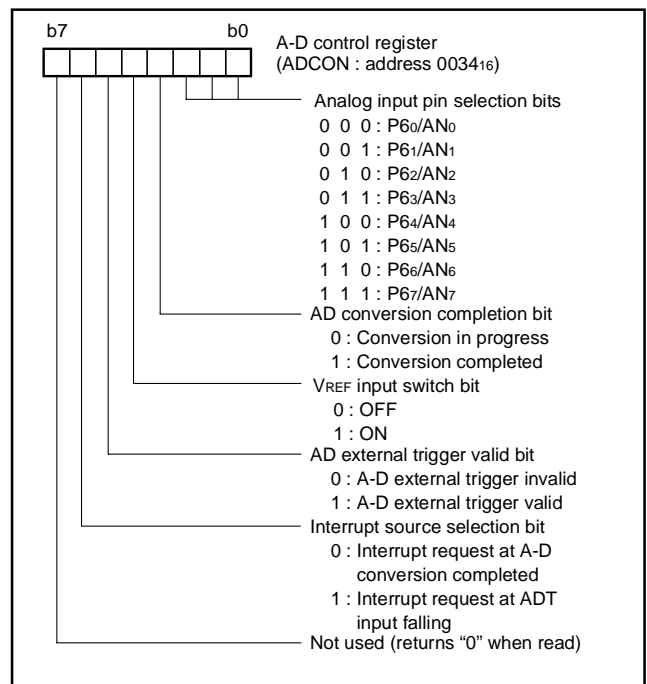


Fig. 28 Structure of A-D control register

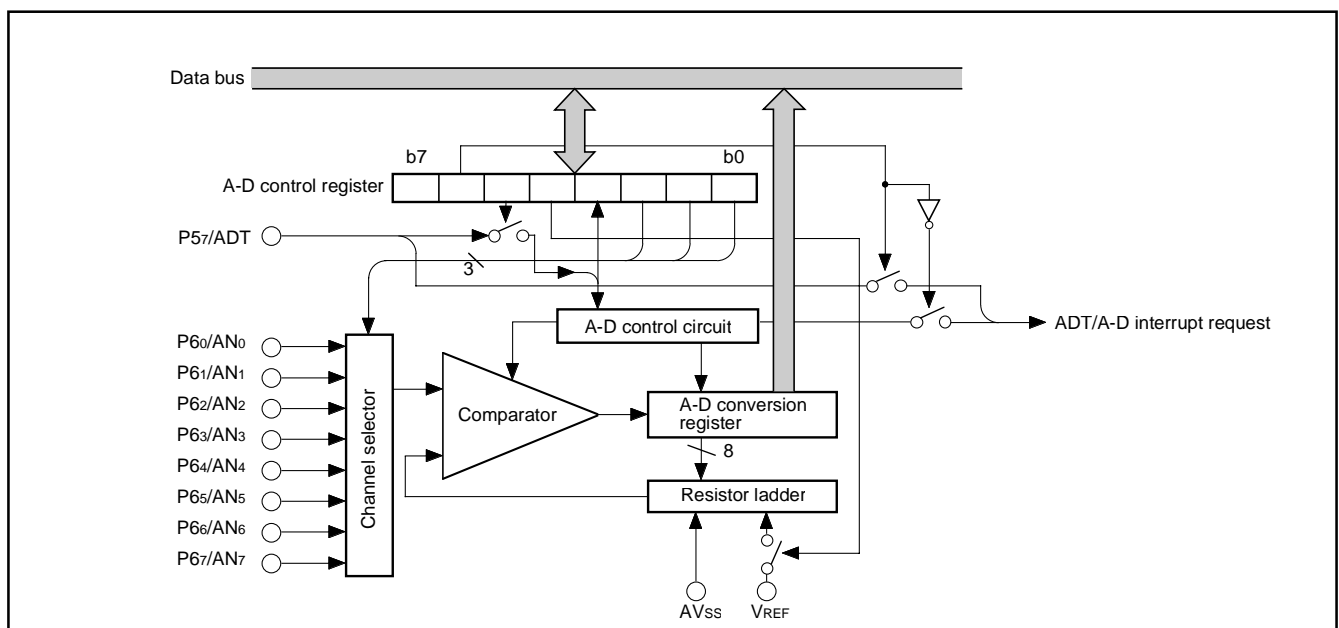


Fig. 29 A-D converter block diagram

LCD DRIVE CONTROL CIRCUIT

The 3825 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output enable register
- LCD mode register
- Voltage multiplier
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 40 segment output pins and 4 common output pins can be used.

Up to 160 pixels can be controlled for LCD display. When the LCD

enable bit is set to "1" after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 10. Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
2	80 dots or 8 segment LCD 10 digits
3	120 dots or 8 segment LCD 15 digits
4	160 dots or 8 segment LCD 20 digits

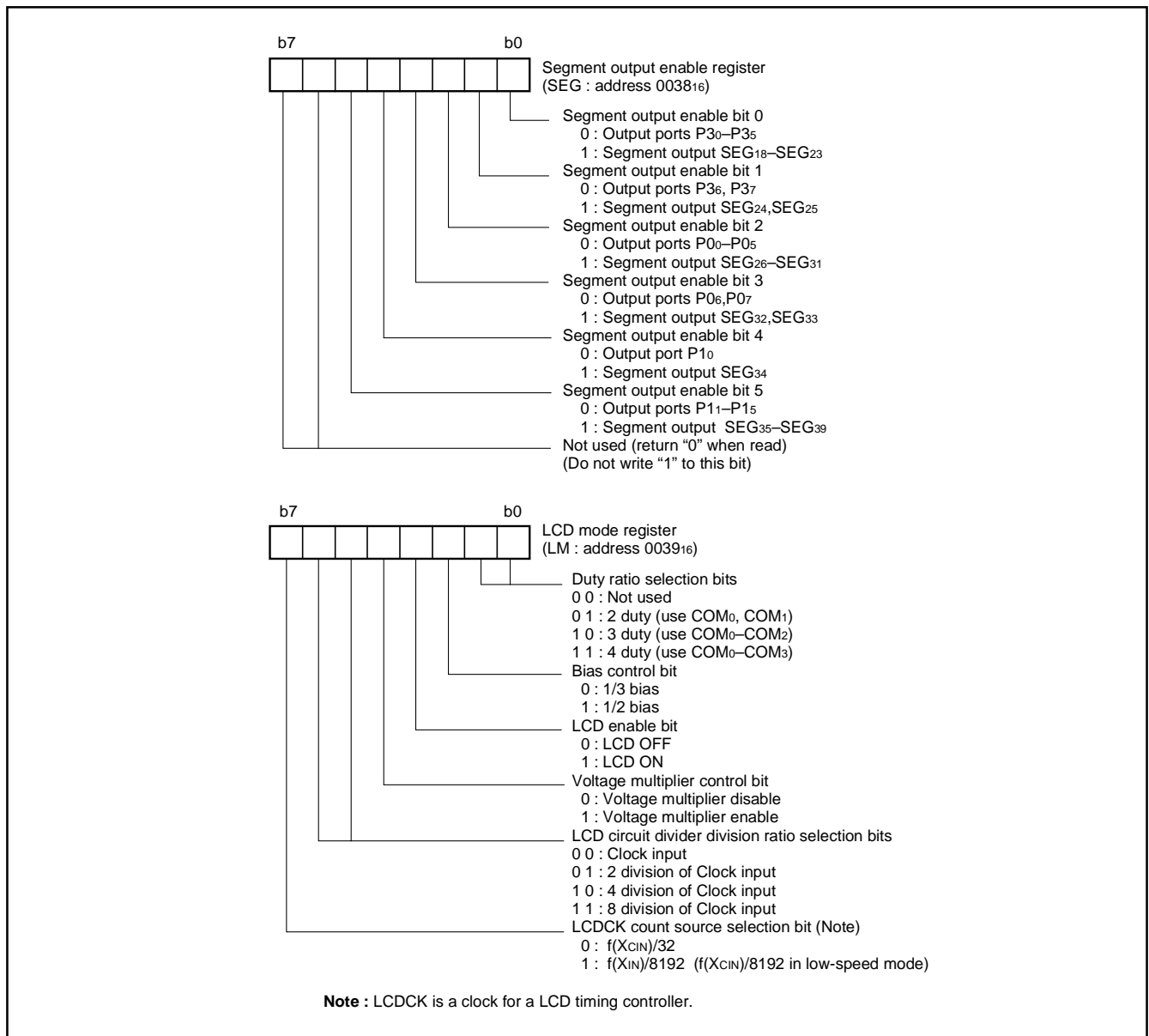


Fig. 30 Structure of segment output enable register and LCD mode register

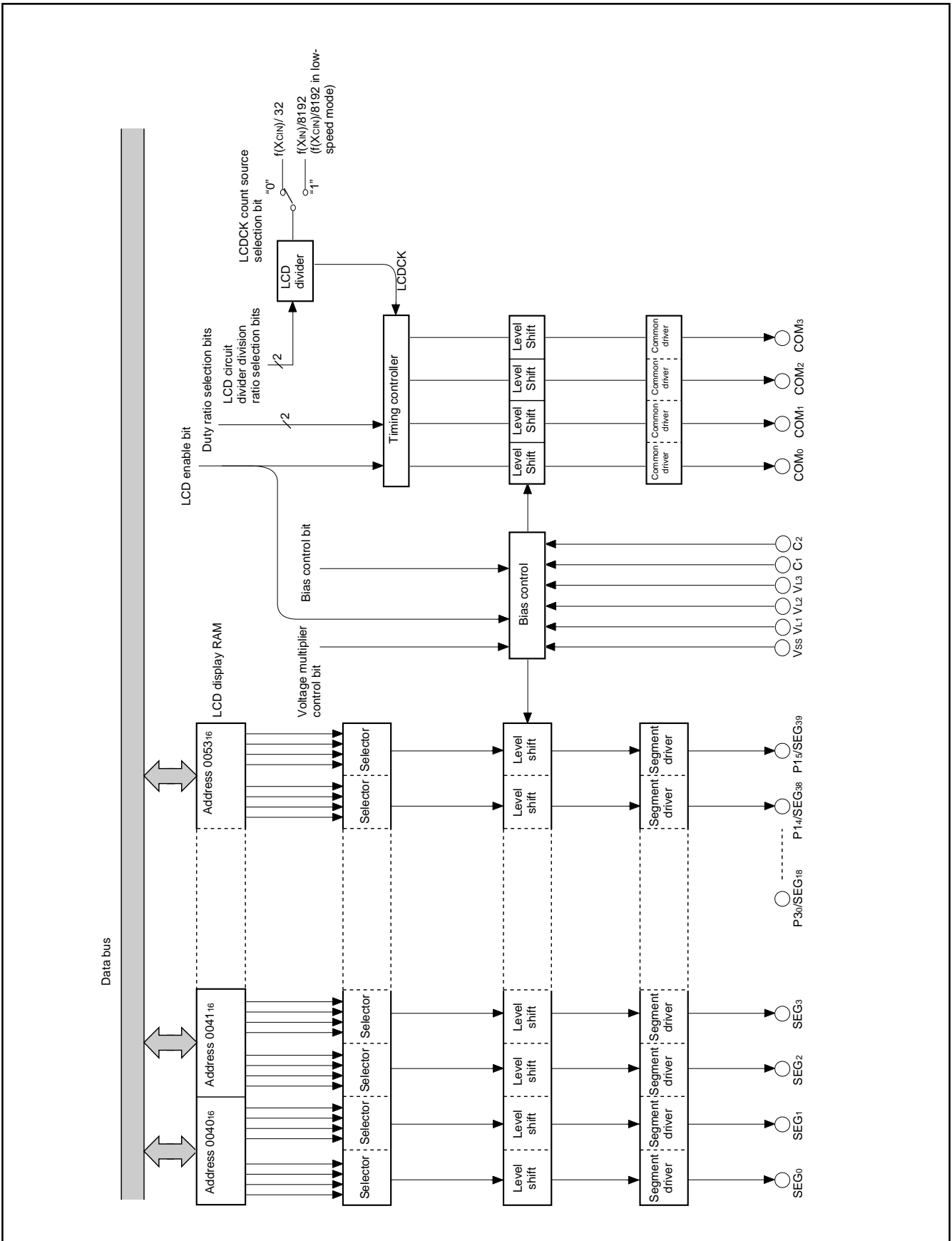


Fig. 31 Block diagram of LCD controller/driver

Voltage Multiplier (3 Times)

The voltage multiplier performs threefold boosting. This circuit inputs a reference voltage for boosting from LCD power input pin VL1. (However, when using a 1/2 bias, connect VL1 and VL2 and apply voltage by external resistor division.)

The voltage multiplier control bit (bit 4 of the LCD mode register) controls the voltage multiplier.

When voltage is input to the VL1 pin during operating the voltage multiplier, voltage that is twice as large as VL1 occurs at the VL2 pin, and voltage that is three times as large as VL1 occurs at the VL3 pin.

When using the voltage multiplier; after applying $1.3\text{ V} \leq \text{Voltage} \leq 2.3\text{ V}$ to the VL1 pin, set the voltage multiplier control bit to "1" to select the voltage multiplier enable.

When not using the voltage multiplier, apply proper voltage to the LCD power input pins (VL1-VL3).

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (VL1-VL3), apply the voltage shown in Table 11 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM0-COM3) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

Table 11. Bias control and applied voltage to VL1-VL3

Bias value	Voltage value
1/3 bias	VL3=VLCD VL2=2/3 VLCD VL1=1/3 VLCD
1/2 bias	VL3=VLCD VL2=VL1=1/2 VLCD

Note : VLCD is the maximum value of supplied voltage for the LCD panel.

Table 12. Duty ratio control and common pins used

Duty ratio	Duty ratio selection bits		Common pins used
	Bit 1	Bit 0	
2	0	1	COM0, COM1 (Note 1)
3	1	0	COM0-COM2 (Note 2)
4	1	1	COM0-COM3

Notes 1: COM2 and COM3 are open.

2: COM3 is open.

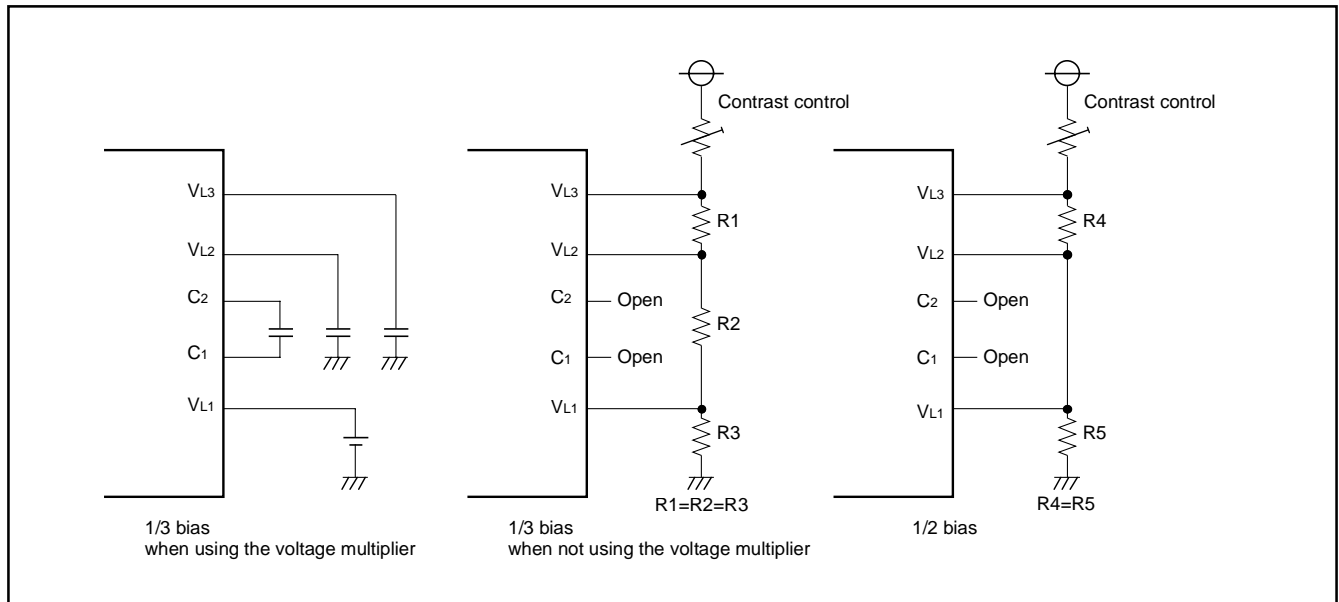


Fig. 32 Example of circuit at each bias

LCD Display RAM

Address 0040₁₆ to 0053₁₆ is the designated RAM for the LCD display. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{\text{duty ratio}}$$

Address	Bit							
	7	6	5	4	3	2	1	0
	COM ₃	COM ₂	COM ₁	COM ₀	COM ₃	COM ₂	COM ₁	COM ₀
0040 ₁₆			SEG ₁					SEG ₀
0041 ₁₆			SEG ₃					SEG ₂
0042 ₁₆			SEG ₅					SEG ₄
0043 ₁₆			SEG ₇					SEG ₆
0044 ₁₆			SEG ₉					SEG ₈
0045 ₁₆			SEG ₁₁					SEG ₁₀
0046 ₁₆			SEG ₁₃					SEG ₁₂
0047 ₁₆			SEG ₁₅					SEG ₁₄
0048 ₁₆			SEG ₁₇					SEG ₁₆
0049 ₁₆			SEG ₁₉					SEG ₁₈
004A ₁₆			SEG ₂₁					SEG ₂₀
004B ₁₆			SEG ₂₃					SEG ₂₂
004C ₁₆			SEG ₂₅					SEG ₂₄
004D ₁₆			SEG ₂₇					SEG ₂₆
004E ₁₆			SEG ₂₉					SEG ₂₈
004F ₁₆			SEG ₃₁					SEG ₃₀
0050 ₁₆			SEG ₃₃					SEG ₃₂
0051 ₁₆			SEG ₃₅					SEG ₃₄
0052 ₁₆			SEG ₃₇					SEG ₃₆
0053 ₁₆			SEG ₃₉					SEG ₃₈

Fig. 33 LCD display RAM map

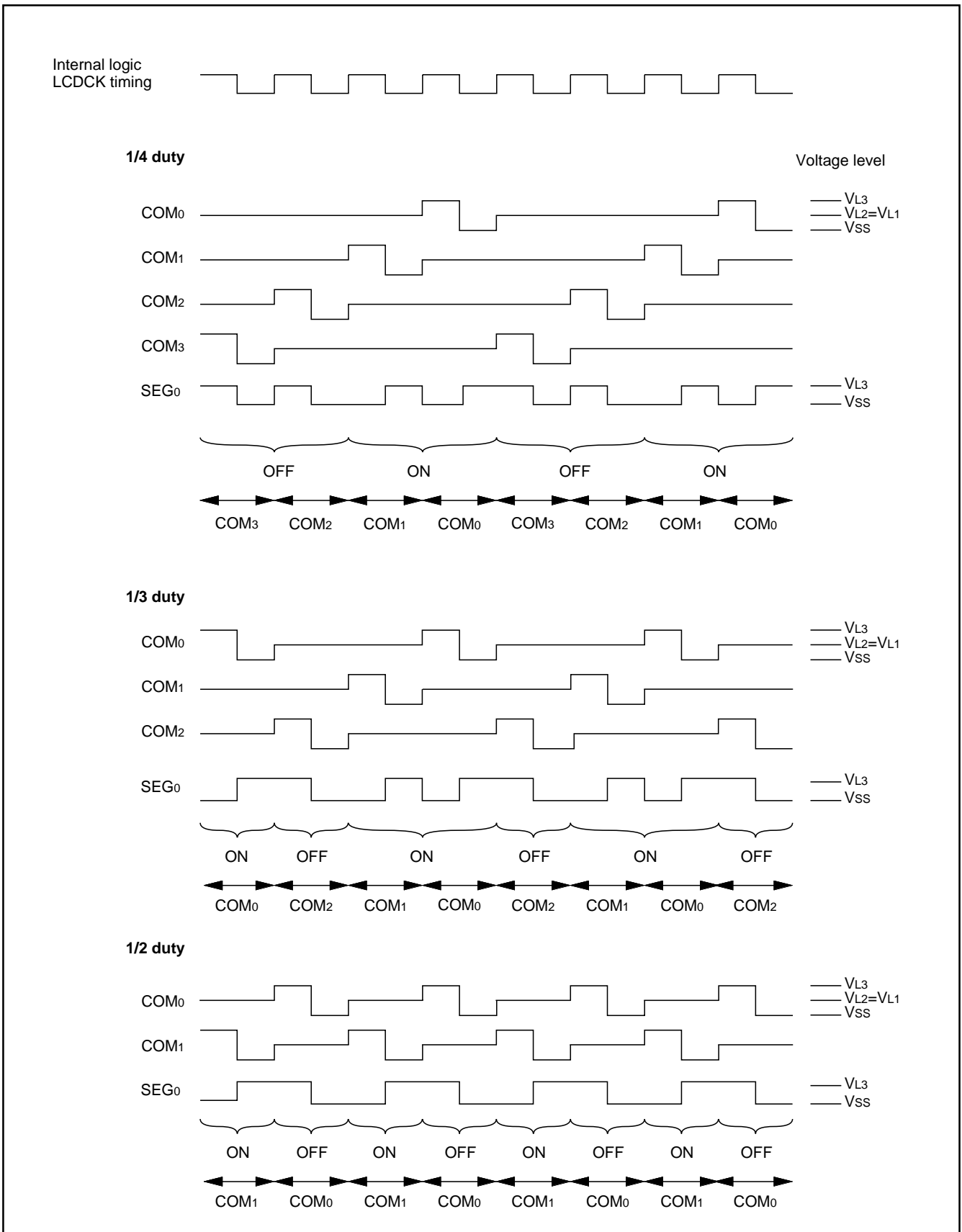


Fig. 34 LCD drive waveform (1/2 bias)

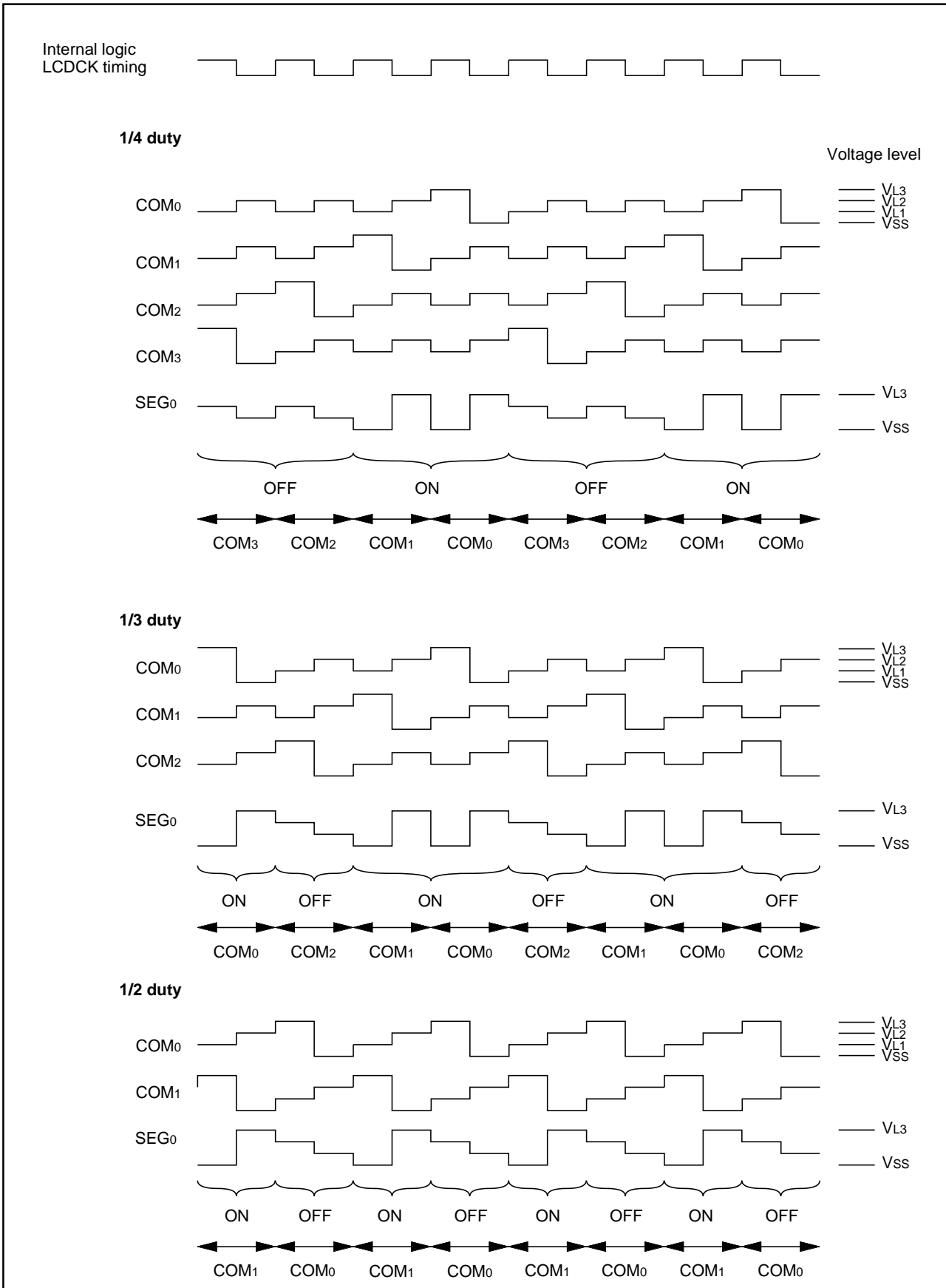


Fig. 35 LCD drive waveform (1/3 bias)

CLOCK OUTPUT FUNCTION

Input/output ports P40 and P41 can output clock. The input/output ports and clock output function are put under double function controlled by the clock output control register (address 002A16).

Selection of Input/Output Ports and Clock Output Function

Bits 0 and 1 of the clock output control register can select between the input/output ports and the clock output function.

When selecting the clock output function, clocks are output while the direction register of ports P40 and P41 are set to output.

At the next cycle of rewriting the clock output control bit, P40 is switched between the port output and the clock output.

In synchronization with the fall of the clock (resulting from dividing XIN by 5) on rewriting the clock output control bit, P41 is switched between the port output and the clock output.

Selection of Output Clock Frequency

Bit 2 (output clock frequency selection bit) of the clock output control register selects an output clock frequency.

When setting the output clock frequency selection bit to "0", port P40 becomes the frequency of $f(XIN)$ and port P41 becomes the frequency of $f(XIN)/5$.

At this time, the output pulse of port P40 depends on the XIN input pulse, while the output pulse of port P41 has duty ratio of about 40%.

When setting the output clock frequency selection bit to "1", port P40 becomes the frequency of $f(XIN)/2$ and port P41 becomes the frequency of $f(XIN)/10$. At this time, the output pulses of both ports P40 and P41 have duty ratio of 50%.

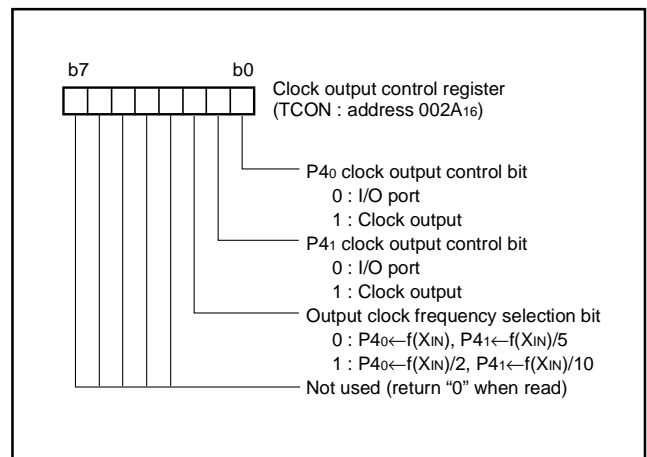


Fig. 36 Structure of clock output control register

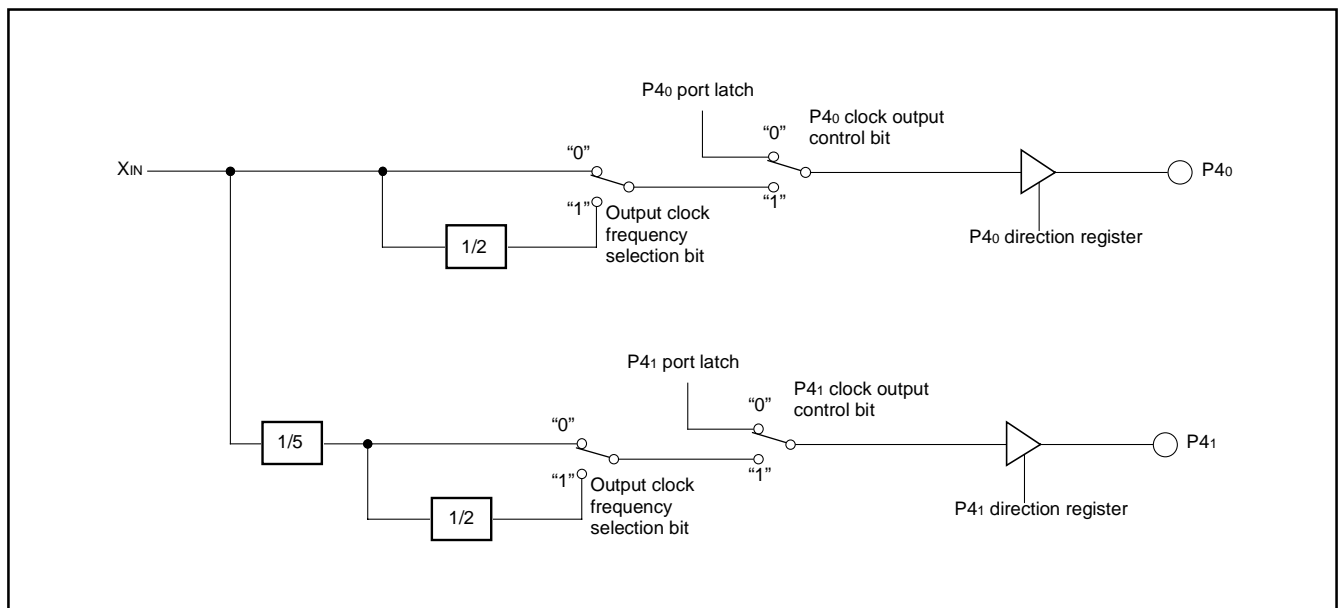


Fig. 37 Clock output function block diagram

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between $V_{CC(\text{min.})}$ and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFD_{16} (high-order byte) and address FFC_{16} (low-order byte). Make sure that the reset input voltage meets V_{IL} spec. when a power source voltage passes $V_{CC(\text{min.})}$.

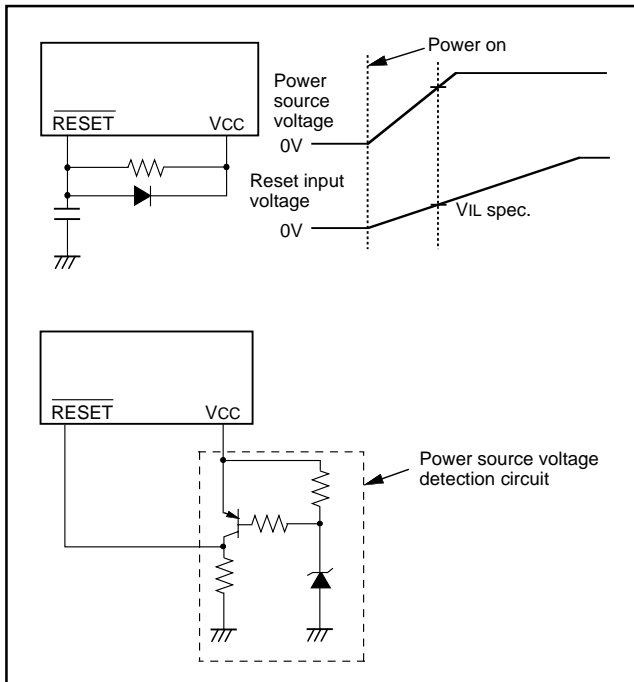


Fig. 38 Example of reset circuit

	Address	Register contents
(1) Port P0	0000 ₁₆	00 ₁₆
(2) Port P1	0002 ₁₆	00 ₁₆
(3) Port P1 output control register	0003 ₁₆	00 ₁₆
(4) Port P2	0004 ₁₆	00 ₁₆
(5) Port P2 direction register	0005 ₁₆	00 ₁₆
(6) Port P3	0006 ₁₆	00 ₁₆
(7) Port P4	0008 ₁₆	00 ₁₆
(8) Port P4 direction register	0009 ₁₆	00 ₁₆
(9) Port P5	000A ₁₆	00 ₁₆
(10) Port P5 direction register	000B ₁₆	00 ₁₆
(11) Port P6	000C ₁₆	00 ₁₆
(12) Port P6 direction register	000D ₁₆	00 ₁₆
(13) Port P7	000E ₁₆	00 ₁₆
(14) Port P7 direction register	000F ₁₆	00 ₁₆
(15) Port P8	0010 ₁₆	00 ₁₆
(16) Port P8 direction register	0011 ₁₆	00 ₁₆
(17) PULL register A	0016 ₁₆	01 ₁₆
(18) PULL register B	0017 ₁₆	00 ₁₆
(19) Serial I/O status register	0019 ₁₆	1 0 0 0 0 0 0 0
(20) Serial I/O control register	001A ₁₆	00 ₁₆
(21) UART control register	001B ₁₆	1 1 1 0 0 0 0 0
(22) Timer X (low)	0020 ₁₆	FF ₁₆
(23) Timer X (high)	0021 ₁₆	FF ₁₆
(24) Timer Y (low)	0022 ₁₆	FF ₁₆
(25) Timer Y (high)	0023 ₁₆	FF ₁₆
(26) Timer 1	0024 ₁₆	FF ₁₆
(27) Timer 2	0025 ₁₆	01 ₁₆
(28) Timer 3	0026 ₁₆	FF ₁₆
(29) Timer X mode register	0027 ₁₆	00 ₁₆
(30) Timer Y mode register	0028 ₁₆	00 ₁₆
(31) Timer 123 mode register	0029 ₁₆	00 ₁₆
(32) Clock output control register	002A ₁₆	00 ₁₆
(33) A-D control register	0034 ₁₆	0 0 0 0 0 1 0 0
(34) Segment output enable register	0038 ₁₆	00 ₁₆
(35) LCD mode register	0039 ₁₆	00 ₁₆
(36) Interrupt edge selection register	003A ₁₆	00 ₁₆
(37) CPU mode register	003B ₁₆	0 1 0 0 1 0 0 0
(38) Interrupt request register 1	003C ₁₆	00 ₁₆
(39) Interrupt request register 2	003D ₁₆	00 ₁₆
(40) Interrupt control register 1	003E ₁₆	00 ₁₆
(41) Interrupt control register 2	003F ₁₆	00 ₁₆
(42) Processor status register	(PS)	X X X X X 1 X X
(43) Program counter	(PC+)	Contents of address FFD_{16}
	(PC-)	Contents of address FFC_{16}

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
X : Undefined

Fig. 39 Internal state of microcomputer immediately after reset

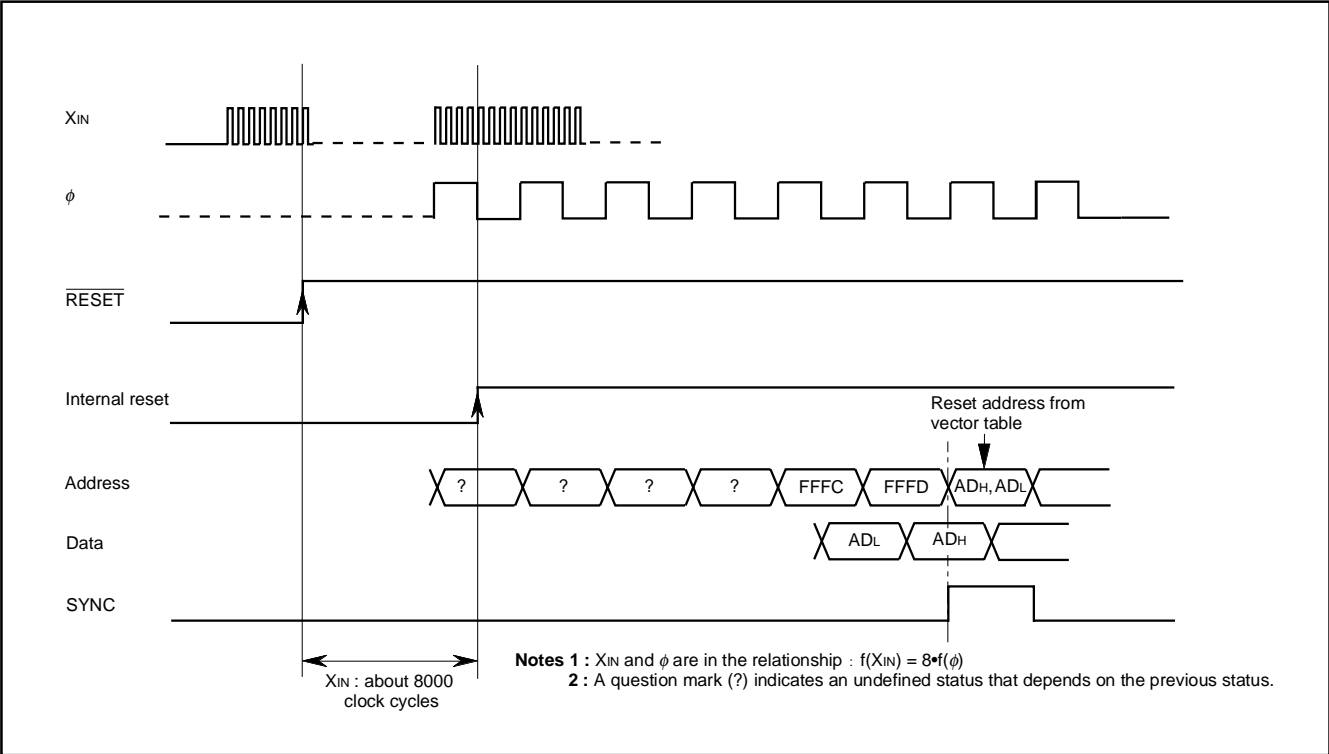


Fig. 40 Reset sequence

CLOCK GENERATING CIRCUIT

The 3825 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub-clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Immediately after power-on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control

(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8.

After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

- The internal clock ϕ is half the frequency of XCIN.
- A low-power consumption operation can be realized by stopping the main clock XIN in this mode. To stop the main clock, set bit 5 of the CPU mode register to "1".

When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.

Note: If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power-on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency in the condition that $f(XIN) > 3 \cdot f(XCIN)$.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either XIN or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2.

The bits of the timer 123 mode register except bit 4 are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction.

Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of XIN and XCIN are the same as the state before the executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

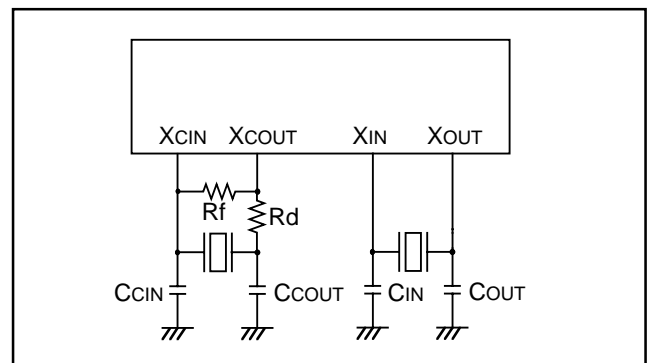


Fig. 41 Ceramic resonator circuit

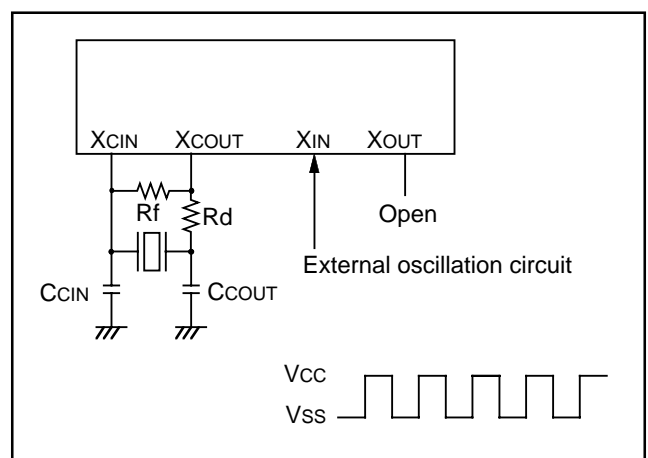


Fig. 42 External clock input circuit

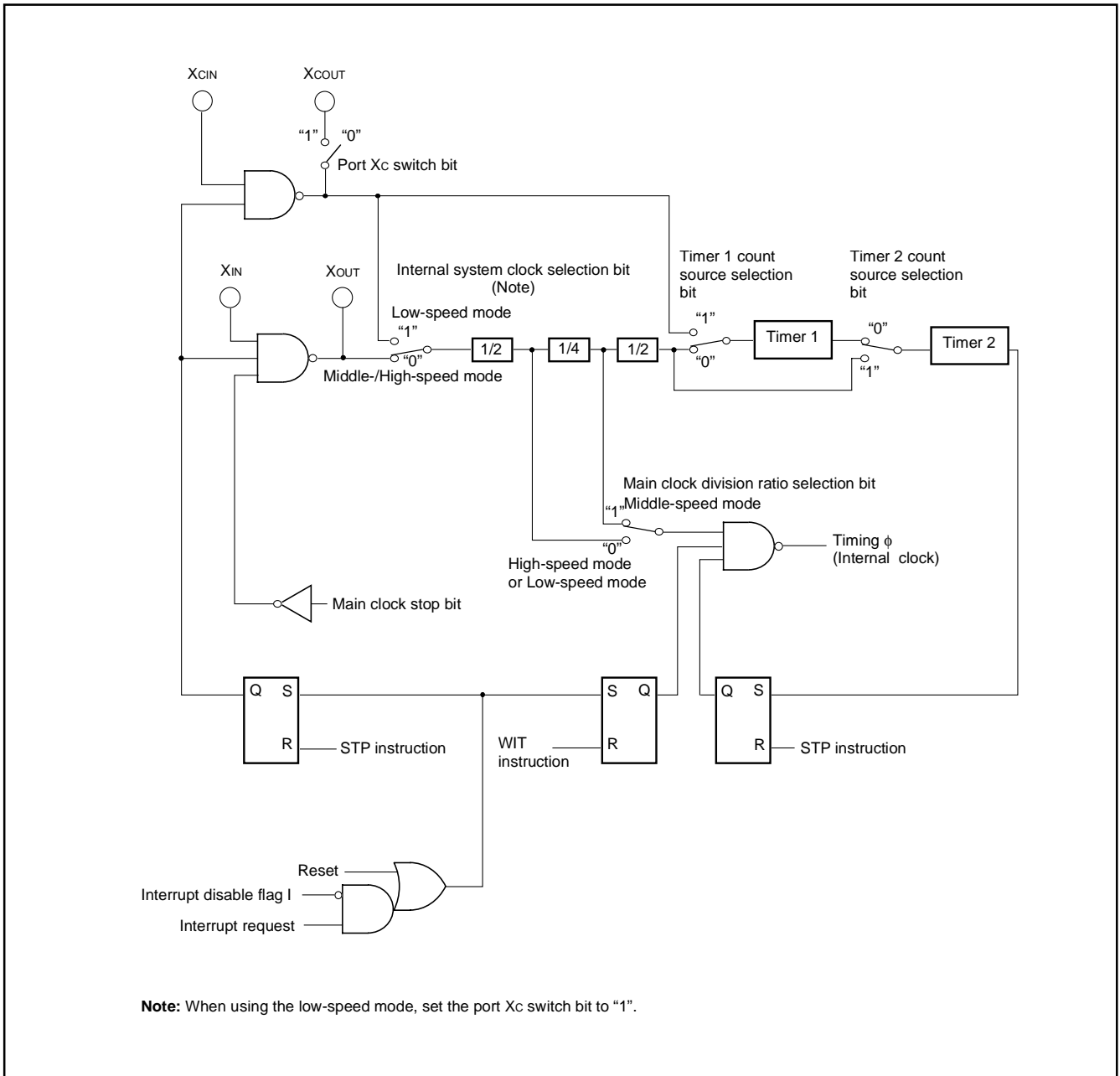


Fig. 43 Clock generating circuit block diagram

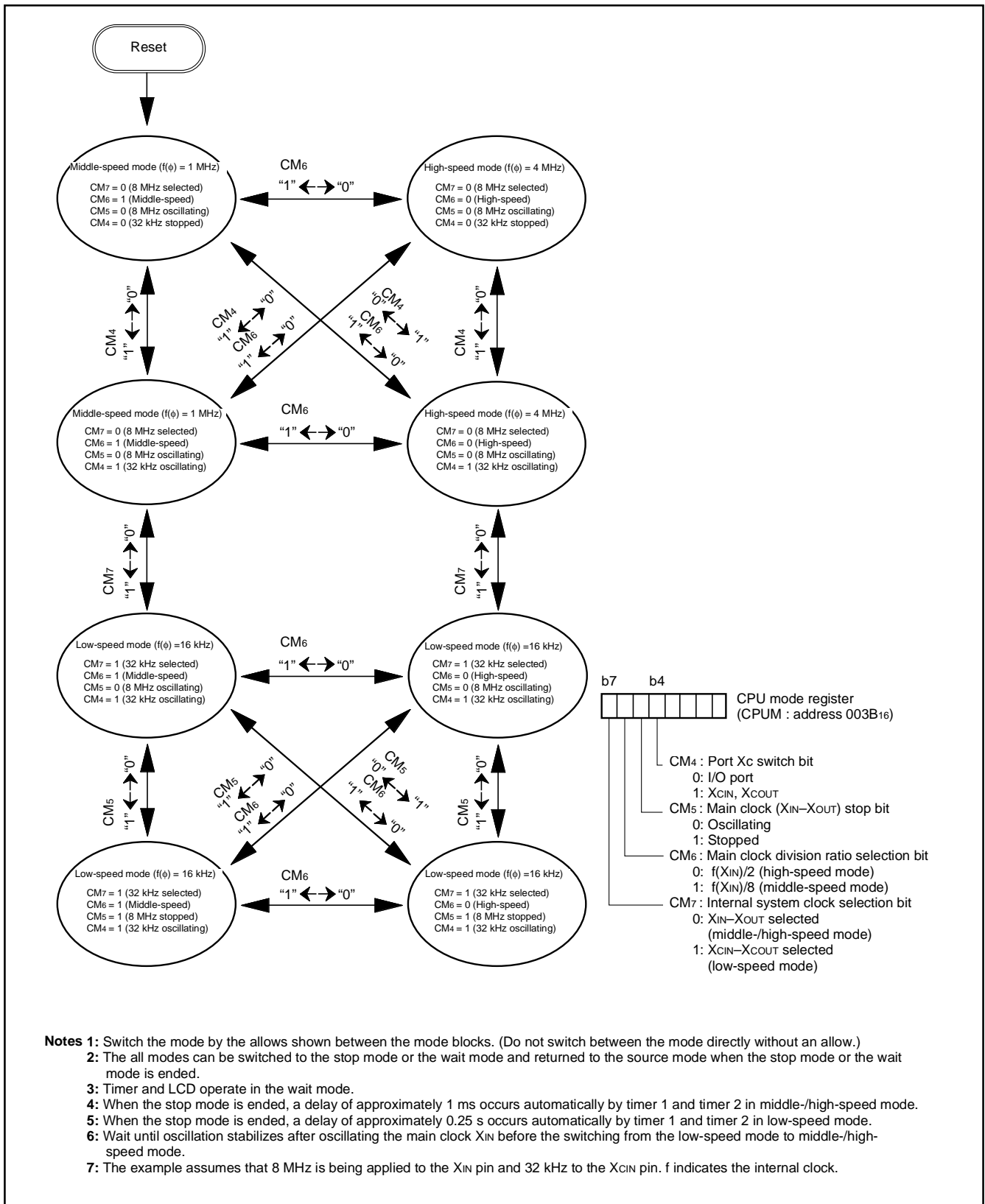


Fig. 44 State transitions of internal clock ϕ

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution.

In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n + 1)$.

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.

The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".

Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(\text{XIN})$ is at least 500kHz during an A-D conversion. Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the XIN frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- 1.Mask ROM Order Confirmation Form*
- 2.Mark Specification Form*
- 3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

*For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage (<http://www.infocom.mesc.co.jp/indexe.htm>).

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 13. Programming adapter

Package	Name of Programming Adapter
100PFB-A	PCA4738H-100A
100P6Q-A	PCA4738G-100A
100P6S-A	PCA4738F-100A
100D0	PCA4738L-100A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 45 is recommended to verify programming.

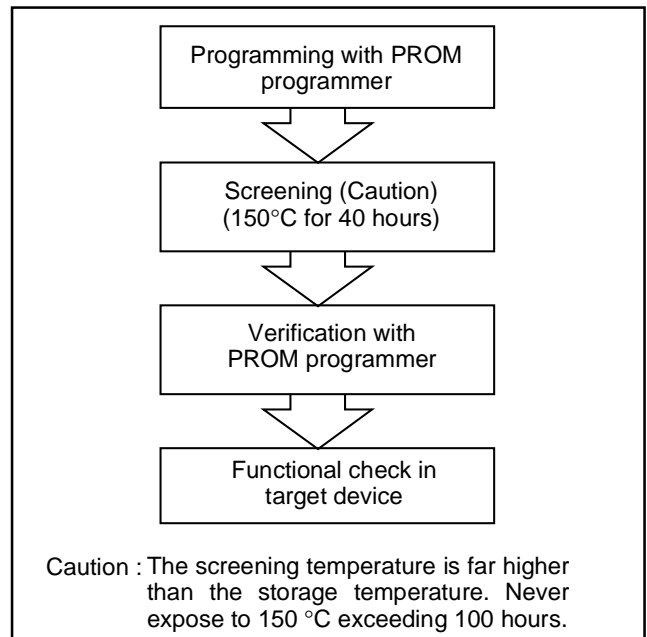


Fig. 45 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS (Standard, One Time PROM Version)

Table 14. Absolute maximum ratings (Standard, One time PROM version)

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage	All voltages are based on VSS. Output transistors are cut off.	-0.3 to 7.0	V
VI	Input voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P80, P81		-0.3 to VCC +0.3	V
VI	Input voltage P70-P77		-0.3 to VCC +0.3	V
VI	Input voltage VL1		-0.3 to VL2	V
VI	Input voltage VL2		VL1 to VL3	V
VI	Input voltage VL3		VL2 to 7.0	V
VI	Input voltage C1, C2		-0.3 to 7.0	V
VI	Input voltage RESET, XIN		-0.3 to VCC +0.3	V
VO	Output voltage C1, C2		-0.3 to 7.0	V
VO	Output voltage P00-P07, P10-P15, P30-P37		At output port At segment output	-0.3 to VCC -0.3 to VL3
VO	Output voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81		-0.3 to VCC +0.3	V
VO	Output voltage VL3		-0.3 to 7.0	V
VO	Output voltage VL2, SEG0-SEG17		-0.3 to VL3	V
VO	Output voltage XOUT		-0.3 to VCC +0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		-20 to 85	°C
Tstg	Storage temperature		-40 to 125	°C

Table 15. Recommended operating conditions (Standard, One time PROM version)

(VCC = 2.5 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage	High-speed mode f(XIN) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(XIN) = 8 MHz	2.5	5.0	5.5	
		Low-speed mode	2.5	5.0	5.5	
VSS	Power source voltage		0		V	
VREF	A-D conversion reference voltage		2.0	VCC	V	
AVSS	Analog power source voltage		0		V	
VIA	Analog input voltage AN0-AN7		AVSS	VCC	V	
VIH	"H" input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60-P67, P70-P77, P80, P81 (CM4=0)	0.7VCC		VCC	V
VIH	"H" input voltage	P20-P27, P42-P44, P46, P50, P51, P54, P55, P57	0.8VCC		VCC	V
VIH	"H" input voltage	RESET	0.8VCC		VCC	V
VIH	"H" input voltage	XIN	0.8VCC		VCC	V
VIL	"L" input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60-P67, P70-P77, P80, P81 (CM4=0)	0		0.3VCC	V
VIL	"L" input voltage	P20-P27, P42-P44, P46, P50, P51, P54, P55, P57	0		0.2VCC	V
VIL	"L" input voltage	RESET	0		0.2VCC	V
VIL	"L" input voltage	XIN	0		0.2VCC	V

Table 16. Recommended operating conditions (Standard, One time PROM version)(V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			-20	mA
ΣIOH(peak)	"H" total peak output current P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 1)			-20	mA
ΣIOL(peak)	"L" total peak output current P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			20	mA
ΣIOL(peak)	"L" total peak output current P40–P47, P50–P57, P60–P67, P80, P81 (Note 1)			20	mA
ΣIOL(peak)	"L" total peak output current P71–P77 (Note 1)			40	mA
ΣIOH(avg)	"H" total average output current P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			-10	mA
ΣIOH(avg)	"H" total average output current P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 1)			-10	mA
ΣIOL(avg)	"L" total average output current P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			10	mA
ΣIOL(avg)	"L" total average output current P40–P47, P50–P57, P60–P67, P80, P81 (Note 1)			10	mA
ΣIOL(avg)	"L" total average output current P71–P77 (Note 1)			20	mA
IOH(peak)	"H" peak output current P00–P07, P10–P15, P30–P37 (Note 2)			-0.5	mA
IOH(peak)	"H" peak output current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 2)			-5.0	mA
IOL(peak)	"L" peak output current P00–P07, P10–P15, P30–P37 (Note 2)			5.0	mA
IOL(peak)	"L" peak output current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81 (Note 2)			10	mA
IOH(avg)	"H" average output current P00–P07, P10–P15, P30–P37 (Note 3)			-0.1	mA
IOH(avg)	"H" average output current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 3)			-2.5	mA
IOL(avg)	"L" average output current P00–P07, P10–P15, P30–P37 (Note 3)			2.5	mA
IOL(avg)	"L" average output current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 3)			5.0	mA
f(CNTR ₀) f(CNTR ₁)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ V _{CC} ≤ 5.5 V)		4.0	MHz
		(V _{CC} ≤ 4.0 V)		(2×V _{CC}) -4	MHz
f(X _{IN})	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ V _{CC} ≤ 5.5 V)		8.0	MHz
		High-speed mode (V _{CC} ≤ 4.0 V)		(4×V _{CC}) -8	MHz
		Middle-speed mode		8.0	MHz
f(X _{CIN})	Sub-clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Note 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the oscillation frequency has a duty cycle of 50%.

5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 17. Electrical characteristics (Standard, One time PROM version)

(VCC =4.0 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
VOH	“H” output voltage P00–P07, P10–P15, P30–P37	IOH = -0.1 mA	VCC-2.0			V	
		IOH = -25 μA	VCC-1.0			V	
		VCC = 2.5 V					
VOH	“H” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	IOH = -5 mA	VCC-2.0			V	
		IOH = -1.25 mA	VCC-0.5			V	
		IOH = -1.25 mA	VCC-1.0			V	
VOL	“L” output voltage P00–P07, P10–P15, P30–P37	IOL = 5 mA			2.0	V	
		IOL = 1.25 mA			0.5	V	
		IOL = 1.25 mA			1.0	V	
VOL	“L” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	IOL = 10 mA			2.0	V	
		IOL = 2.5 mA			0.5	V	
		IOL = 2.5 mA			1.0	V	
VT+ – VT-	Hysteresis	INT0–INT3, ADT, CNTR0, CNTR1, P20–P27		0.5		V	
VT+ – VT-	Hysteresis	SCLK, RXD		0.5		V	
VT+ – VT-	Hysteresis	RESET	RESET: VCC=2.5 V to 5.5 V	0.5		V	
IiH	“H” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81	Vi = VCC		5.0	μA	
IiH	“H” input current	RESET	Vi = VCC		5.0	μA	
IiH	“H” input current	XIN	Vi = VCC	4.0		μA	
IiL	“L” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81	Vi = VSS Pull-ups “off”			-5.0	μA
		VCC = 5 V, Vi = VSS Pull-ups “on”	-30	-70	-140	μA	
		VCC = 3 V, Vi = VSS Pull-ups “on”	-6.0	-25	-45	μA	
IiL	“L” input current	P70			-5.0	μA	
IiL	“L” input current	RESET	Vi = VSS		-5.0	μA	
IiL	“L” input current	XIN	Vi = VSS	-4.0		μA	
ILOAD	Output load current P00–P07, P10–P15, P30–P37	VCC = 5.0 V, Vo = VCC, Pull-downs “on” Output transistors “off”	30	70	140	μA	
		VCC = 3.0 V, Vo = VCC, Pull-downs “on” Output transistors “off”	6.0	25	45	μA	
ILEAK	Output leak current P00–P07, P10–P15, P30–P37	Vo = VCC, Pull-downs “off” Output transistors “off”			5.0	μA	
		Vo = VSS, Pull-downs “off” Output transistors “off”			-5.0	μA	

Note: When “1” is set to port Xc switch bit (bit 4 of address 003B16) of CPU mode register, the drive ability of port P80 is different from the value above mentioned.

Table 18. Electrical characteristics (Standard, One time PROM version)

(VCC = 2.5 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM retention voltage	At clock stop mode	2.0		5.5	V
ICC	Power source current	<ul style="list-style-type: none"> High-speed mode, VCC = 5 V f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors "off" A-D converter in operating 		6.4	13	mA
		<ul style="list-style-type: none"> High-speed mode, VCC = 5 V f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors "off" A-D converter in operating 		1.6	3.2	mA
		<ul style="list-style-type: none"> Low-speed mode, VCC = 5 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off" 		25	36	μA
		<ul style="list-style-type: none"> Low-speed mode, VCC = 5 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off" 		7.0	14	μA
		<ul style="list-style-type: none"> Low-speed mode, VCC = 3 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off" 		15	22	μA
		<ul style="list-style-type: none"> Low-speed mode, VCC = 3 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off" 		4.5	9.0	μA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C Ta = 85 °C		0.1	10
VL1	Power source voltage	When using voltage multiplier	1.3	1.8	2.3	V
IL1	Power source current (VL1) (Note)	VL1 = 1.8 V		3.0	6.0	μA
		VL1 < 1.3 V		10	50	

Note : When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".

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Table 19. A-D converter characteristics (Standard, One time PROM version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85°C, 4 MHz ≤ f(XIN) ≤ 8 MHz, in middle-/high-speed mode, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	VCC = VREF = 5 V			±2	LSB
tCONV	Conversion time	f(XIN) = 8 MHz		12.5 (Note)		μs
RLADDER	Ladder resistor		12	35	100	kΩ
IVREF	Reference input current	VREF = 5 V	50	150	200	μA
IIA	Analog port input current				5.0	μA

Note : When an internal trigger is used in middle-speed mode, it is 14 μs.

Table 20. Timing requirements 1 (Standard, One time PROM version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	Main clock input cycle time (XIN input)	125			ns
twH(XIN)	Main clock input "H" pulse width	45			ns
twL(XIN)	Main clock input "L" pulse width	40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	250			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	105			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	105			ns
twH(INT)	INT0 to INT3 input "H" pulse width	80			ns
twL(INT)	INT0 to INT3 input "L" pulse width	80			ns
tc(SCLK)	Serial I/O clock input cycle time (Note)	800			ns
twH(SCLK)	Serial I/O clock input "H" pulse width (Note)	370			ns
twL(SCLK)	Serial I/O clock input "L" pulse width (Note)	370			ns
tsu(RxD-SCLK)	Serial I/O input set up time	220			ns
th(SCLK-RxD)	Serial I/O input hold time	100			ns

Note : When f(XIN) = 8 MHz and bit 6 of address 001A16 is "1" (Clock synchronous).

Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is "0" (UART).

Table 21. Timing requirements 2 (Standard, One time PROM version)

(VCC = 2.5 to 4.0 V, VSS = 0 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	Main clock input cycle time (XIN input)	125			ns
twH(XIN)	Main clock input "H" pulse width	45			ns
twL(XIN)	Main clock input "L" pulse width	40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	500/ (VCC-2)			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	250/ (VCC-2)-20			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	250/ (VCC-2)-20			ns
twH(INT)	INT0 to INT3 input "H" pulse width	230			ns
twL(INT)	INT0 to INT3 input "L" pulse width	230			ns
tc(SCLK)	Serial I/O clock input cycle time (Note)	2000			ns
twH(SCLK)	Serial I/O clock input "H" pulse width (Note)	950			ns
twL(SCLK)	Serial I/O clock input "L" pulse width (Note)	950			ns
tsu(RxD-SCLK)	Serial I/O input set up time	400			ns
th(SCLK-RxD)	Serial I/O input hold time	200			ns

Note : When f(XIN) = 8 MHz and bit 6 of address 001A16 is "1" (Clock synchronous).

Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is "0" (UART).

Table 22. Switching characteristics 1 (Standard, One time PROM version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{wH} (SCLK)	Serial I/O clock output "H" pulse width	t _c (SCLK)/2-30			ns
t _{wL} (SCLK)	Serial I/O clock output "L" pulse width	t _c (SCLK)/2-30			ns
t _d (SCLK-TxD)	Serial I/O output delay time (Note 1)			140	ns
t _v (SCLK-TxD)	Serial I/O output valid time (Note 1)	-30			ns
t _r (SCLK)	Serial I/O clock output rising time			30	ns
t _f (SCLK)	Serial I/O clock output falling time			30	ns
t _r (CMOS)	CMOS output rising time (Note 2)		10	30	ns
t _f (CMOS)	CMOS output falling time (Note 2)		10	30	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".**2** : XOUT and XCOUT pins are excluded.**Table 23. Switching characteristics 2 (Standard, One time PROM version)**

(VCC = 2.5 to 4.0 V, VSS = 0 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{wH} (SCLK)	Serial I/O clock output "H" pulse width	t _c (SCLK)/2-50			ns
t _{wL} (SCLK)	Serial I/O clock output "L" pulse width	t _c (SCLK)/2-50			ns
t _d (SCLK-TxD)	Serial I/O output delay time (Note 1)			350	ns
t _v (SCLK-TxD)	Serial I/O output valid time (Note 1)	-30			ns
t _r (SCLK)	Serial I/O clock output rising time			50	ns
t _f (SCLK)	Serial I/O clock output falling time			50	ns
t _r (CMOS)	CMOS output rising time (Note 2)		20	50	ns
t _f (CMOS)	CMOS output falling time (Note 2)		20	50	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".**2** : XOUT and XCOUT pins are excluded.

ELECTRICAL CHARACTERISTICS (Extended Operating Temperature Version)

Table 24. Absolute maximum ratings (Extended operating temperature version)

Symbol	Parameter	Conditions	Ratings	Unit	
VCC	Power source voltage	All voltages are based on VSS. Output transistors are cut off.	-0.3 to 7.0	V	
VI	Input voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P80, P81		-0.3 to VCC +0.3	V	
VI	Input voltage P70-P77		-0.3 to VCC +0.3	V	
VI	Input voltage VL1		-0.3 to VL2	V	
VI	Input voltage VL2		VL1 to VL3	V	
VI	Input voltage VL3		VL2 to 7.0	V	
VI	Input voltage C1, C2		-0.3 to 7.0	V	
VI	Input voltage RESET, XIN		-0.3 to VCC +0.3	V	
VO	Output voltage C1, C2		-0.3 to 7.0	V	
VO	Output voltage P00-P07, P10-P15, P30-P37		At output port	-0.3 to VCC	V
			At segment output	-0.3 to VL3	V
VO	Output voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81		-0.3 to VCC +0.3	V	
VO	Output voltage VL3		-0.3 to 7.0	V	
VO	Output voltage VL2, SEG0-SEG17	-0.3 to VL3	V		
VO	Output voltage XOUT	-0.3 to VCC +0.3	V		
Pd	Power dissipation	Ta = 25°C	300	mW	
Topr	Operating temperature		-40 to 85	°C	
Tstg	Storage temperature		-65 to 150	°C	

Table 25. Recommended operating conditions (Extended operating temperature version)

(VCC = 2.5 to 5.5 V, Ta = -20 to 85°C, and VCC = 3.0 to 5.5 V, Ta = -40 to -20°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit	
			Min.	Typ.	Max.		
VCC	Power source voltage	High-speed mode f(XIN)=8 MHz	4.0	5.0	5.5	V	
		Middle-speed mode f(XIN) = 8 MHz	Ta = -20 to 85°C	2.5	5.0		5.5
			Ta = -40 to -20°C	3.0	5.0		5.5
		Low-speed mode	Ta = -20 to 85°C	2.5	5.0		5.5
			Ta = -40 to -20°C	3.0	5.0		5.5
VSS	Power source voltage		0		V		
VREF	A-D conversion reference voltage		2.0	VCC	V		
AVSS	Analog power source voltage		0		V		
VIA	Analog input voltage AN0-AN7		AVSS	VCC	V		
VIH	"H" input voltage P16, P17, P40, P41, P45, P47, P52, P53, P56, P60-P67, P70-P77, P80, P81 (CM4=0)		0.7VCC	VCC	V		
VIH	"H" input voltage P20-P27, P42-P44, P46, P50, P51, P54, P55, P57		0.8VCC	VCC	V		
VIH	"H" input voltage RESET		0.8VCC	VCC	V		
VIH	"H" input voltage XIN		0.8VCC	VCC	V		
VIL	"L" input voltage P16, P17, P40, P41, P45, P47, P52, P53, P56, P60-P67, P70-P77, P80, P81 (CM4=0)		0	0.3VCC	V		
VIL	"L" input voltage P20-P27, P42-P44, P46, P50, P51, P54, P55, P57		0	0.2VCC	V		
VIL	"L" input voltage RESET		0	0.2VCC	V		
VIL	"L" input voltage XIN		0	0.2VCC	V		

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Table 26. Recommended operating conditions (Extended operating temperature version)(V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, and V_{CC} = 3.0 to 5.5 V, T_a = -40 to -20°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current	P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			-20	mA
ΣIOH(peak)	"H" total peak output current	P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 1)			-20	mA
ΣIOL(peak)	"L" total peak output current	P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			20	mA
ΣIOL(peak)	"L" total peak output current	P40-P47, P50-P57, P60-P67, P80, P81 (Note 1)			20	mA
ΣIOL(peak)	"L" total peak output current	P71-P77 (Note 1)			40	mA
ΣIOH(avg)	"H" total average output current	P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			-10	mA
ΣIOH(avg)	"H" total average output current	P40-P47, P50-P57, P60-P67, P70-P71, P80, P81 (Note 1)			-10	mA
ΣIOL(avg)	"L" total average output current	P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			10	mA
ΣIOL(avg)	"L" total average output current	P40-P47, P50-P57, P60-P67, P80, P81 (Note 1)			10	mA
ΣIOL(avg)	"L" total average output current	P71-P77 (Note 1)			20	mA
IOH(peak)	"H" peak output current	P00-P07, P10-P15, P30-P37 (Note 2)			-0.5	mA
IOH(peak)	"H" peak output current	P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 2)			-5.0	mA
IOL(peak)	"L" peak output current	P00-P07, P10-P15, P30-P37 (Note 2)			5.0	mA
IOL(peak)	"L" peak output current	P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 2)			10	mA
IOH(avg)	"H" average output current	P00-P07, P10-P15, P30-P37 (Note 3)			-0.1	mA
IOH(avg)	"H" average output current	P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 3)			-2.5	mA
IOL(avg)	"H" average output current	P00-P07, P10-P15, P30-P37 (Note 3)			2.5	mA
IOL(avg)	"H" average output current	P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 3)			5.0	mA
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ V _{CC} ≤ 5.5 V)			4.0	MHz
		(V _{CC} ≤ 4.0 V)			(2×V _{CC})-4	MHz
f(XIN)	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ V _{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (V _{CC} ≤ 4.0 V)			(4×V _{CC})-8	MHz
		Middle-speed mode			8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency (Note 4, 5)		32.768	50		kHz

Notes 1 : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2 : The peak output current is the peak current flowing in each port.

3 : The average output current is an average value measured over 100 ms.

4 : When the oscillation frequency has a duty cycle of 50%.

5 : When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

Table 27. Electrical characteristics (Extended operating temperature version)(V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, and V_{CC} = 3.0 to 5.5V, T_a = -40 to -20°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V _{OH}	“H” output voltage P00–P07, P10–P15, P30–P37	I _{OH} = -2.5 mA	V _{CC} -2.0			V	
		I _{OH} = -0.6 mA	V _{CC} -0.9			V	
		V _{CC} = 3.0 V					
V _{OH}	“H” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	I _{OH} = -5 mA	V _{CC} -2.0			V	
		I _{OH} = -1.25 mA	V _{CC} -0.5			V	
		I _{OH} = -1.25 mA	V _{CC} -0.9			V	
V _{OL}	“L” output voltage P00–P07, P10–P15, P30–P37	I _{OL} = 5 mA			2.0	V	
		I _{OL} = 1.25 mA			0.5	V	
		I _{OL} = 1.25 mA			1.1	V	
V _{OL}	“L” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	I _{OL} = 10 mA			2.0	V	
		I _{OL} = 2.5 mA			0.5	V	
		I _{OL} = 2.5 mA			1.1	V	
		V _{CC} = 3.0 V					
V _{T+} – V _{T-}	Hysteresis	INT0–INT3, ADT, CNTR0, CNTR1, P20–P27		0.5		V	
V _{T+} – V _{T-}	Hysteresis	SCLK, RXD		0.5		V	
V _{T+} – V _{T-}	Hysteresis	RESET	RESET: V _{CC} =2.5 V to 5.5 V	0.5		V	
I _{IH}	“H” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81	V _I = V _{CC}		5.0	μA	
I _{IH}	“H” input current	RESET	V _I = V _{CC}		5.0	μA	
I _{IH}	“H” input current	XIN	V _I = V _{CC}	4.0		μA	
I _{IL}	“L” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81	V _I = V _{SS} Pull-ups “off”			-5.0	μA
			V _{CC} = 5 V, V _I = V _{SS} Pull-ups “on”	-30	-70	-140	μA
			V _{CC} = 3 V, V _I = V _{SS} Pull-ups “on”	-6.0	-25	-45	μA
I _{IL}	“L” input current	P70			-5.0	μA	
I _{IL}	“L” input current	RESET	V _I = V _{SS}		-5.0	μA	
I _{IL}	“L” input current	XIN	V _I = V _{SS}	-4.0		μA	
I _{LOAD}	Output load current P00–P07, P10–P15, P30–P37	V _{CC} = 5.0 V, V _O = V _{CC} , Pull-downs “on” Output transistors “off”	30	70	170	μA	
		V _{CC} = 3.0 V, V _O = V _{CC} , Pull-downs “on” Output transistors “off”	6.0	25	55	μA	
I _{LEAK}	Output leak current P00–P07, P10–P15, P30–P37	V _O = V _{CC} , Pull-downs “off” Output transistors “off”			5.0	μA	
		V _O = V _{SS} , Pull-downs “off” Output transistors “off”			-5.0	μA	

Note : When “1” is set to port Xc switch bit (bit 4 of address 003B16) of CPU mode register, the drive ability of port P80 is different from the value above mentioned.

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Table 28. Electrical characteristics (Extended operating temperature version)

(VCC = 2.5 to 5.5 V, Ta = -20 to 85°C, and VCC = 3.0 to 5.5 V, Ta = -40 to -20°C, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM retention voltage	At clock stop mode	2.0		5.5	V
ICC	Power source current	• High-speed mode, VCC = 5 V f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors "off" A-D converter in operating		6.4	13	mA
		• High-speed mode, VCC = 5 V f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors "off" A-D converter in operating		1.6	3.2	mA
		• Low-speed mode, VCC = 5 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off"		25	36	μA
		• Low-speed mode, VCC = 5 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off"		7.0	14	μA
		• Low-speed mode, VCC = 3 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off"		15	22	μA
		• Low-speed mode, VCC = 3 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off"		4.5	9.0	μA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25°C Ta = 85°C		0.1 10	1.0
VL1	Power source voltage	When using voltage multiplier	1.3	1.8	2.3	V
IL1	Power source current (VL1) (Note)	VL1 = 1.8 V		3.0	6.0	μA
		VL1 < 1.3 V		10	50	

Note : When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".**Table 29. A-D converter characteristics (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -40 to 85°C, 4 MHz ≤ f(XIN) ≤ 8 MHz, in middle-/high-speed mode, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute accuracy (excluding quantization error)	VCC = VREF = 5 V			±2	LSB
tCONV	Conversion time	f(XIN) = 8 MHz		12.5 (Note)		μs
RLADDER	Ladder resistor		12	35	100	kΩ
IVREF	Reference input current	VREF = 5 V	50	150	200	μA
IIA	Analog iinput current				5.0	μA

Note : When an internal trigger is used in middle-speed mode, it is 14 μs.

Table 30. Timing requirements 1 (Extended operating temperature version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -40 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (XIN)	Main clock input cycle time (XIN input)	125			ns
t _{wH} (XIN)	Main clock input "H" pulse width	45			ns
t _{wL} (XIN)	Main clock input "L" pulse width	40			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	250			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input "H" pulse width	105			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input "L" pulse width	105			ns
t _{wH} (INT)	INT0 to INT3 input "H" pulse width	80			ns
t _{wL} (INT)	INT0 to INT3 input "L" pulse width	80			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	800			ns
t _{wH} (SCLK)	Serial I/O clock input "H" pulse width (Note)	370			ns
t _{wL} (SCLK)	Serial I/O clock input "L" pulse width (Note)	370			ns
t _{su} (RxD-SCLK)	Serial I/O input set up time	220			ns
t _h (SCLK-RxD)	Serial I/O input hold time	100			ns

Note : When f(XIN) = 8 MHz and bit 6 of address 001A16 is "1" (Clock synchronous).

Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is "0" (UART).

Table 31. Timing requirements 2 (Extended operating temperature version)

(VCC = 2.5 to 4.0 V, VSS = 0 V, Ta = -20 to 85°C, and VCC = 3.0 to 4.0 V, VSS = 0 V, Ta = -40 to -20°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (XIN)	Main clock input cycle time (XIN input)	125			ns
t _{wH} (XIN)	Main clock input "H" pulse width	45			ns
t _{wL} (XIN)	Main clock input "L" pulse width	40			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	500/ (VCC-2)			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input "H" pulse width	250/ (VCC-2)-20			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input "L" pulse width	250/ (VCC-2)-20			ns
t _{wH} (INT)	INT0 to INT3 input "H" pulse width	230			ns
t _{wL} (INT)	INT0 to INT3 input "L" pulse width	230			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	2000			ns
t _{wH} (SCLK)	Serial I/O clock input "H" pulse width (Note)	950			ns
t _{wL} (SCLK)	Serial I/O clock input "L" pulse width (Note)	950			ns
t _{su} (RxD-SCLK)	Serial I/O input set up time	400			ns
t _h (SCLK-RxD)	Serial I/O input hold time	200			ns

Note: When f(XIN) = 8 MHz and bit 6 of address 001A16 is "1" (Clock synchronous).

Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is "0" (UART).

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Table 32. Switching characteristics 1 (Extended operating temperature version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -40 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
twH(SCLK)	Serial I/O clock output "H" pulse width	tc(SCLK)/2-30			ns
twL(SCLK)	Serial I/O clock output "L" pulse width	tc(SCLK)/2-30			ns
td(SCLK-TxD)	Serial I/O output delay time (Note 1)			140	ns
tv(SCLK-TxD)	Serial I/O output valid time (Note 1)	-30			ns
tr(SCLK)	Serial I/O clock output rising time			30	ns
tf(SCLK)	Serial I/O clock output falling time			30	ns
tr(CMOS)	CMOS output rising time (Note 2)		10	30	ns
tf(CMOS)	CMOS output falling time (Note 2)		10	30	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".**2** : XOUT and Xcout pins are excluded.**Table 33. Switching characteristics 2 (Extended operating temperature version)**

(VCC = 2.5 to 4.0 V, VSS = 0 V, Ta = -20 to 85°C, and VCC = 3.0 to 4.0 V, VSS = 0 V, Ta = -40 to -20°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
twH(SCLK)	Serial I/O clock output "H" pulse width	tc(SCLK)/2-50			ns
twL(SCLK)	Serial I/O clock output "L" pulse width	tc(SCLK)/2-50			ns
td(SCLK-TxD)	Serial I/O output delay time (Note 1)			350	ns
tv(SCLK-TxD)	Serial I/O output valid time (Note 1)	-30			ns
tr(SCLK)	Serial I/O clock output rising time			50	ns
tf(SCLK)	Serial I/O clock output falling time			50	ns
tr(CMOS)	CMOS output rising time (Note 2)		20	50	ns
tf(CMOS)	CMOS output falling time (Note 2)		20	50	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".**2** : XOUT and Xcout pins are excluded.

ELECTRICAL CHARACTERISTICS (M Version)

Table 34. Absolute maximum ratings (M version)

Symbol	Parameter	Conditions	Ratings	Unit	
VCC	Power source voltage	All voltages are based on VSS. Output transistors are cut off.	-0.3 to 7.0	V	
VI	Input voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P80, P81		-0.3 to VCC +0.3	V	
VI	Input voltage P70-P77		-0.3 to VCC +0.3	V	
VI	Input voltage VL1		-0.3 to VL2	V	
VI	Input voltage VL2		VL1 to VL3	V	
VI	Input voltage VL3		VL2 to 7.0	V	
VI	Input voltage C1, C2		-0.3 to 7.0	V	
VI	Input voltage RESET, XIN		-0.3 to VCC +0.3	V	
VO	Output voltage C1, C2		-0.3 to 7.0	V	
VO	Output voltage P00-P07, P10-P15, P30-P37		At output port	-0.3 to VCC	V
			At segment output	-0.3 to VL3	V
VO	Output voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81		-0.3 to VCC +0.3	V	
VO	Output voltage VL3		-0.3 to 7.0	V	
VO	Output voltage VL2, SEG0-SEG17	-0.3 to VL3	V		
VO	Output voltage XOUT	-0.3 to VCC +0.3	V		
Pd	Power dissipation	Ta = 25°C	300	mW	
Topr	Operating temperature		-20 to 85	°C	
Tstg	Storage temperature		-40 to 125	°C	

Table 35. Recommended operating conditions (M version)

(VCC = 2.2 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage	High-speed mode, f(XIN)=8 MHz	4.0	5.0	5.5	V
		Middle-speed mode, f(XIN) = 8 MHz	2.2	5.0	5.5	
		Low-speed mode	2.2	5.0	5.5	
VSS	Power source voltage		0		V	
VREF	A-D conversion reference voltage		2.0	VCC	V	
AVSS	Analog power source voltage			0	V	
VIA	Analog input voltage	AN0-AN7	AVSS		VCC	V
VIH	"H" input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60-P67, P70-P77, P80, P81 (CM4=0)	0.7VCC		VCC	V
VIH	"H" input voltage	P20-P27, P42-P44, P46, P50, P51, P54, P55, P57	0.8VCC		VCC	V
VIH	"H" input voltage	RESET	0.8VCC		VCC	V
VIH	"H" input voltage	XIN	0.8VCC		VCC	V
VIL	"L" input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60-P67, P70-P77, P80, P81 (CM4=0)	0		0.3VCC	V
VIL	"L" input voltage	P20-P27, P42-P44, P46, P50, P51, P54, P55, P57	0		0.2VCC	V
VIL	"L" input voltage	RESET	0		0.2VCC	V
VIL	"L" input voltage	XIN	0		0.2VCC	V

Table 36. Recommended operating conditions (M version)

(VCC = 2.2 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			-20	mA
ΣIOH(peak)	"H" total peak output current P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 1)			-20	mA
ΣIOL(peak)	"L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			20	mA
ΣIOL(peak)	"L" total peak output current P40-P47, P50-P57, P60-P67, P80, P81 (Note 1)			20	mA
ΣIOL(peak)	"L" total peak output current P71-P77 (Note 1)			40	mA
ΣIOH(avg)	"H" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			-10	mA
ΣIOH(avg)	"H" total average output current P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 1)			-10	mA
ΣIOL(avg)	"L" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			10	mA
ΣIOL(avg)	"L" total average output current P40-P47, P50-P57, P60-P67, P80, P81 (Note 1)			10	mA
ΣIOL(avg)	"L" total average output current P71-P77 (Note 1)			20	mA
IOH(peak)	"H" peak output current P00-P07, P10-P15, P30-P37 (Note 2)			-0.5	mA
IOH(peak)	"H" peak output current P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 2)			-5.0	mA
IOL(peak)	"L" peak output current P00-P07, P10-P15, P30-P37 (Note 2)			5.0	mA
IOL(peak)	"L" peak output current P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 2)			10	mA
IOH(avg)	"H" average output current P00-P07, P10-P15, P30-P37 (Note 3)			-0.1	mA
IOH(avg)	"H" average output current P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 3)			-2.5	mA
IOL(avg)	"H" average output current P00-P07, P10-P15, P30-P37 (Note 3)			2.5	mA
IOL(avg)	"H" average output current P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77, P80, P81 (Note 3)			5.0	mA
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ VCC ≤ 5.5 V)		4.0	MHz
		(2.2 V ≤ VCC ≤ 4.0 V)		(10 × VCC - 4) / 9	MHz
f(XIN)	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ VCC ≤ 5.5 V)		8.0	MHz
		High-speed mode (2.2 V ≤ VCC ≤ 4.0 V)		(20 × VCC - 8) / 9	MHz
		Middle-speed mode		8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Notes 1 : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2 : The peak output current is the peak current flowing in each port.

3 : The average output current is an average value measured over 100 ms.

4 : When the oscillation frequency has a duty cycle of 50%.

5 : When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(XCIN) < f(XIN)/3$.

Table 37. Electrical characteristics (M version)

(V_{CC} = 2.2 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V _{OH}	“H” output voltage P00–P07, P10–P15, P30–P37	I _{OH} = -2.5 mA	V _{CC} -2.0			V	
		I _{OH} = -0.25 mA	V _{CC} -0.8			V	
		V _{CC} = 2.2 V					
V _{OH}	“H” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	I _{OH} = -5 mA	V _{CC} -2.0			V	
		I _{OH} = -1.25 mA	V _{CC} -0.5			V	
		I _{OH} = -1.25 mA	V _{CC} -0.8			V	
V _{OL}	“L” output voltage P00–P07, P10–P15, P30–P37	I _{OL} = 5 mA			2.0	V	
		I _{OL} = 1.25 mA			0.5	V	
		I _{OL} = 1.25 mA			0.8	V	
V _{OL}	“L” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	I _{OL} = 10 mA			2.0	V	
		I _{OL} = 2.5 mA			0.5	V	
		I _{OL} = 2.5 mA			0.8	V	
		V _{CC} = 2.2 V					
V _{T+} – V _{T-}	Hysteresis	INT0–INT3, ADT, CNTR0, CNTR1, P20–P27		0.5		V	
V _{T+} – V _{T-}	Hysteresis	SCLK, RXD		0.5		V	
V _{T+} – V _{T-}	Hysteresis	RESET	RESET: V _{CC} =2.2 V to 5.5 V	0.5		V	
I _{IH}	“H” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81	V _I = V _{CC}		5.0	μA	
I _{IH}	“H” input current	RESET	V _I = V _{CC}		5.0	μA	
I _{IH}	“H” input current	XIN	V _I = V _{CC}	4.0		μA	
I _{IL}	“L” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81	V _I = V _{SS} Pull-ups “off”			-5.0	μA
			V _{CC} = 5 V, V _I = V _{SS} Pull-ups “on”	-30	-70	-140	μA
			V _{CC} = 2.2 V, V _I = V _{SS} Pull-ups “on”	-6.0	-25	-45	μA
I _{IL}	“L” input current	P70			-5.0	μA	
I _{IL}	“L” input current	RESET	V _I = V _{SS}		-5.0	μA	
I _{IL}	“L” input current	XIN	V _I = V _{SS}	-4.0		μA	
I _{LOAD}	Output load current P00–P07, P10–P15, P30–P37	V _{CC} = 5.0 V, V _O = V _{CC} , Pull-downs “on” Output transistors “off”	30	70	140	μA	
		V _{CC} = 2.2 V, V _O = V _{CC} , Pull-downs “on” Output transistors “off”	6.0	25	45	μA	
I _{LEAK}	Output leak current P00–P07, P10–P15, P30–P37	V _O = V _{CC} , Pull-downs “off” Output transistors “off”			5.0	μA	
		V _O = V _{SS} , Pull-downs “off” Output transistors “off”			-5.0	μA	

Note : When “1” is set to port Xc switch bit (bit 4 of address 003B16) of CPU mode register, the drive ability of port P80 is different from the value above mentioned.

Table 38. Electrical characteristics (M version)

(VCC = 2.2 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM retention voltage	At clock stop mode	2.0		5.5	V
Icc	Power source current	<ul style="list-style-type: none"> High-speed mode, VCC = 5 V f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors "off" A-D converter in operating 		6.4	13	mA
		<ul style="list-style-type: none"> High-speed mode, VCC = 5 V f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors "off" A-D converter in operating 		1.6	3.2	mA
		<ul style="list-style-type: none"> Low-speed mode, VCC = 5 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off" 		25	36	μA
		<ul style="list-style-type: none"> Low-speed mode, VCC = 5 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off" 		7.0	14	μA
		<ul style="list-style-type: none"> Low-speed mode, VCC = 3 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off" 		15	22	μA
		<ul style="list-style-type: none"> Low-speed mode, VCC = 3 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off" 		4.5	9.0	μA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25°C Ta = 85°C		0.1	1.0
				10		
VL1	Power source voltage	When using voltage multiplier	1.3	1.8	2.3	V
IL1	Power source current (VL1) (Note)	VL1 = 1.8 V		3.0	6.0	μA
		VL1 < 1.3 V		10	50	

Note : When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".

Table 39. A-D converter characteristics (M version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85°C, 4 MHz ≤ f(XIN) ≤ 8 MHz, in middle-/high-speed mode, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	VCC = VREF = 5 V			±2	LSB
tCONV	Conversion time	f(XIN) = 8 MHz		12.5 (Note)		μs
RLADDER	Ladder resistor		12	35	100	kΩ
IVREF	Reference input current	VREF = 5 V	50	150	200	μA
IiA	Analog input current				5.0	μA

Note : When an internal trigger is used in middle-speed mode, it is 14 μs.

Table 40. Timing requirements 1 (M Version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (XIN)	Main clock input cycle time (XIN input)	125			ns
t _{wH} (XIN)	Main clock input "H" pulse width	45			ns
t _{wL} (XIN)	Main clock input "L" pulse width	40			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	250			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input "H" pulse width	105			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input "L" pulse width	105			ns
t _{wH} (INT)	INT0 to INT3 input "H" pulse width	80			ns
t _{wL} (INT)	INT0 to INT3 input "L" pulse width	80			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	800			ns
t _{wH} (SCLK)	Serial I/O clock input "H" pulse width (Note)	370			ns
t _{wL} (SCLK)	Serial I/O clock input "L" pulse width (Note)	370			ns
t _{su} (RxD-SCLK)	Serial I/O input set up time	220			ns
t _h (SCLK-RxD)	Serial I/O input hold time	100			ns

Note : When f(XIN) = 8 MHz and bit 6 of address 001A16 is "1" (Clock synchronous).
Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is "0" (UART).

Table 41. Timing requirements 2 (M Version)

(VCC = 2.2 to 4.0 V, VSS = 0 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (XIN)	Main clock input cycle time (XIN input)	125			ns
t _{wH} (XIN)	Main clock input "H" pulse width	45			ns
t _{wL} (XIN)	Main clock input "L" pulse width	40			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	900 / (VCC - 0.4)			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input "H" pulse width	450 / (VCC - 0.4) - 20			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input "L" pulse width	450 / (VCC - 0.4) - 20			ns
t _{wH} (INT)	INT0 to INT3 input "H" pulse width	230			ns
t _{wL} (INT)	INT0 to INT3 input "L" pulse width	230			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	2000			ns
t _{wH} (SCLK)	Serial I/O clock input "H" pulse width (Note)	950			ns
t _{wL} (SCLK)	Serial I/O clock input "L" pulse width (Note)	950			ns
t _{su} (RxD-SCLK)	Serial I/O input set up time	400			ns
t _h (SCLK-RxD)	Serial I/O input hold time	200			ns

Note: When f(XIN) = 8 MHz and bit 6 of address 001A16 is "1" (Clock synchronous).
Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is "0" (UART).

Table 42. Switching characteristics 1 (M version)

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
twH(SCLK)	Serial I/O clock output "H" pulse width	tc(SCLK)/2-30			ns
twL(SCLK)	Serial I/O clock output "L" pulse width	tc(SCLK)/2-30			ns
td(SCLK-TxD)	Serial I/O output delay time (Note 1)			140	ns
tv(SCLK-TxD)	Serial I/O output valid time (Note 1)	-30			ns
tr(SCLK)	Serial I/O clock output rising time			30	ns
tf(SCLK)	Serial I/O clock output falling time			30	ns
tr(CMOS)	CMOS output rising time (Note 2)		10	30	ns
tf(CMOS)	CMOS output falling time (Note 2)		10	30	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2 : XOUT and Xcout pins are excluded.

Table 43. Switching characteristics 2 (M version)

(VCC = 2.2 to 4.0 V, VSS = 0 V, Ta = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
twH(SCLK)	Serial I/O clock output "H" pulse width	tc(SCLK)/2-50			ns
twL(SCLK)	Serial I/O clock output "L" pulse width	tc(SCLK)/2-50			ns
td(SCLK-TxD)	Serial I/O output delay time (Note 1)			350	ns
tv(SCLK-TxD)	Serial I/O output valid time (Note 1)	-30			ns
tr(SCLK)	Serial I/O clock output rising time			50	ns
tf(SCLK)	Serial I/O clock output falling time			50	ns
tr(CMOS)	CMOS output rising time (Note 2)		20	50	ns
tf(CMOS)	CMOS output falling time (Note 2)		20	50	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2 : XOUT and Xcout pins are excluded.

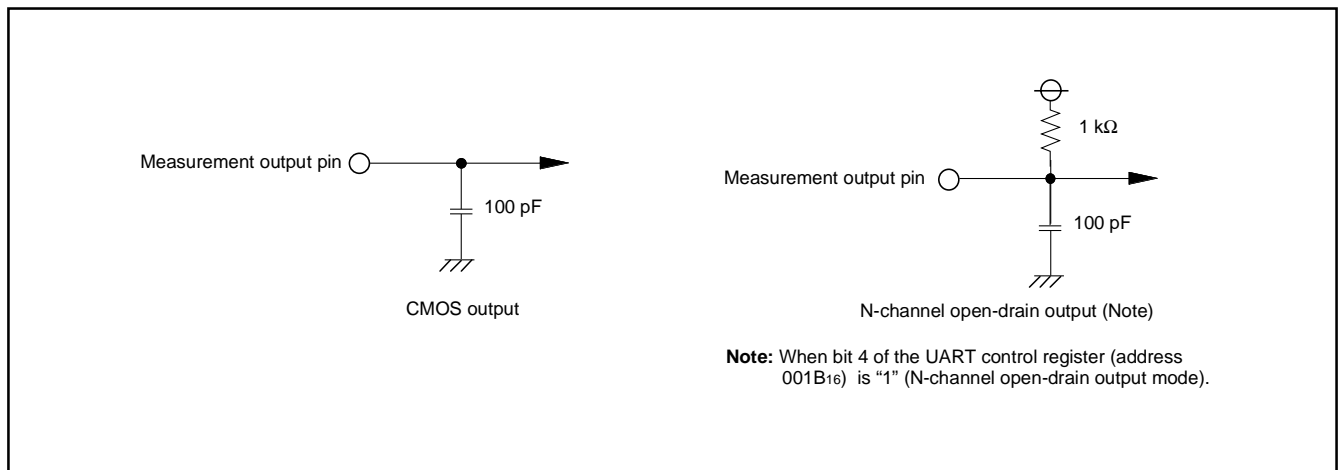


Fig. 46 Circuit for measuring output switching characteristics

TIMING DIAGRAM

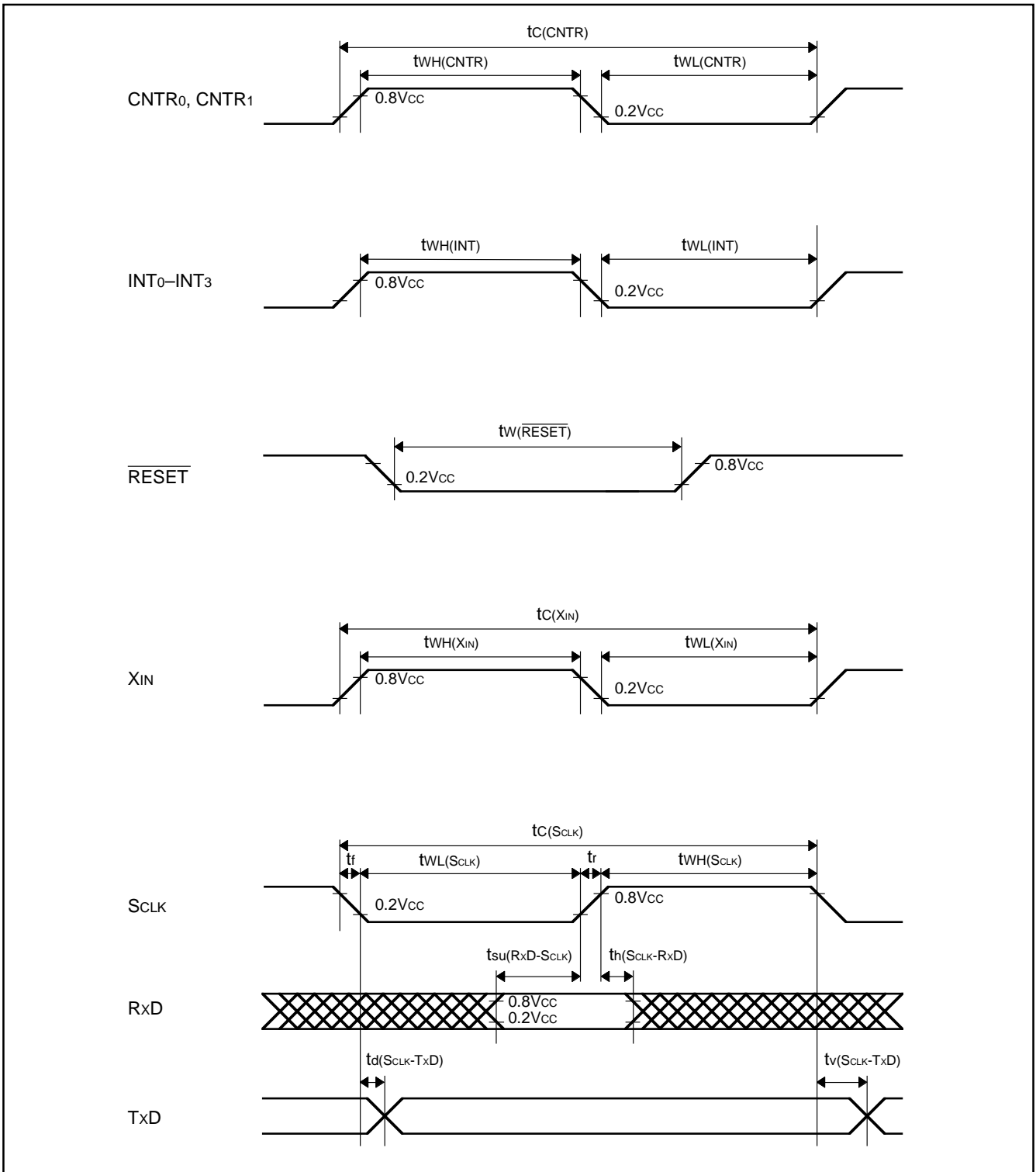


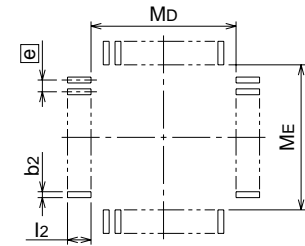
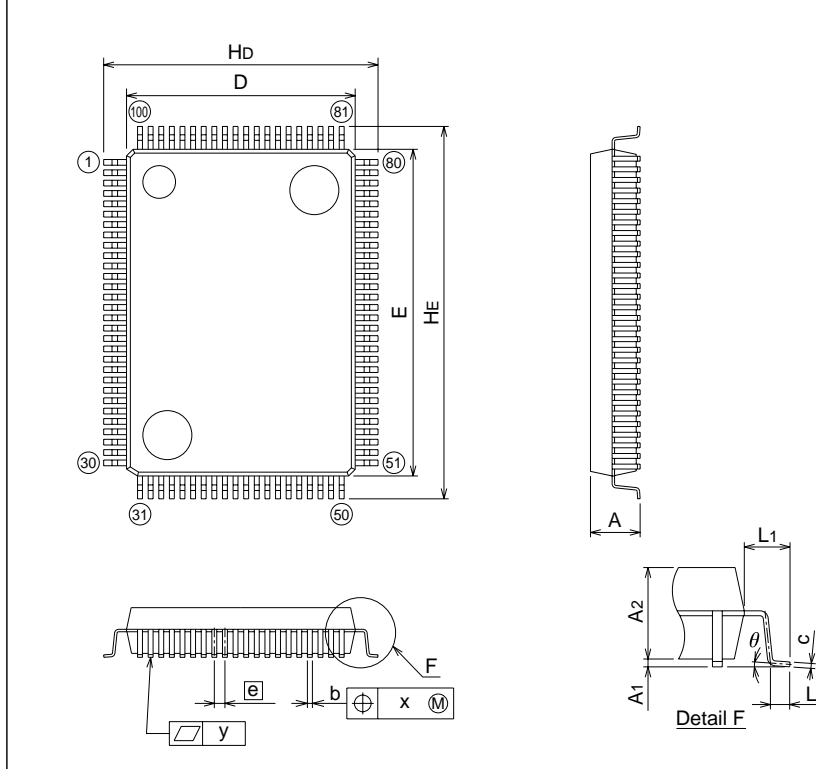
Fig. 47 Timing diagram

PACKAGE OUTLINES

100P6S-A (MMP)

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	-	1.58	Alloy 42

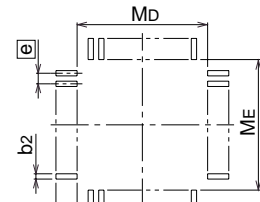
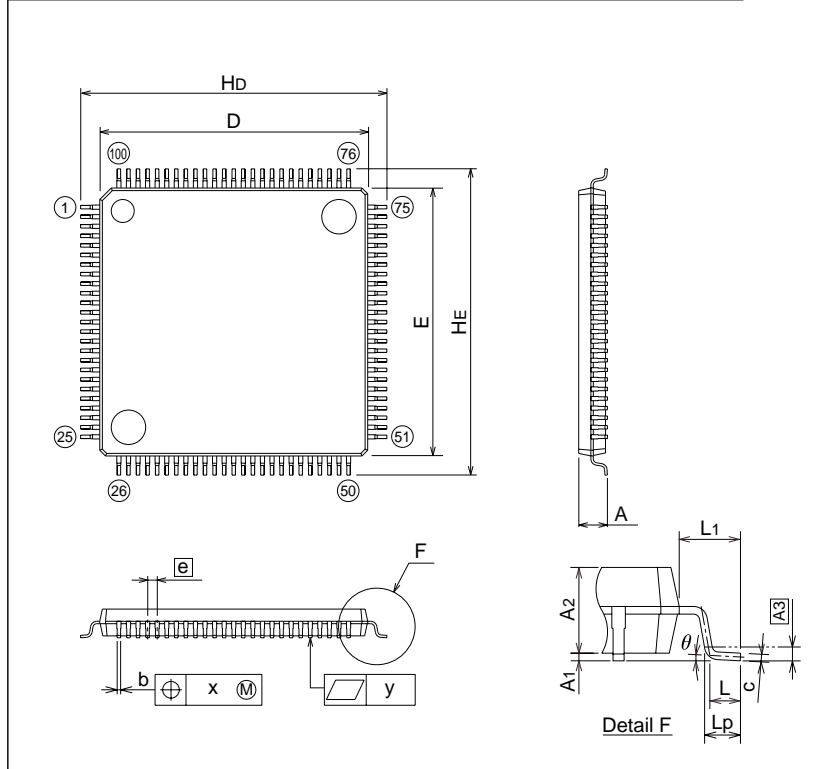


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	-	0.65	-
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	-	1.4	-
x	-	-	0.13
y	-	-	0.1
theta	0°	-	10°
b2	-	0.35	-
l2	1.3	-	-
MD	-	14.6	-
ME	-	20.6	-

100P6Q-A (MMP)

Plastic 100pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	-	0.63	Cu Alloy

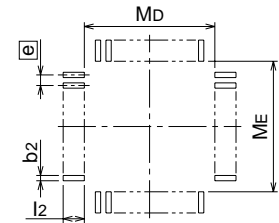
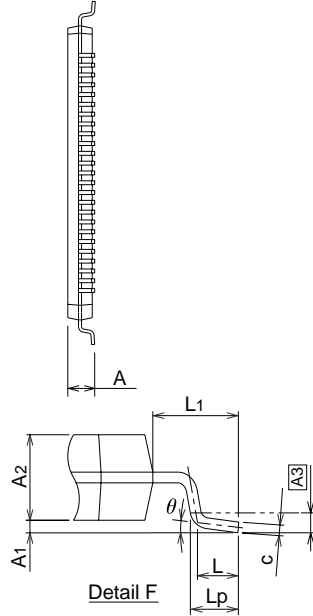
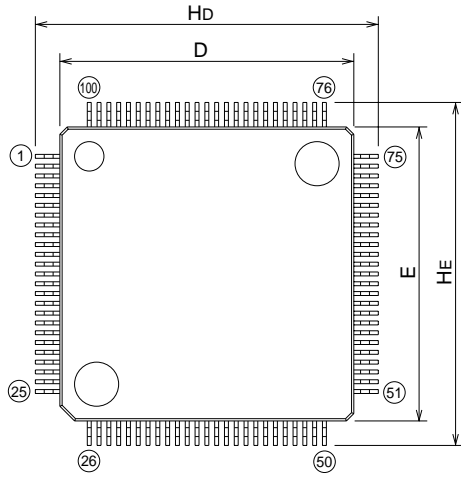


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	-	0.5	-
Hd	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
theta	0°	-	10°
b2	-	0.225	-
l2	0.9	-	-
MD	-	14.4	-
ME	-	14.4	-

100PFB-A (MMP)

Plastic 100pin 12X12mm body TQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TQFP100-P-1212-0.40	-	0.37	Cu Alloy



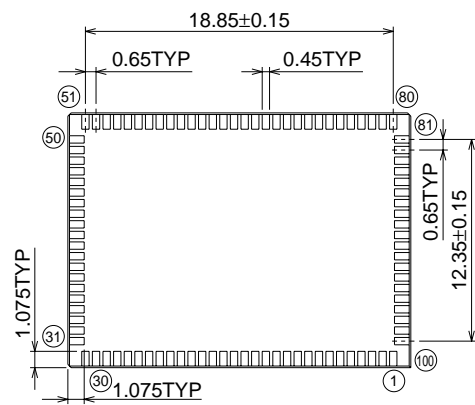
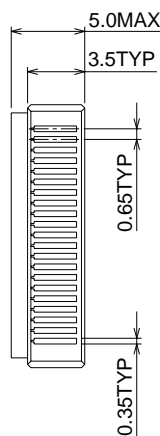
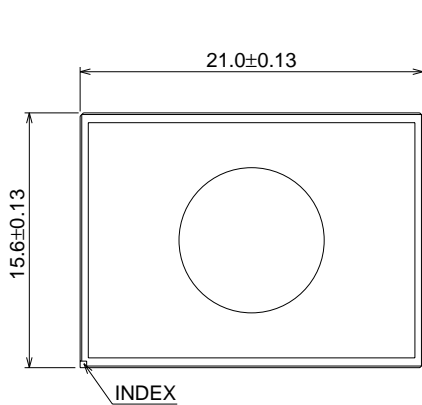
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.2
A1	0.05	0.1	0.15
A2	-	1.0	-
b	0.13	0.18	0.23
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	-	0.4	-
Hd	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.4	0.5	0.6
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.07
y	-	-	0.08
theta	0°	-	10°
b2	-	0.225	-
l2	1.0	-	-
MD	-	12.4	-
ME	-	12.4	-

100D0

Glass seal 100pin QFN

EIAJ Package Code	JEDEC Code	Weight(g)
-	-	-





MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

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REVISION HISTORY

3825 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.0	01/23/98		First Edition
2.0	05/15/98		Low power source version is added.
2.1	07/13/99	7 to 10 17 43 53	The followings are mainly revised: Group expansion (11) Port P70 of port block diagram Name in Table 11 The "L" input current parameter of I _L in Tables 25 and 35 is not P70–P77 but P71–P77.
3.0	12/11/00	1 1 4 6 7 8 9 10 10 11 to 13 20 24 34 40 40 42 43 45 46 46 48 50 57 60 to 65 60 61 63	"•2 Clock generating circuits" of "FEATURES" is partly eliminated. "•Power source voltage" of "FEATURES" is partly revised. "Function" of "V _{cc} , V _{ss} " into Table 1 is partly revised. Figure 4 is partly revised. Clause name and explanations of "GROUP EXPANSION (STANDARD, ONE TIME PROM VERSION, EPROM VERSION)" are partly revised. Table 3 is partly eliminated. Table 4 is partly eliminated. Clause name and explanations of "GROUP EXPANSION (M VERSION)" are partly revised. Figure name of Figure 7 is partly revised. Explanations of "CENTRAL PROCESSING UNIT (CPU)" are added. (12), (13), (14) into Figure 15 is partly revised. Figure 19 is partly revised. Figure 31 is partly revised. Explanations of "RESET CIRCUIT" are partly revised. Figure 38 is partly revised. Explanations of "CLOCK GENERATING CIRCUIT" are partly eliminated. Figure 43 is partly revised. Explanations of "Decimal Calculations" of "NOTES ON PROGRAMMING" are partly eliminated. Explanations of "DATA REQUIRED FOR MASK ORDERS" are partly added. Explanations of "DATA REQUIRED FOR WRITING ORDERS" in Rev.2.1 are eliminated. Note number of "I _{OH(avg)} P00–P07, P10–P15, P30–P37" into Table 16 is revised. Test conditions of I _{cc} into Table 18 are partly revised. Test conditions of I _{cc} into Table 28 are partly revised. Table names of Tables 34 to 43 are partly revised. Limits of AV _{ss} into Table 35 is partly revised. Parameter of ΣI _{OH(avg)} into Table 36 is partly revised. Test conditions of I _{cc} into Table 38 is partly revised.
3.1	02/06/01	22 24 30 46	Explanations of "■Notes on interrupts" are partly revised. Figure 19 is partly revised. "■Notes on serial I/O" is added. Explanations of "DATA REQUIRED FOR MASK ORDERS" are partly revised.