

M5M51008DFP,VP,RV,KV,KR -55H, -70H

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008DFP,VP,RV,KV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance quadruple-polysilicon and double metal CMOS technology. The use of thin film transistor (TFT) load cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51008DVP,RV,KV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD). Two types of devices are available. M5M51008DVP(normal lead bend type package), M5M51008DRV(reverse lead bend type package).Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

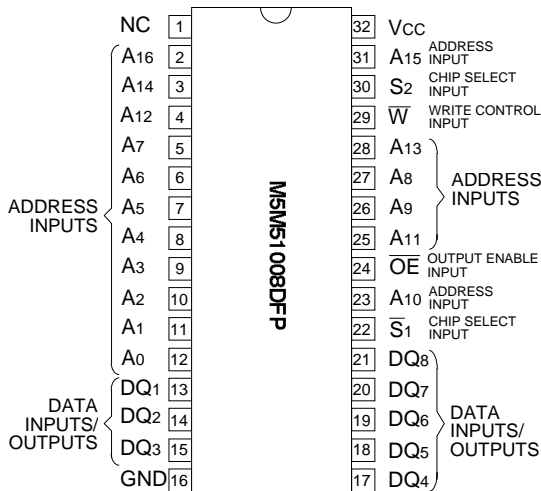
Type name	Access time (max)	Power supply current	
		Active (1MHz) (max)	stand-by (max)
M5M51008DFP,VP,RV,KV-55H	55ns	15mA (1MHz)	20µA (V _{CC} =5.5V)
M5M51008DFP,VP,RV,KV-70H	70ns		

- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by \bar{S}_1, S_2
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- \bar{OE} prevents data contention in the I/O bus
- Common data I/O
- Package
 - M5M51008DFP 32pin 525mil SOP
 - M5M51008DVP,RV 32pin 8 X 20 mm² TSOP
 - M5M51008DKV 32pin 8 X 13.4 mm² TSOP

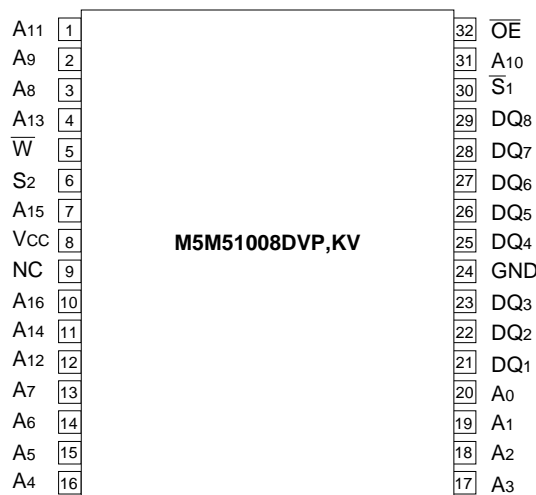
APPLICATION

Small capacity memory units

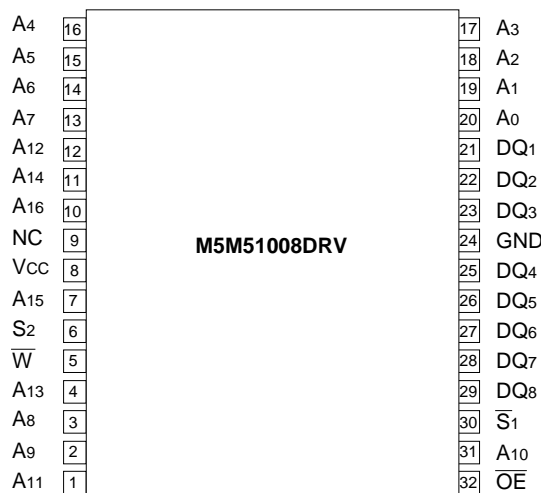
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A(FP)



Outline 32P3H-E(VP), 32P3K-B(KV)



Outline 32P3H-F(RV)

NC : NO CONNECTION

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FUNCTION

The operation mode of the M5M51008D series are determined by a combination of the device control inputs \bar{S}_1, S_2, \bar{W} and \bar{OE} .

Each mode is summarized in the function table.
 A write cycle is executed whenever the low level \bar{W} overlaps with the low level \bar{S}_1 and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \bar{W}, \bar{S}_1 or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \bar{OE} directly controls the output stage. Setting the \bar{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

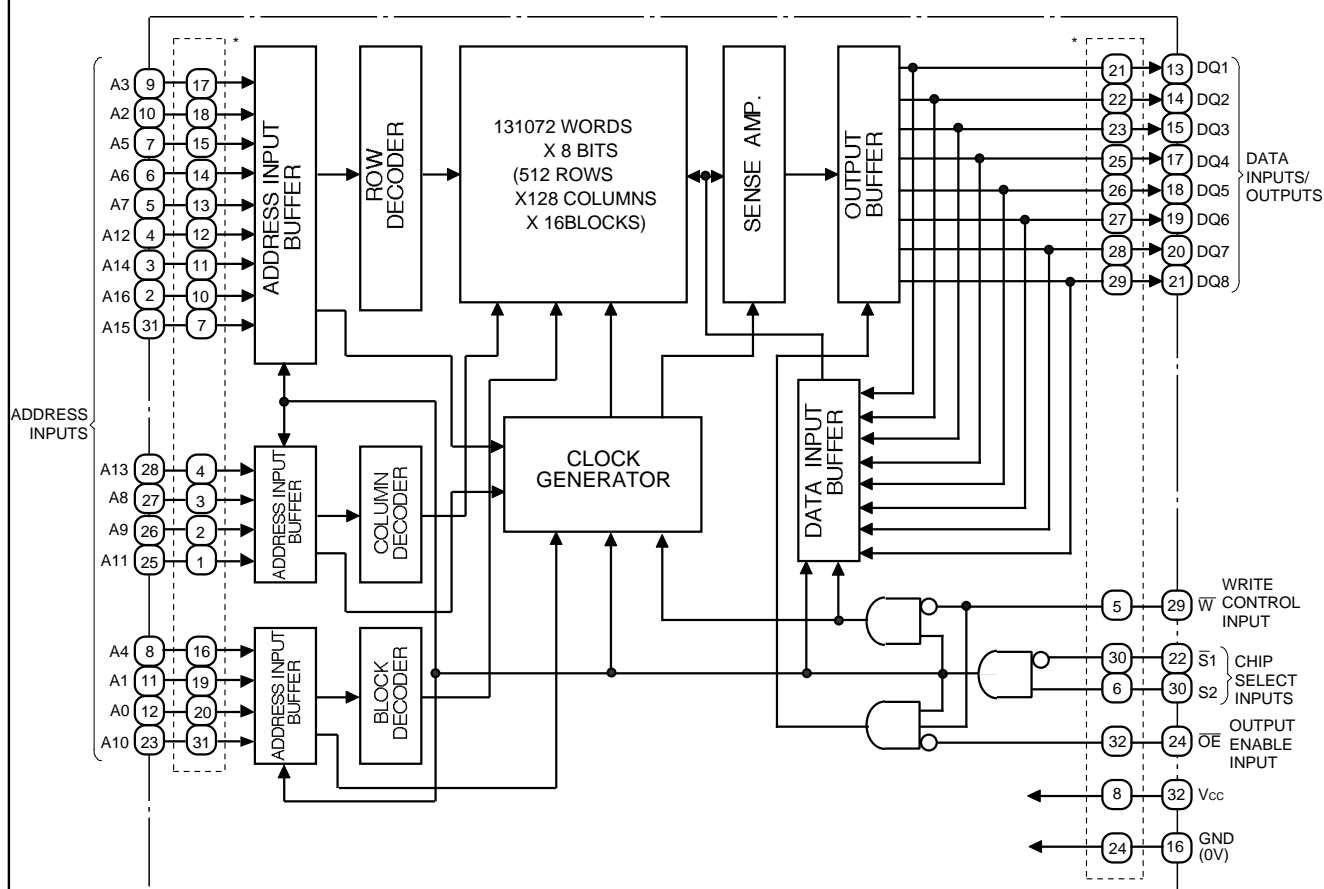
A read cycle is executed by setting \bar{W} at a high level and \bar{OE} at a low level while \bar{S}_1 and S_2 are in an active state($\bar{S}_1=L, S_2=H$).

When setting \bar{S}_1 at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \bar{S}_1 and S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

\bar{S}_1	S_2	\bar{W}	\bar{OE}	Mode	DQ	I _{CC}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	-0.3*~7	V
V _I	Input voltage		-0.3*~V _{CC} + 0.3	V
V _O	Output voltage		0~V _{CC}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

* -3.0V in case of AC (Pulse width 50ns)

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{CC} + 0.3	V
V _{IL}	Low-level input voltage		-0.3*		0.8	V
V _{OH}	High-level output voltage	I _{OH} = -1.0mA	2.4			V
		I _{OH} = -0.1mA	V _{CC} - 0.5			V
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4	V
I _I	Input current	V _I =0~V _{CC}			±1	μA
I _O	Output current in off-state	$\bar{S}_1=V_{IH}$ or $S_2=V_{IL}$ or $\bar{OE}=V_{IH}$ V _{I/O} =0~V _{CC}			±1	μA
I _{CC1}	Active supply current (AC, MOS level)	\bar{S}_1 0.2V, S ₂ V _{CC} -0.2V other inputs 0.2V or V _{CC} -0.2V Output-open(duty 100%)	55ns	39	80	mA
			70ns	34	70	
			1MHz	4	15	
I _{CC2}	Active supply current (AC, TTL level)	$\bar{S}_1=V_{IL}$, S ₂ =V _{IH} , other inputs=V _{IH} or V _{IL} Output-open(duty 100%)	55ns	42	85	mA
			70ns	37	70	
			1MHz	5	15	
I _{CC3}	Stand-by current	1) S ₂ 0.2V, other inputs=0~V _{CC} 2) \bar{S}_1 V _{CC} -0.2V, S ₂ V _{CC} -0.2V, other inputs=0~V _{CC}	-H			μA
			~25°C		2	
			~40°C		6	
I _{CC4}	Stand-by current	$\bar{S}_1=V_{IH}$ or S ₂ =V _{IL} , other inputs=0~V _{CC}				mA
			~70°C		20	

* -3.0V in case of AC (Pulse width 50ns)

CAPACITANCE (T_a=0~70°C, V_{CC}=5V±10% unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	FP,VP,RV,KV V _I =GND, V _I =25mVrms, f=1MHz			8	pF
C _O	Output capacitance	FP,VP,RV,KV V _O =GND, V _O =25mVrms, f=1MHz			10	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V_{CC} = 5V, T_a = 25°C

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, 5V±10% unless otherwise noted)**(1) MEASUREMENT CONDITIONS**Input pulse level $V_{IH}=2.4V, V_{IL}=0.6V$ (-70H) $V_{IH}=3.0V, V_{IL}=0.0V$ (-55H)

Input rise and fall time 5ns

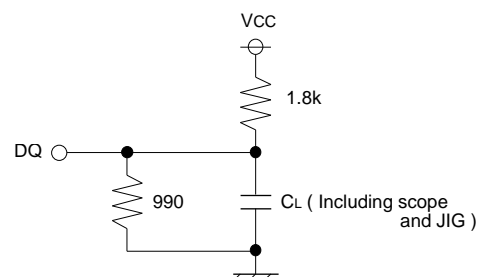
Reference level $V_{OH}=V_{OL}=1.5V$ Output loads Fig.1, $C_L=100pF$ (-70H) $C_L=30pF$ (-55H) $C_L=5pF$ (for t_{en}, t_{dis})Transition is measured ± 500mV from steady state voltage. (for t_{en}, t_{dis})

Fig.1 Output load

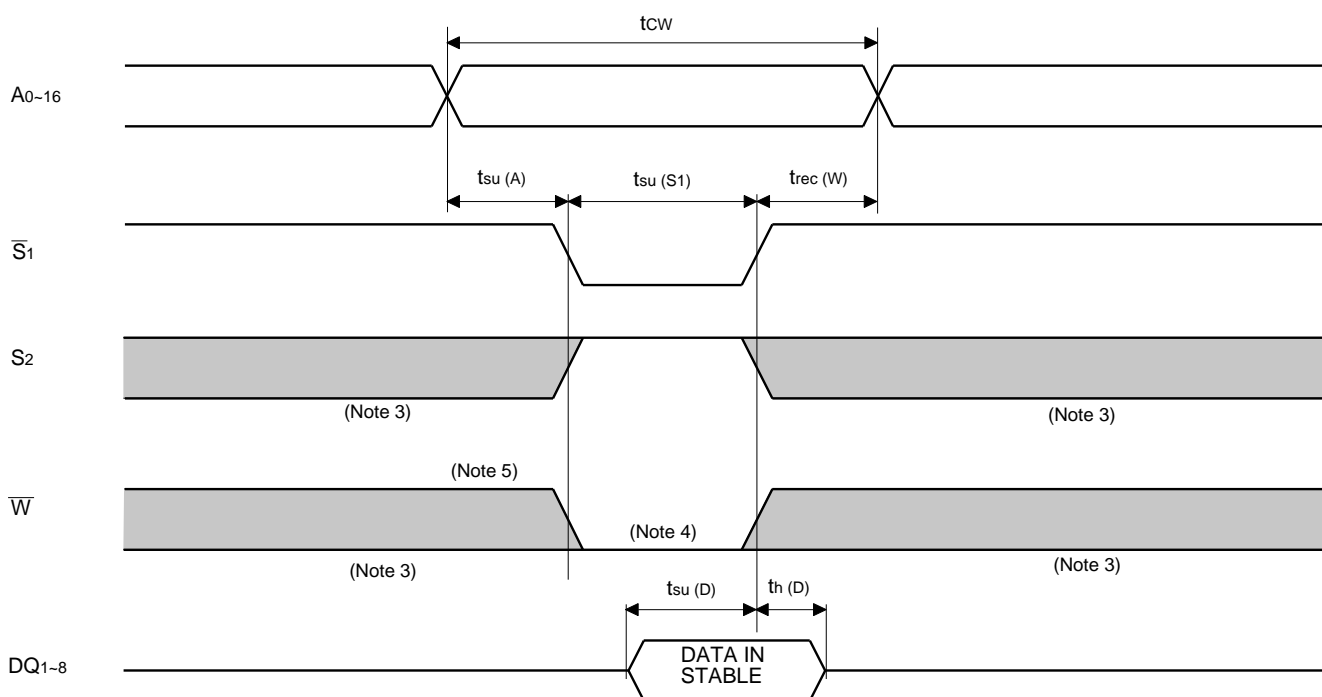
(2) READ CYCLE

Symbol	Parameter	Limits				Unit
		-55H		-70H		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		ns
$t_{a(A)}$	Address access time		55		70	ns
$t_{a(S1)}$	Chip select 1 access time		55		70	ns
$t_{a(S2)}$	Chip select 2 access time		55		70	ns
$t_{a(OE)}$	Output enable access time		30		35	ns
$t_{dis(S1)}$	Output disable time after $\overline{S1}$ high		20		25	ns
$t_{dis(S2)}$	Output disable time after $S2$ low		20		25	ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high		20		25	ns
$t_{en(S1)}$	Output enable time after $\overline{S1}$ low	5		10		ns
$t_{en(S2)}$	Output enable time after $S2$ high	5		10		ns
$t_{en(OE)}$	Output enable time after \overline{OE} low	5		5		ns
$t_{V(A)}$	Data valid time after address	5		10		ns

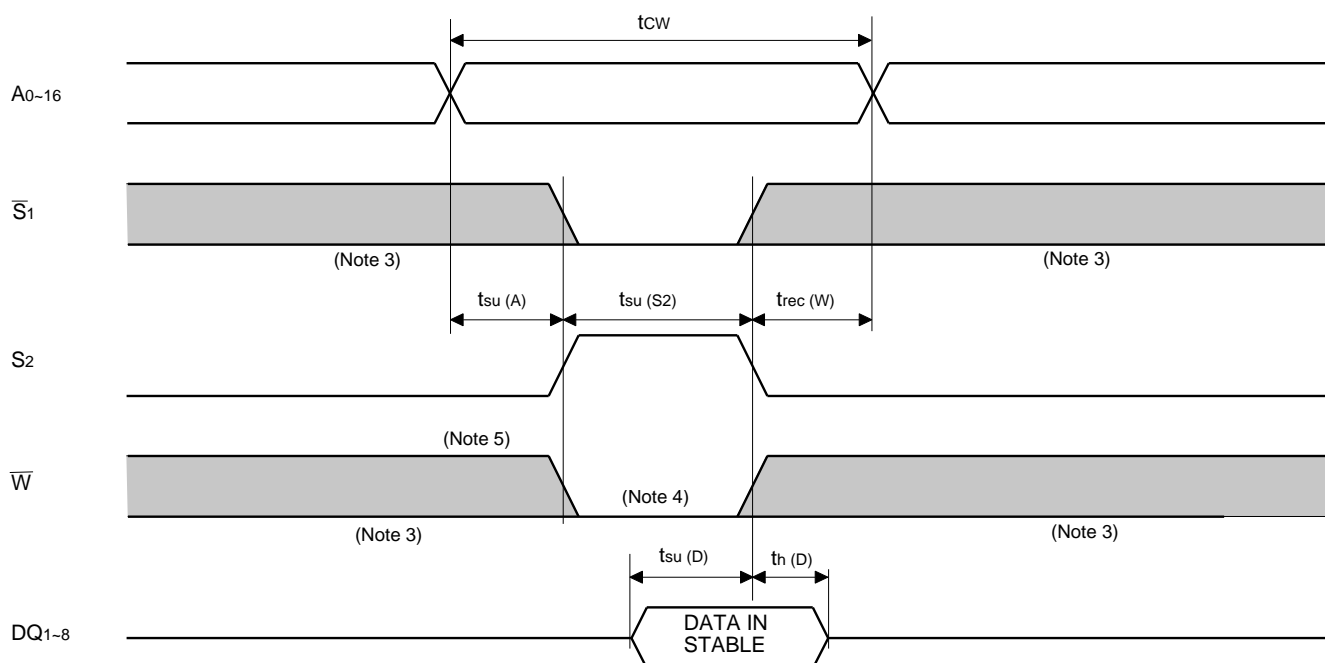
(3) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		-55H		-70H		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		ns
$t_{w(W)}$	Write pulse width	45		50		ns
$t_{su(A)}$	Address setup time	0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to \overline{W}	50		55		ns
$t_{su(S1)}$	Chip select 1 setup time	50		55		ns
$t_{su(S2)}$	Chip select 2 setup time	50		55		ns
$t_{su(D)}$	Data setup time	25		30		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time from \overline{W} low		20		25	ns
$t_{dis(OE)}$	Output disable time from \overline{OE} high		20		25	ns
$t_{en(W)}$	Output enable time from \overline{W} high	5		5		ns
$t_{en(OE)}$	Output enable time from \overline{OE} low	5		5		ns

Write cycle ($\overline{S1}$ control mode)



Write cycle ($S2$ control mode)



- Note 3: Hatching indicates the state is "don't care".
- 4: Writing is executed while $S2$ high overlaps $\overline{S1}$ and \overline{W} low.
- 5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of $S2$, the outputs are maintained in the high impedance state.
- 6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

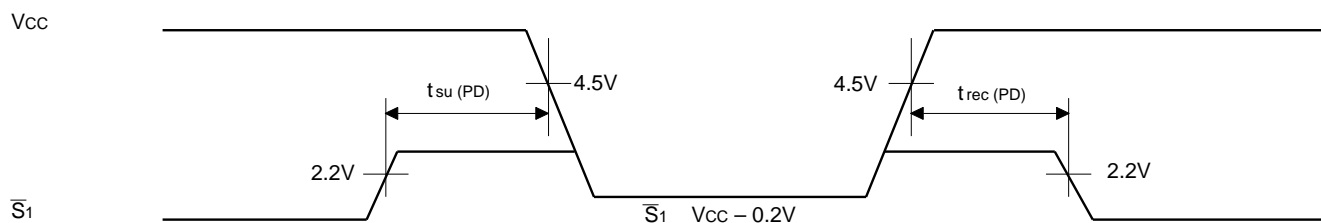
(1) ELECTRICAL CHARACTERISTICS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC} (PD)	Power down supply voltage		2.0			V
V _I (S ₁)	Chip select input \overline{S}_1	2.2V V _{CC} (PD) 2V V _{CC} (PD) 2.2V	2.2		V _{CC} (PD)	V
V _I (S ₂)	Chip select input S ₂	4.5V V _{CC} (PD) V _{CC} (PD)<4.5V			0.8 0.2	V
I _{CC} (PD)	Power down supply current	V _{CC} = 3V 1) S ₂ 0.2V, other inputs = 0~3V 2) \overline{S}_1 V _{CC} -0.2V, S ₂ V _{CC} -0.2V other inputs = 0~3V	-H	~25°C ~40°C ~70°C	1 3 10	μA

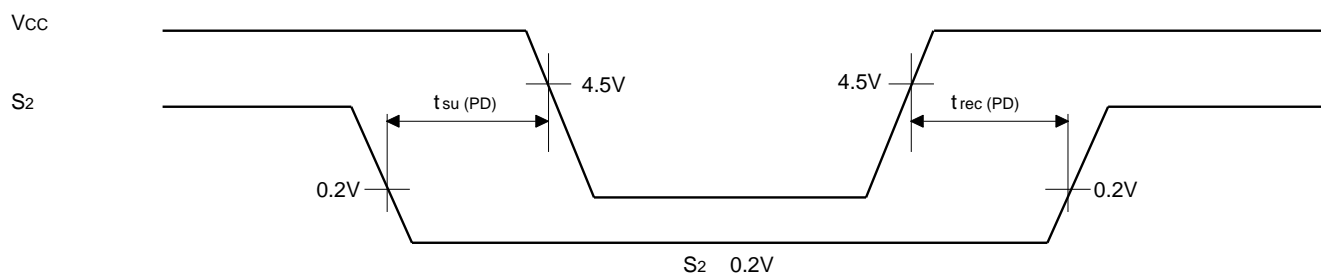
(2) TIMING REQUIREMENTS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

 \overline{S}_1 control mode

Note 7: On the power down mode by controlling \overline{S}_1 , the input level of S₂ must be S₂ V_{CC} - 0.2V or S₂ 0.2V. The other pins (Address, I/O, \overline{WE} , \overline{OE}) can be in high impedance state.

S₂ control mode

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