M5M54R01AJ-12,-15

1998.11.30 Ver.B

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change

4194304-BIT (4194304-WORD BY 1-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M54R01AJ is a family of 4194304-word by 1-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high speed application.

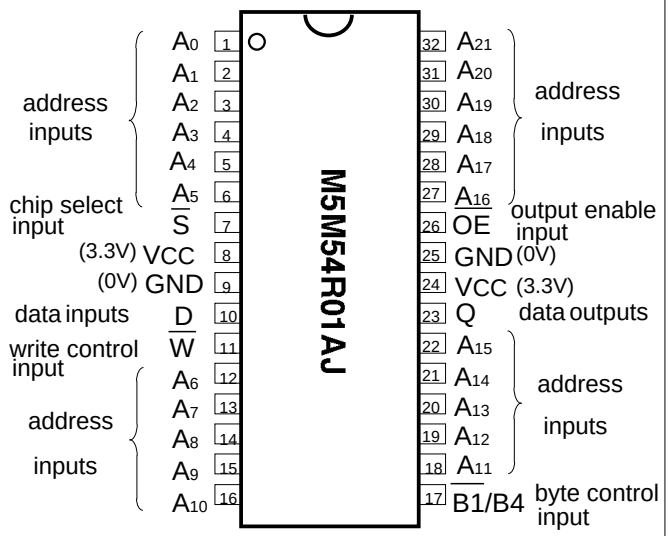
These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power down feature as well.

FEATURES

•Fast access time M5M54R01AJ-12 ... 12ns(max)
M5M54R01AJ-15 ... 15ns(max)

•Single +3.3V power supply
•Fully static operation : No clocks, No refresh
•Easy memory expansion by $\overline{S}$
•Three-state outputs : OR-tie capability
•$\overline{OE}$ prevents data contention in the I/O bus
•Directly TTL compatible : All inputs and outputs

PIN CONFIGURATION (TOP VIEW)



Outline 32P0K

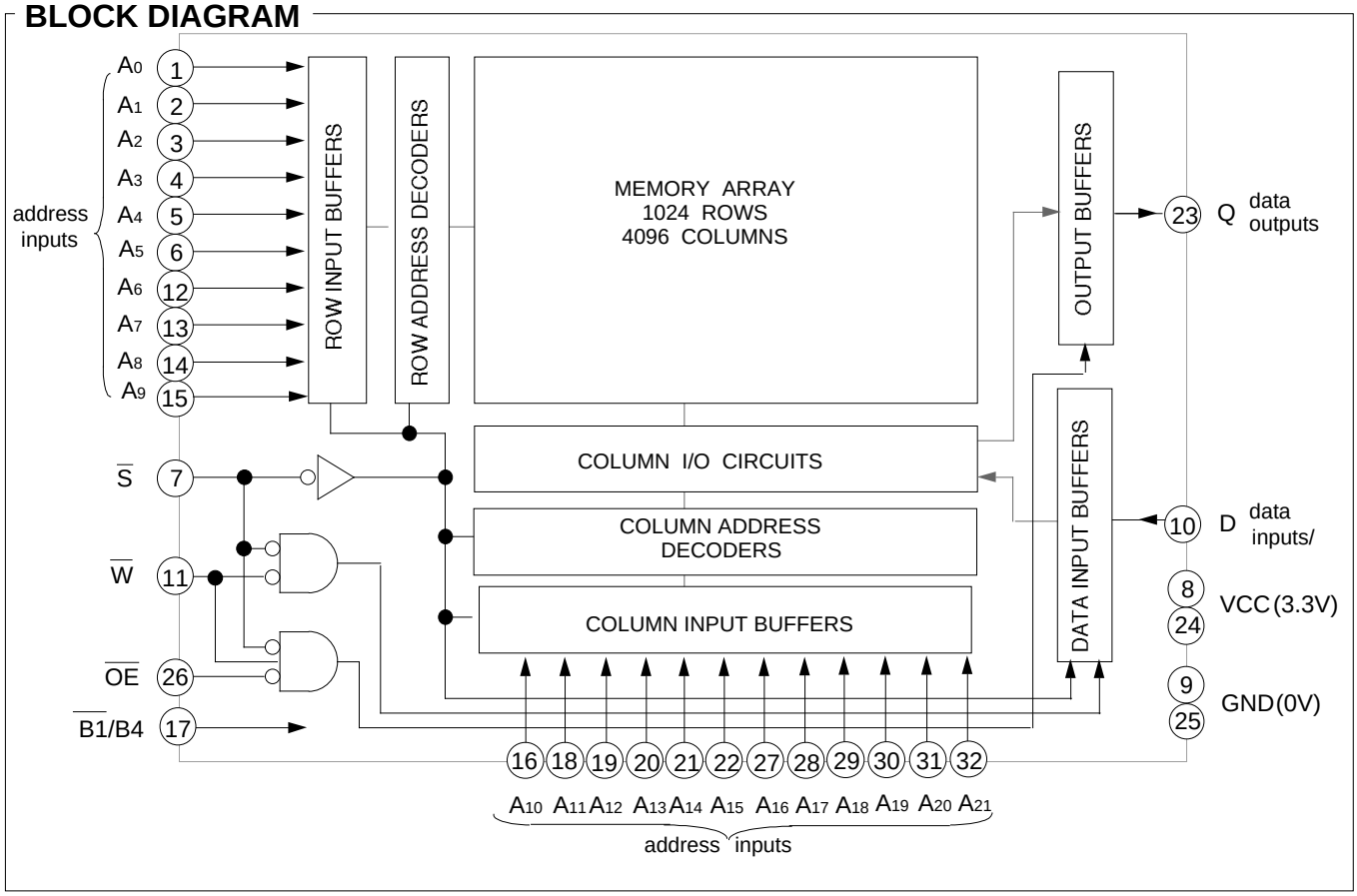
APPLICATION

High-speed memory units

PACKAGE

M5M54R01AJ : 32pin 400mil SOJ

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M54R01AJ is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is excuted by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state ($\overline{S}$=L).

When setting $\overline{S}$ at high level, the chip is in a non-selectable mode in which both reading and writing are disable. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$.

Signal-$\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissapation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

The RAM works with an organization of 4194304-word by 1bit, when $\overline{B1}$/B4 is low of floating. And an organization of 1048576-word by 4bit is also obtained for reducing the test time,when $\overline{B1}$/B4 is high. The pin configuration and function is as same as M5M54R04AJ.

FUNCTION TABLE

$\overline{B1}$/B4	$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	D	Q	Icc
L	H	X	X	Non selection	High-impedance	High-impedance	Stand by
L	L	L	X	Write	Din	High-impedance	Active
L	L	H	L	Read	High-impedance	Dout	Active
L	L	H	H		High-impedance	High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	- 2.0*~ 4.6	V
V_I	Input voltage		- 2.0*~ VCC+0.5	V
V_O	Output voltage		- 2.0*~ VCC	V
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg(bias)	Storage temperature(bias)		- 10 ~ 85	°C
Tstg	Storage temperature		- 65 ~ 150	°C

* Pulse width≦3ns, In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V $^{+10\%}_{-5\%}$,unless otherwise noted)

Symbol	Parameter	Condition			Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage				2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	I_{OH}= - 4mA			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA					0.4	V
I_I	Input current	V_I= 0 ~ Vcc					2	uA
$\lvert I_{OZ} \rvert$	Output current in off-state	$V_{I(\overline{S})}=V_{IH}$ $V_{I/O}$= 0 ~ Vcc					2	uA
I_{CC1}	Active supply current (TTL level)	$V_{I(\overline{S})}=V_{IL}$ other inpus=V_{IH} or V_{IL} Output-open(duty 100%)	AC	12ns cycle			180	mA
				15ns cycle			160	
			DC				90	
I_{CC2}	Stand by current (TTL level)	$V_{I(\overline{S})}=V_{IH}$	AC	12ns cycle			70	mA
				15ns cycle			60	
			DC				40	
I_{CC3}	Stand by current	$V_{I(\overline{S})}$=Vcc≧0.2V other inputs V_I≦0.2V or V_I ≧Vcc - 0.2V					10	mA

Note 1: Direction for current flowing into an IC is positive (no mark).

CAPACITANCE (Ta=0~70°C, Vcc=3.3V $^{+10\%}_{-5\%}$,unless otherwise noted)

Symbol	Parameter	Test Condition	Limit			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms,f=1MHz			8	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms,f=1MHz			8	pF

Note 2: C_I,C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V $^{+10\%}_{-5\%}$,unless otherwise noted)

(1)MEASUREMENT CONDITION

Input pulse levels ..... V_{IH}=3.0V, V_{IL}=0.0V
Input rise and fall time 3ns
Input timing reference levels ..... V_{IH}=1.5V, V_{IL}=1.5V
Output timing reference levels ..... V_{OH} =1.5V, V_{OL}=1.5V
Output loads Fig.1,Fig.2

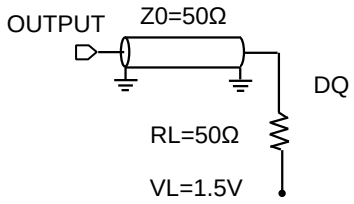


Fig.1 Output load

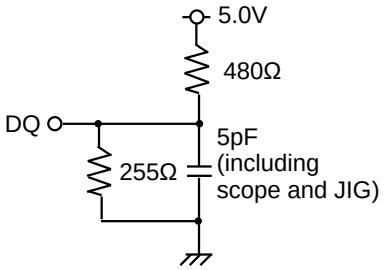


Fig.2 Output load for t_{en}, t_{dis}

(2)READ CYCLE

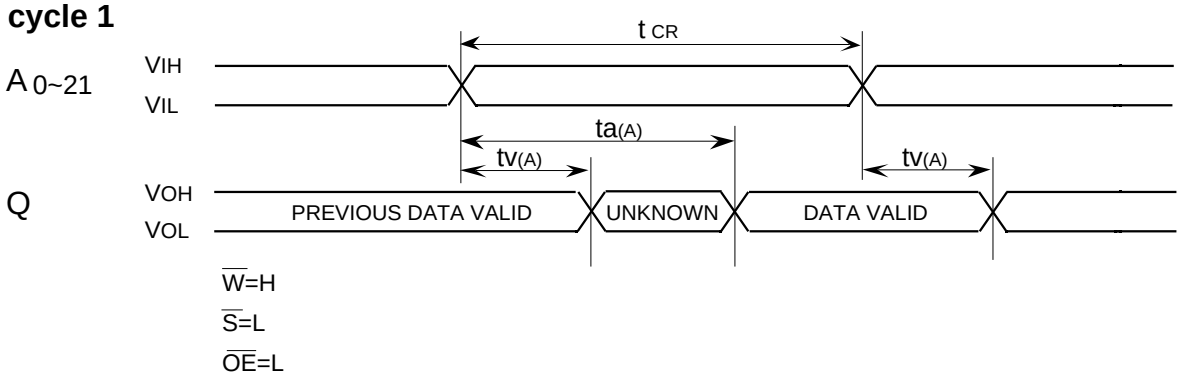
Symbol	Parameter	Limits				Unit
		M5M54R01AJ-12		M5M54R01AJ-15		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	12		15		ns
$t_{a(A)}$	Address access time		12		15	ns
$t_{a(S)}$	Chip select access time		12		15	ns
$t_{a(OE)}$	Output enable access time		6		7	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	6	0	7	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	6	0	7	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	3		3		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	1		1		ns
$t_{v(A)}$	Data valid time after address change	3		3		ns
tPU	Power-up time after chip selection	0		0		ns
tPD	Power-down time after chip selection		12		15	ns

(3)WRITE CYCLE

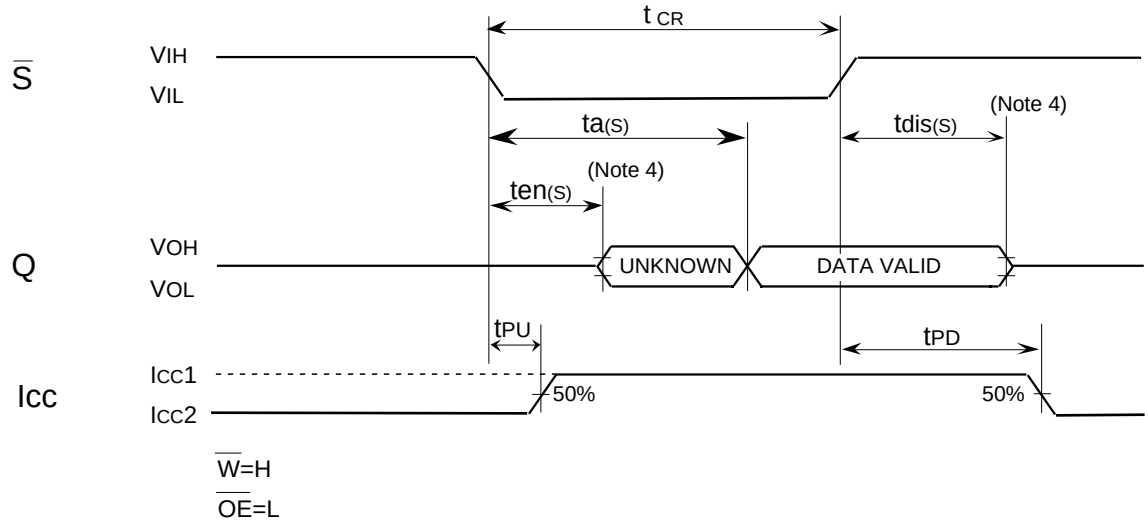
Symbol	Parameter	Limits				Unit
		M5M54R01AJ-12		M5M54R01AJ-15		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	12		15		ns
$t_{w(W)}$	Write pulse width ($\overline{OE}$ low)	12		15		ns
$t_{w(W)}$	Write pulse width($\overline{OE}$ high)	10		10		ns
$t_{su(A)1}$	Address setup time($\overline{W}$)	0		0		ns
$t_{su(A)2}$	Address setup time($\overline{S}$)	0		0		ns
$t_{su(S)}$	Chip select setup time	10		10		ns
$t_{su(D)}$	Data setup time	6		7		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	1		1		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	6	0	7	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	6	0	7	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ High	10		10		ns

(4)TIMING DIAGRAMS

Read cycle 1

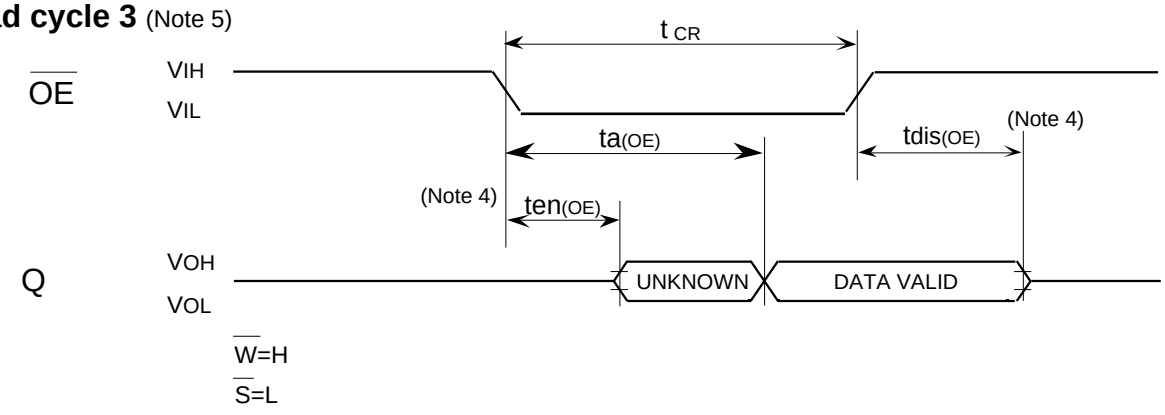


Read cycle 2 (Note 3)



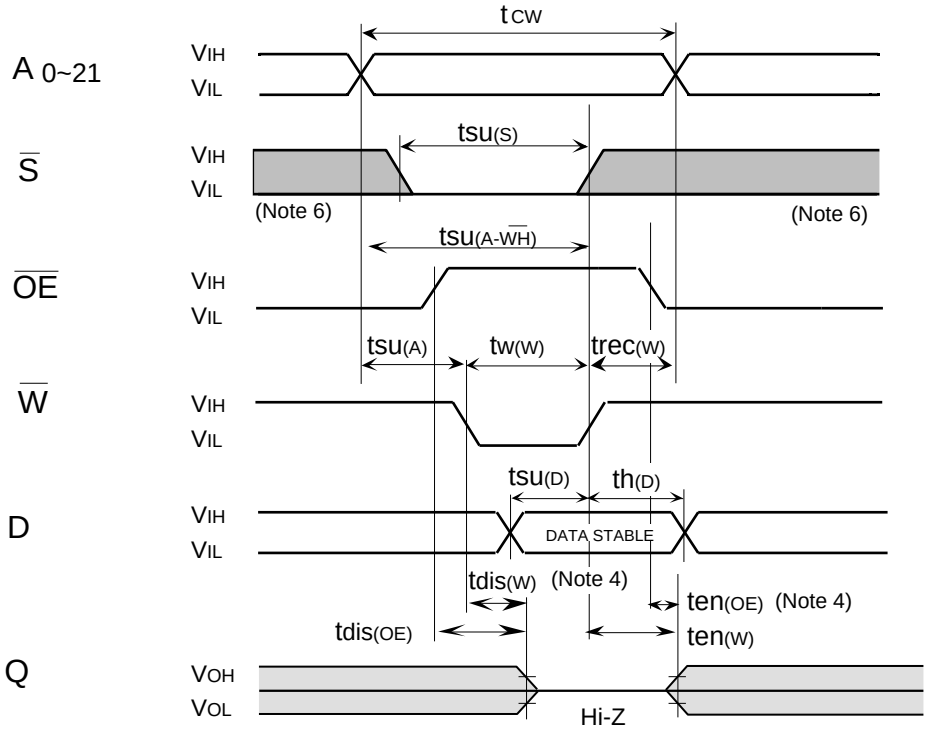
Note 3. Addresses valid prior to or coincident with S transition low.
4. Transition is measured ±500mv from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 5)

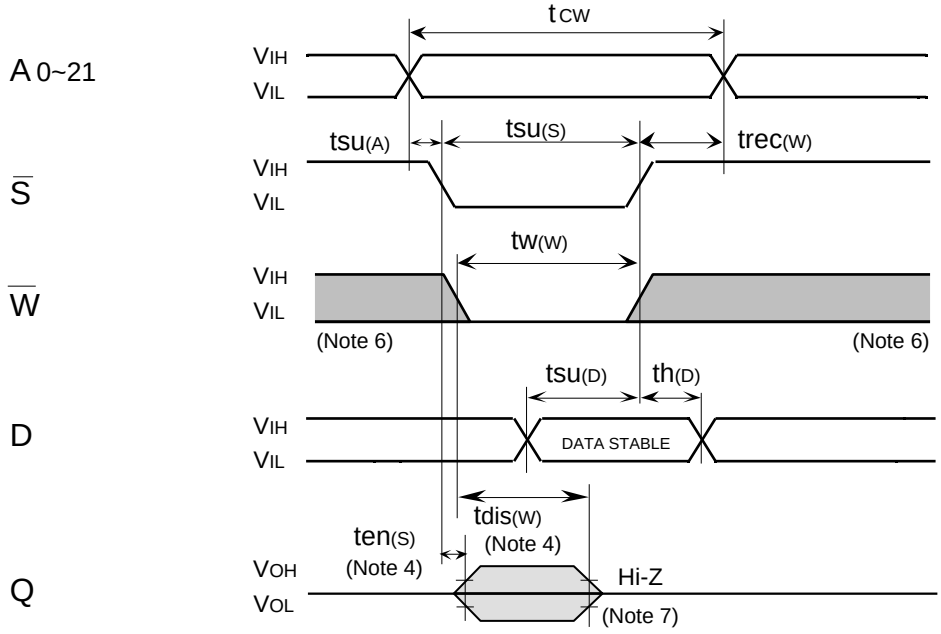


Note 5. Addresses and S valid prior to OE transition low by (ta(A)-ta(OE)), (ta(S)-ta(OE))

Write cycle ($\overline{W}$ control mode)



Write cycle($\overline{S}$ control)



Note 6: Hatching indicates the state is don't care.

7: When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

8: ten,tdis are periodically sampled and are not 100% tested.