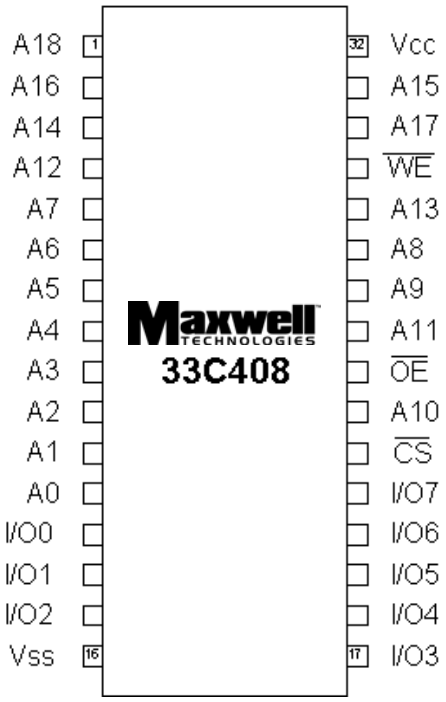
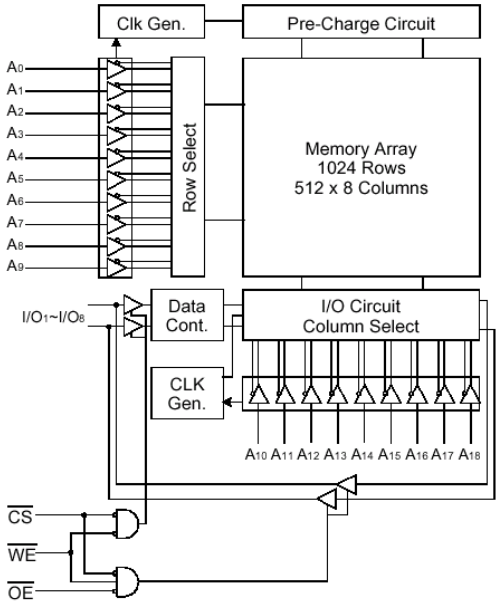
33C408
4 Megabit (512K x 8-Bit) CMOS SRAM





Logic Diagram

FEATURES:

- RAD-PAK® Technology radiation-hardened against natural space radiation
- 524,288 x 8 bit organization
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Excellent Single Event Effect
- - SEL_{TH}: > 68 MeV/mg/cm^2
- - SEU_{TH}: = 3 MeV/mg/cm^2
  - SEU saturated cross section: 6E-9 cm^2/bit
- Package:
  - 32-Pin RAD-PAK® flat pack
  - 32-Pin Non-RAD-PAK® flat pack
- Fast access time:
  - 20, 25, 30 ns maximum times available
- Single 5V ± 10% power supply
- Fully static operation
  - No clock or refresh required
- Three state outputs
- TTL compatible inputs and outputs
- Low power:
  - Standby: 60 mA (TTL); 10 mA (CMOS)
  - Operation: 180 mA (20 ns); 170 mA (25 ns); 160 mA (30 ns)

DESCRIPTION:

Maxwell Technologies' 33C408 high-density 4 Megabit SRAM microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. Using Maxwell's radiation-hardened RAD-PAK® packaging technology, the 33C408 realizes a high density, high performance, and low power consumption. Its fully static design eliminates the need for external clocks, while the CMOS circuitry reduces power consumption and provides higher reliability. The 33C408 is equipped with eight common input/output lines, chip select and output enable, allowing for greater system flexibility and eliminating bus contention. The 33C408 features the same advanced 512K x 8-bit SRAM, high-speed, and low-power demand as the commercial counterpart.

Maxwell Technologies' patented RAD-PAK packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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Table 1. Pinout Description

Pin	Symbol	Description
12-5, 27, 26, 23, 25, 4, 28, 3, 31, 2, 30, 1	A0-A18	Address Inputs
29	$\overline{WE}$	Write Enable
22	$\overline{CS}$	Chip Select
24	$\overline{OE}$	Output Enable
13-15, 17-21	I/O 1-I/O 8	Data Inputs/Outputs
32	V_{CC}	Power (+5.0V)
16	V_{SS}	Ground

Table 2. 33C408 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5	7.0	V
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	V_{CC} +0.5	V
Power Dissipation	P_D	--	1.0	W
Storage Temperature	T_S	-65	+150	˚C
Operating Temperature	T_A	-55	+125	˚C

Table 3. Delta Limits

Parameter	Variation
I_{CC1}	±10% of stated vaule in Table 6
I_{CC2}	±10% of stated vaule in Table 6
I_{CC3}	±10% of stated vaule in Table 6
I_{LI}	±10% of stated vaule in Table 6

TABLE 4. 33C408 RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5.0 ± 10%, T_A = -55 TO +125 ˚C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5.5	V
Ground	V_{SS}	0	0	V
Input High Voltage [1]	V_{IH}	2.2	V_{CC}+0.5	V
Input Low Voltage [2]	V_{IL}	-0.5	0.8	V
Thermal Impedance	Θ_{JC}	--	1.21	°C/W

1. V_{IH} (max) = V_{CC} +2.0V ac (pulse width ≤ 10 ns) for I ≤ 20 mA
2. V_{IL} (min) = -2.0V ac(pulse width ≤ 10 ns) for I ≤ 20 mA

TABLE 5. 33C408 CAPACITANCE

(f = 1.0 MHz, dV = 3.0V, T_A = 25 ˚C)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Input Capacitance[1] $\overline{CS1}$ - $\overline{CS4}$, $\overline{OE}$, $\overline{WE}$ I/O0-7, I/O8-15, I/O16-23, I/O24-31	C_{IN}	V_{IN} = 0 V	 7 28 7	pF
Input / Output Capacitance[1]	C_{OUT}	$V_{I/O}$ = 0 V	8	pF

1. Guaranteed by design.

TABLE 6. 33C408 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55 TO +125 ˚C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}	-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT} =V_{SS} to V_{CC}	-2	2	µA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	--	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	--	V
Operating Current -20 -25 -30	I_{CC}	Min cycle, 100% Duty, $\overline{CS}$=V_{IL}, I_{OUT}=0mA, V_{IN} = V_{IH} or V_{IL}	 -- -- --	 180 170 160	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, Min Cycle	--	60	mA
Input Capacitance [1]	C_{IN}	V_{IN} = 0V, f = 1MHz, T_A = 25 °C	--	7	pF

TABLE 6. 33C408 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Output Capacitance [1]	$C_{I/O}$	$V_{I/O}$ = 0V	--	8	pF

1. Guaranteed by design.

TABLE 7. 33C408 AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 ± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE NOTED)

PARAMETER	MIN	TYP	MAX	UNITS
Input Pulse Level	0.0	--	3.0	V
Output Timing Measurement Reference Level	--	--	1.5	V
Input Rise/Fall Time	--	--	3.0	ns
Input Timing Measurement Reference Level	--	--	1.5	V

TABLE 8. 33C408 AC CHARACTERISTICS FOR READ CYCLE

(V_{CC} = 5V ± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Read Cycle Time	t_{RC}				ns
-20		20	--	--	
-25		25	--	--	
-30		30	--	--	
Address Access Time	t_{AA}				ns
-20		--	--	20	
-25		--	--	25	
-30		--	--	30	
Chip Select Access Time	t_{CO}				ns
-20		--	--	20	
-25		--	--	25	
-30		--	--	30	
Output Enable to Output Valid	t_{OE}				
-20		--	--	10	ns
-25		--	--	12	
-30		--	--	14	
Chip Enable to Output in Low-Z	t_{LZ}				ns
-20		--	3	--	
-25		--	3	--	
-30		--	3	--	
Output Enable to Output in Low-Z	t_{OLZ}				ns
-20		--	0	--	
-25		--	0	--	
-30		--	0	--	

TABLE 8. 33C408 AC CHARACTERISTICS FOR READ CYCLE

(V_{CC} = 5V ± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Chip Deselect to Output in High-Z	t_{HZ}				ns
-20		--	5	--	
-25		--	6	--	
-30		--	8	--	
Output Disable to Output in High-Z	t_{OHZ}				ns
-20		--	5	--	
-25		--	6	--	
-30		--	8	--	
Output Hold from Address Change	t_{OH}				ns
-20		3	--	--	
-25		5	--	--	
-30		6	--	--	
Chip Select to Power Up Time	t_{PU}				ns
-20		--	0	--	
-25		--	0	--	
-30		--	0	--	
Chip Select to Power Down Time	t_{PD}				ns
-20		--	10	--	
-25		--	15	--	
-30		--	20	--	

TABLE 9. 33C408 FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O PIN	SUPPLY CURRENT
H	X[1]	X[1]	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X[1]	Write	D_{IN}	I_{CC}

1. X = don't care.

TABLE 10. 33C408 AC CHARACTERISTICS FOR WRITE CYCLE

(V_{CC} = 5V ± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Write Cycle Time	t_{WC}				ns
-20		20	--	--	
-25		25	--	--	
-30		30	--	--	

TABLE 10. 33C408 AC CHARACTERISTICS FOR WRITE CYCLE

(V_{CC} = 5V ± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Chip Select to End of Write	t_{CW}				ns
-20		14	--	--	
-25		15	--	--	
-30		17	--	--	
Address Setup Time	t_{AS}				ns
-20		0	--	--	
-25		0	--	--	
-30		0	--	--	
Address Valid to End of Write	t_{AW}				ns
-20		14	--	--	
-25		15	--	--	
-30		17	--	--	
Write Pulse Width ($\overline{OE}$ High)	t_{WP}				ns
-20		14	--	--	
-25		15	--	--	
-30		17	--	--	
Write Recovery Time	t_{WR}				ns
-20		0	--	--	
-25		0	--	--	
-30		0	--	--	
Write to Output in High-Z	t_{WHZ}				ns
-20		--	5	--	
-25		--	5	--	
-30		--	6	--	
Write Pulse Width ($\overline{OE}$ Low)	t_{WP1}				ns
-20		--	22	--	
-25		--	24	--	
-30		--	26	--	
Data to Write Time Overlap	t_{DW}				ns
-20		9	--	--	
-25		10	--	--	
-30		11	--	--	
End Write to Output Low-Z	t_{OW}				ns
-20		--	6	--	
-25		--	7	--	
-30		--	8	--	
Data Hold from Write Time	t_{DH}				ns
-20		0	--	--	
-25		0	--	--	
-30		0	--	--	

FIGURE 1. AC TEST LOADS

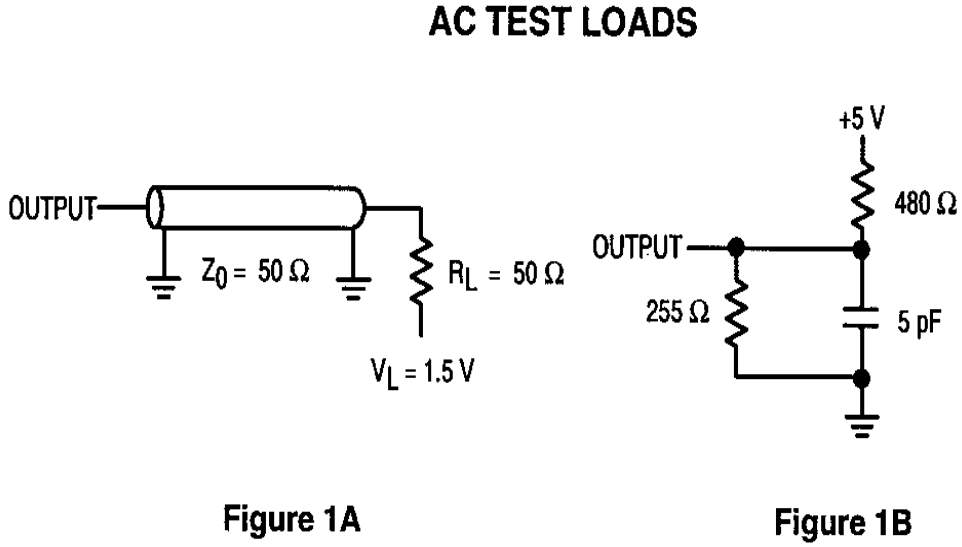


FIGURE 2. TIMING WAVEFORM OF READ CYCLE(1)

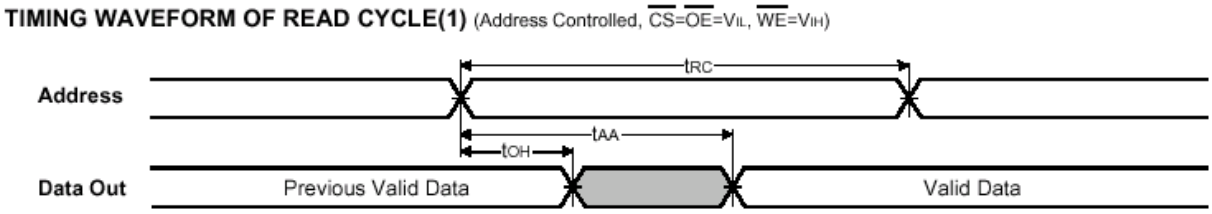
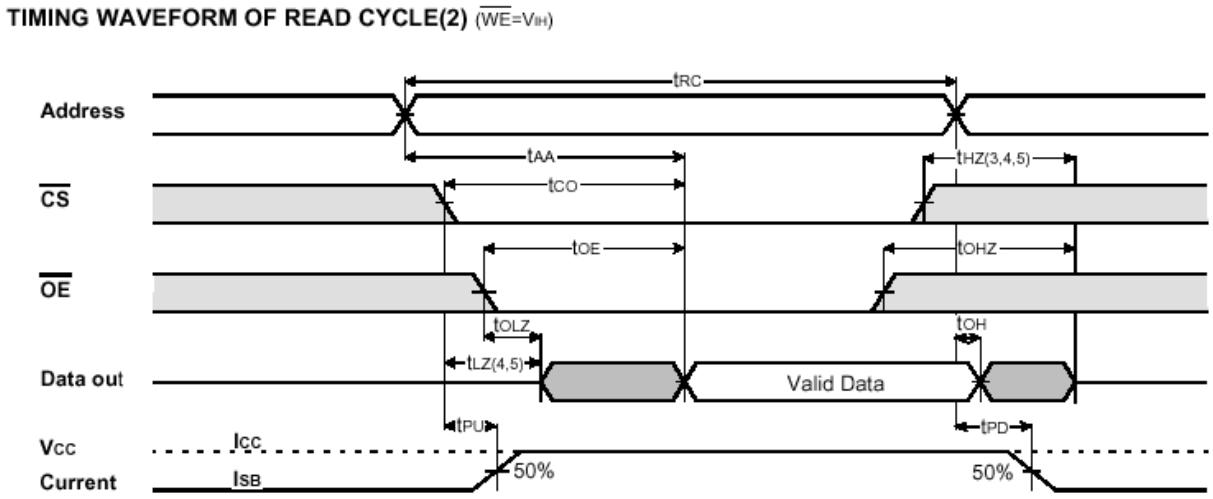


FIGURE 3. TIMING WAVEFORM OF READ CYCLE (2)



Read Cycle Notes:

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced form the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ(max)}$ is less than $t_{LZ(min)}$ both for a given device and from device to device.
5. Transition is measured + 200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with CS = V_{IL}.
7. Address valid prior to coincident with CS transition low.
8. For common I/O applications, minimization or elimination of bus contention condition is necessary during read and write cycle.

FIGURE 4. TIMING WAVEFORM OF WRITE CYCLE(1)

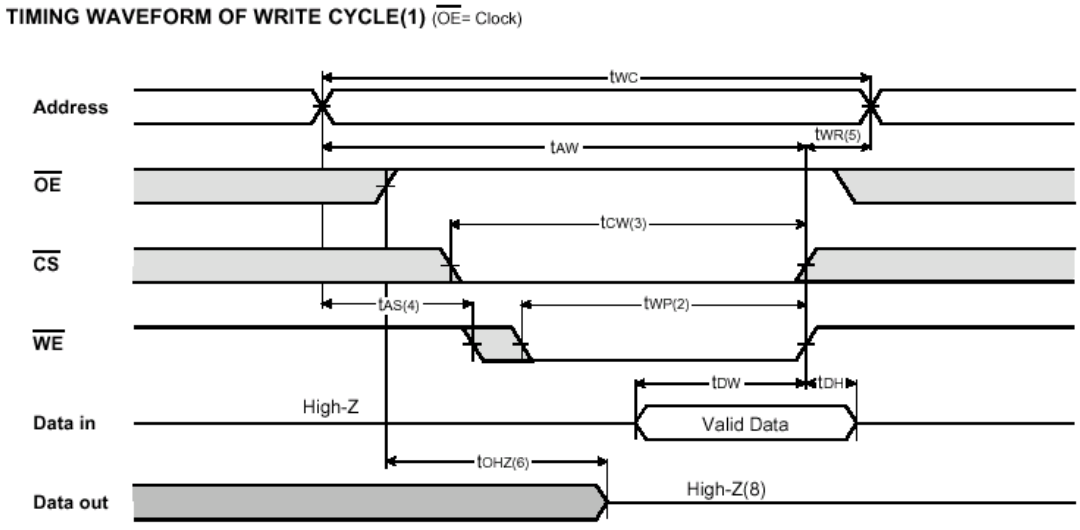


FIGURE 5. TIMING WAVEFORM OF WRITE CYCLE(2)

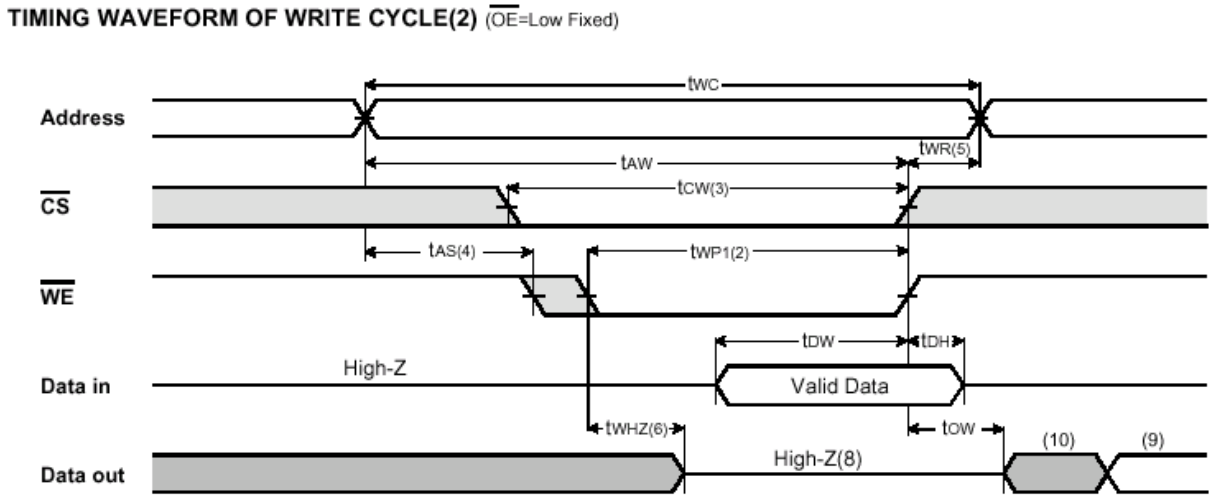
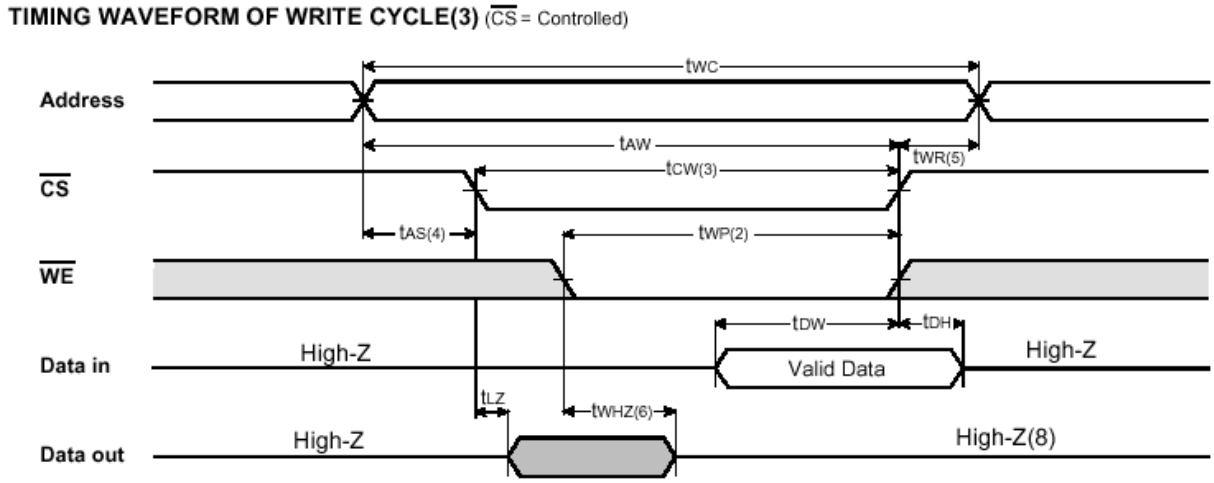


FIGURE 6. TIMING WAVEFORM OF WRITE CYCLE (3)



WRITE CYCLE NOTE:

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{wp} is measured from beginning of write to the end of write.
3. t_{cw} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured form the end of write to the address change. TWR applied in case a write ends as $\overline{CS}$, or $\overline{WR}$ going high.

6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. $\overline{IC}$ $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FIGURE 7. SRAM HEAVY ION CROSS SECTION

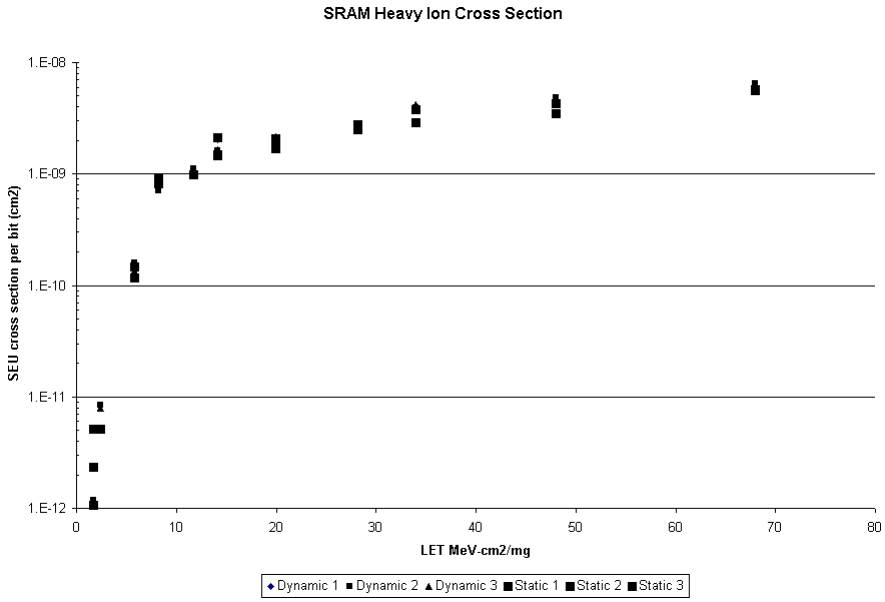
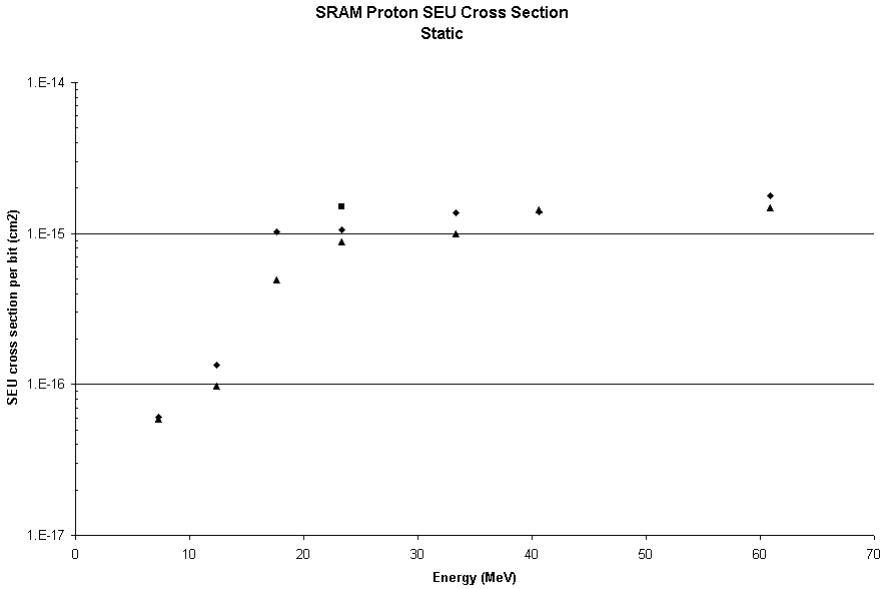
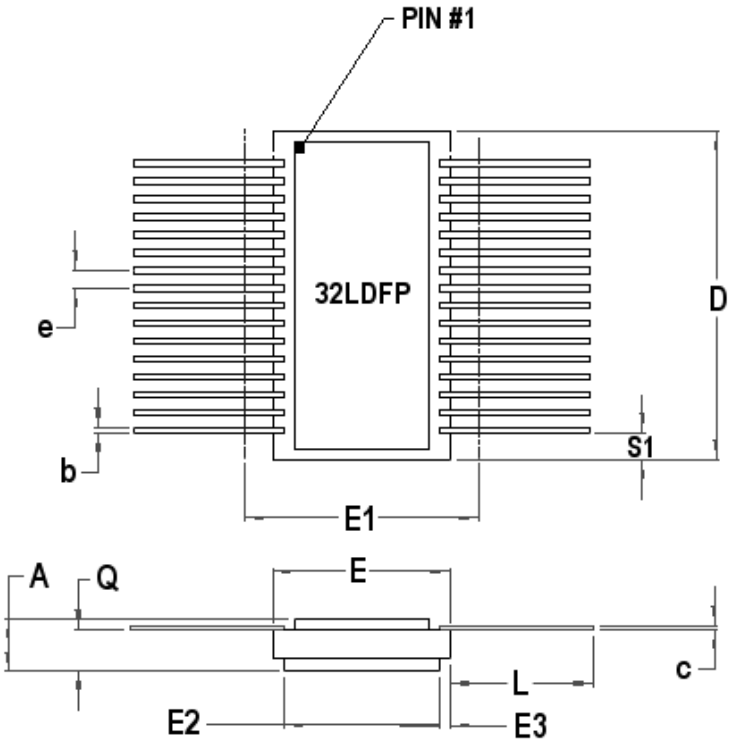


FIGURE 8. SRAM PROTON SEU CROSS SECTION STATIC





32 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.120	0.135	0.155
b	0.013	0.015	0.020
c	0.008	0.010	0.012
D	--	0.930	0.940
E	0.635	0.645	0.655
E1	--	--	0.690
E2	0.550	0.565	--
E3	0.030	0.040	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.026	0.098	--
S1	0.005	0.082	--
N	32		

F32-06

Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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