DESCRIPTION

The LD4100 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire EEPR4 1,7 code read channel for zoned recording hard disk drive systems with data rates from 34 to 120 Mbit/s.

Functional blocks include AGC, programmable filter, Maximum Likelihood (ML) Detector, 1,7 ENDEC, data synchronizer, time base generator, servo data detector, and 4-burst servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones.

1,7 RLL code operation is used to reduce the magnetic media flux transitions per inch and the write current rise time requirements.

GENERAL FEATURES

- Register programmable data rates from 34 to 120 Mbit/s
- Sampled data read channel with maximum likelihood (ML) detector
- Programmable filter with asymmetrical zeros to compensate pulse asymmetry
- 1,7 RLL ENDEC
- Data scrambler/descrambler
- Low operating power (0.95 W typical at 5 V)
- Register programmable power management (<5mW power-down mode)
- Dual bit NRZ data interface
- Serial interface port for access to internal program storage registers
- Single power supply (5 V ± 10%)
- Small footprint 100-Lead TQFP package to internal

AUTOMATIC GAIN CONTROL

- Dual mode AGC, continuous time during acquisition, sampled during data reads
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents for data reads
- Charge pump currents track programmable data rate during data reads
- Low drift AGC hold circuitry
- Automatic AGC fast recovery and input Low-Z modes with programmable time durations
- Wide bandwidth, precision full-wave rectifier
- 3-bit DAC to control AGC voltage in servo mode between 0.8 and 1.5 V

FILTER / EQUALIZER

Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:

- Channel filter and pulse slimming equalization for equalization to EEPR4
- Programmable cutoff frequency from 6 to 38 MHz
- Programmable boost/equalization of 0 to 17 dB
- Programmable asymmetrical zeros equalization to correct pulse shape asymmetry
- Low-Z switch for fast offset recovery at the filter output
- Internal AC coupling

PULSE QUALIFICATION

- Sampled Maximum Likelihood data detector with fixed EEPR4 target detection
- With white gaussian noise, within 0.5 dB of ideal Viterbi detector at user density of 2
- Register programmable qualification thresholds for servo reads
- Selectable hysteresis or window qualification modes for servo reads

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 180 MHz frequency output
- Independent M and N divide-by registers

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 1,7 RLL ENDEC
- Register programmable to 120 Mbits operation
- Fast acquisition, zero phase restart, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 2-bit NRZ data interface
- Data rate tracking, programmable write precompensation for non-linear transition shift
- Differential PECL write data output with power reduction
- Integrated dual byte sync detection
- Programmable offset to compensate for MR head asymmetry

SERVO

- 4-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- "Soft Landing" charge pump architecture with programmable charge pump current
- Separate, automatically selected, registers for servo Fc, boost, and threshold
- Wide bandwidth, precision full-wave rectifier with programmable offset to compensate for MR head asymmetry.
- RDS and PPOL outputs for servo timing support

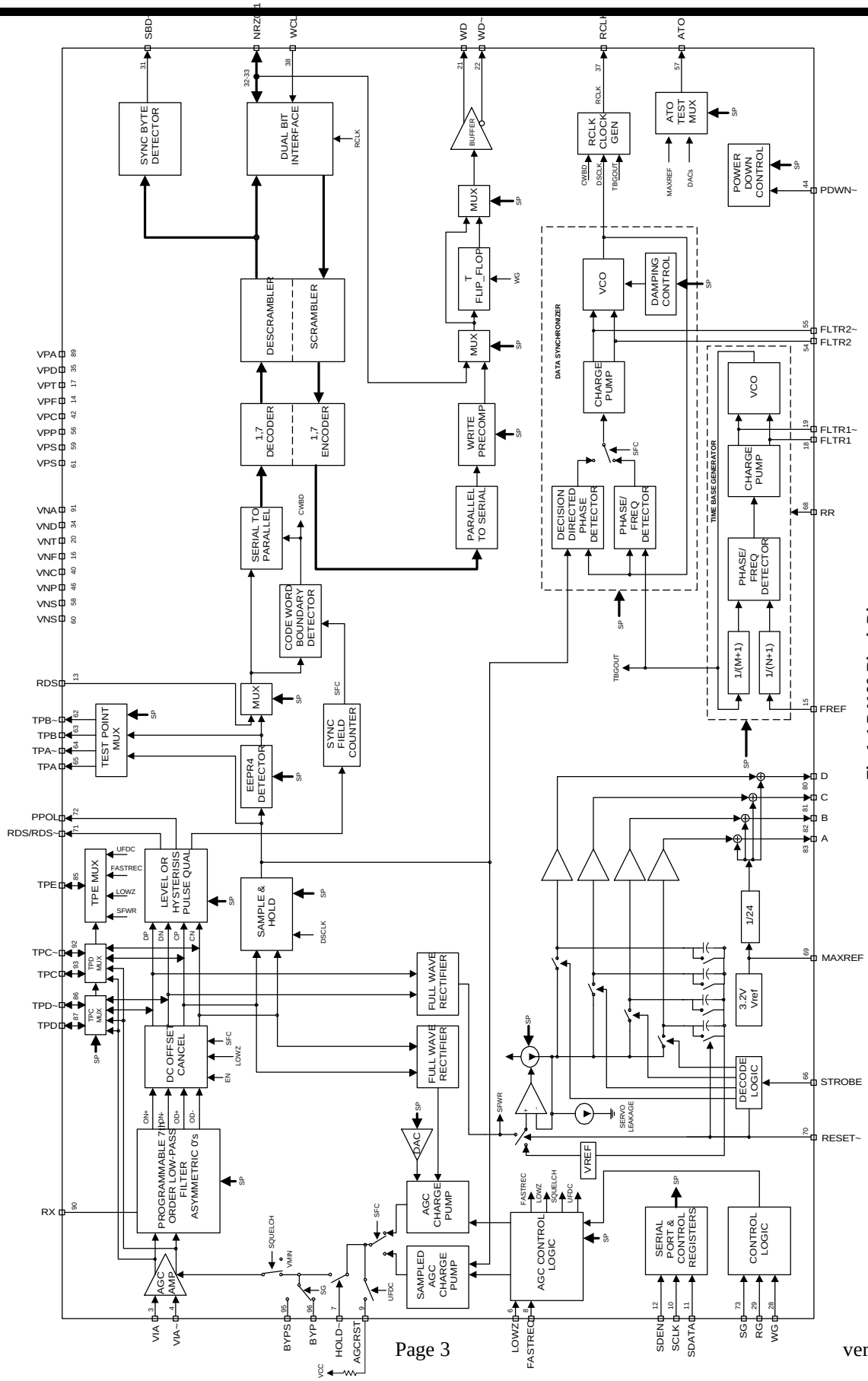
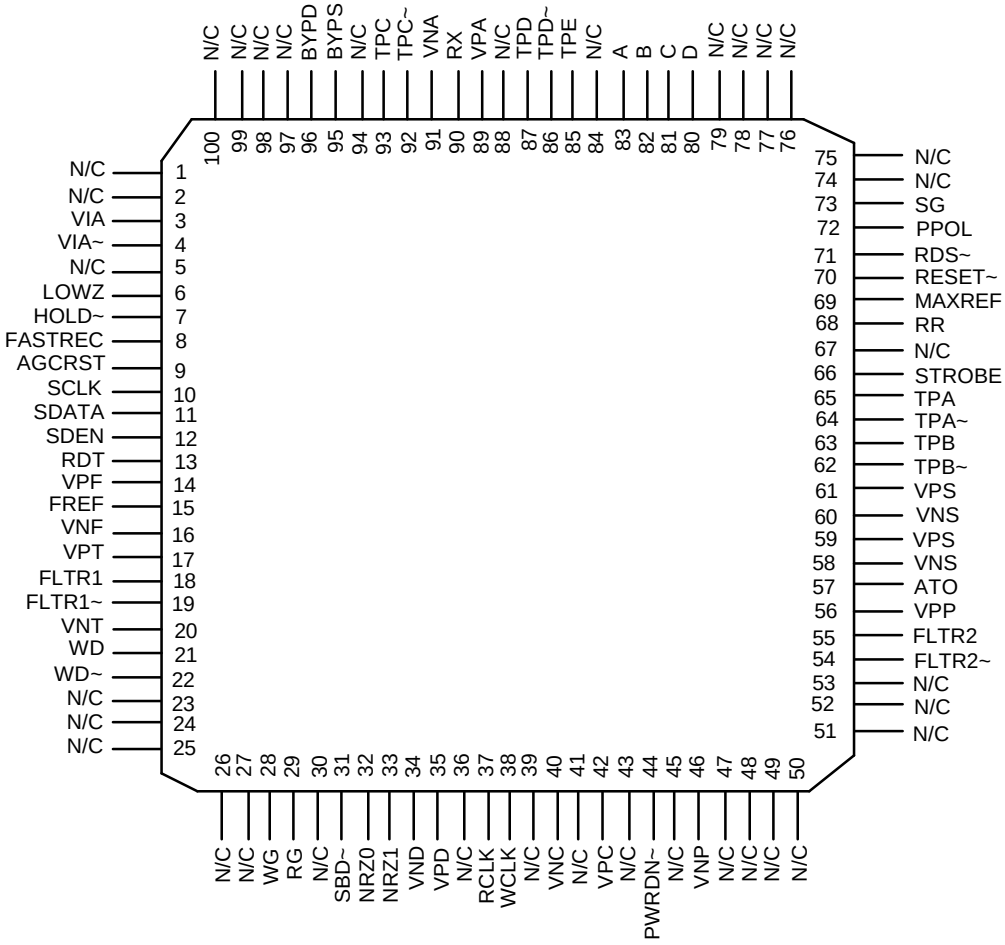


Fig 1 LD4100 Block Diagram



LD4100
100-Lead TQFP