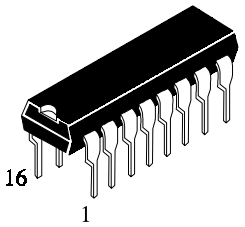
**IN91531**

# PARALLEL INPUT TONE/PULSE DIALER

## High-Performance Silicon-Gate CMOS



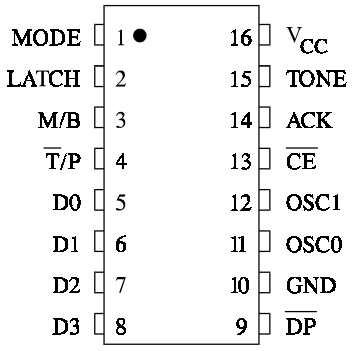

N SUFFIX
PLASTIC

**ORDERING INFORMATION**
IN91531N
$T_A$ = -10° to 70° C

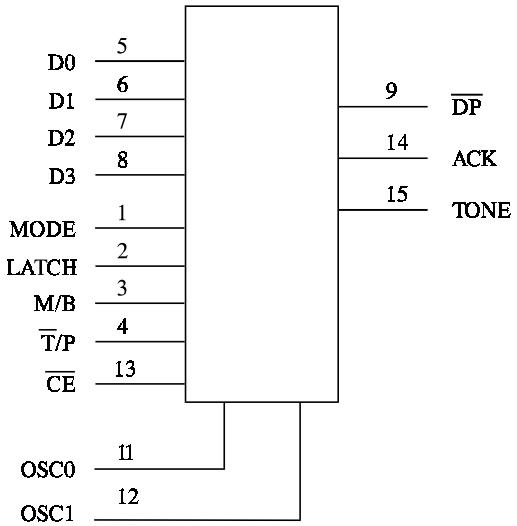
The IN91531 provides a 4-bit data input and a handshaking signal to serve as microcomputer interfaces. Under microcomputer control the IN91531 generates both a DTMF signal and a pulse output for telephone dialing. All necessary dual-tone frequencies and dial pulse outputs are derived from the widely used TV crystal standard, providing high accuracy and stability. The required sinusoidal waveform for individual tones is digitally synthesized on the chip, resulting in a waveform with very low total harmonic distortion.

- 4-bit parallel data input from microcomputer
- TTL compatible inputs and outputs
- Uses TV crystal standard (3.58 MHz) to derive all frequencies, providing high accuracy and stability
- Operating voltage: 2.5 to 5.5 Volts
- Selectable M/B ratio
- 10 PPS dial rate
- DTMF signaling of digits 0 9, *, #, A, B, C, and D
- Pulse signaling of 0 ~ 9, *, #, and A
- High group tone pre-emphasis: 2 dB
- Low total harmonic distortion in DTMF signaling

### PIN ASSIGNMENT




### LOGIC DIAGRAM




PIN 10 = GND
PIN 16 = $V_{CC}$

## PIN DESCRIPTION

| Pin No. | Designation | DESCRIPTION |
|---|---|---|
| 1 | MODE | Tone mode select input.<br>When this input is high, the tone output and ASK output are normal. When this input is low, a DTMF signal will be generated continuously and any new input data will be ignored.<br>This input affects the tone output mode only. |
| 2 | LATCH | Latch input.<br>When input on this pin changes from low to high (at the rising edge), the IN91531 latches the 4-bit input data and T/P input. The latch input should not be changed back from low to high again until the ASK output falls low, and new data must not be latched while the ASK output is still low. |
| 3 | M/B | Make/Break ratio select input.<br>This pin is used to select one of two available make/break ratios. A high input selects the 2/3 make/break ratio; a low input selects the 1/23 ratio. This input should be connected to $V_{CC}$ or GND only. Changing the state of this pin when $\overline{CE}$ is active (low) enables the test mode. |
| 4 | $\overline{T/P}$ | Tone/pulse mode select input.<br>This input determines whether tone or pulse mode will be activated. It is latched together with the 4-bit data input. |
| 5 - 8 | D0 - D3 | 4-bit data input pins.<br>This 4-bit parallel input is used to receive data generated by the microcomputer. (Input data vs. output signal is shown in table 1.) Valid input data should be presented at these inputs before and during the rising edge of the latch signal. |
| 9 | $\overline{DP}$ | Dial pulse output.<br>The dial pulse output consists of an N-channel open drain device. During dial pulse break periods this output is switched on (sinking current to GND); it is switched off during all other states. Dialing rate is 9.71 PPS and post-digit pause is 823 ms. (The output of this pin during test mode is discussed below.) |
| 10<br>16 | GND<br>$V_{CC}$ | Negative power supply input.<br>Positive power supply input (operating range 2.5 to 5.5 volts). |
| 11<br>12 | OSC0<br>OSC1 | Oscillator output.<br>Oscillator input.<br>The IN91531 contains an oscillator circuit with the necessary parasitic capacitance and feedback resistor on chip, making it necessary to connect only a standard 3.58 MHz TV crystal across the OSC1 and OSC0 terminals to implement the oscillator function. An external clock input can be applied to the OSC1 pin directly. The oscillator is enabled when the $\overline{CE}$ input is low. |
| 13 | $\overline{CE}$ | Chip enable input.<br>This input controls the onset of oscillation and serves as the master reset for this device. |
| 14 | ASK | Acknowledge output.<br>This pin provides an acknowledge signal to the microcomputer. This output is high when the device is ready to dial out the next digit; it falls low immediately after the rising edge of the latch signal. |
| 15 | TONE | DTMF signal output.<br>This pin consists of an NPN transistor output, with the collector connected to $V_{CC}$. This pin is also connected to the emitter output. The internally generated DTMF signal is delivered to the base of the NPN transistor and is amplified as the transistor connected in common collector. DTMF signaling output time is 70 ms and the interdigit interval is 70 ms. Typical output impedance of the DTMF signal is 1.25 kΩ, and the $h_{FE}$ of the NPN transistor is at least 30 at $I_C$ = 3 mA. |

## FUNCTIONAL DESCRIPTION

### Input Data vs. Output Signal

Parallel binary on D0 - D3 pins are input from microcomputer. Output signal vs. input data is shown in Table 1:

| D3 | D2 | D1 | D0 | DTMF Signaling | PULSE Signal (O/P Pulse No.) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 10 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 | 2 |
| 0 | 0 | 1 | 1 | 3 | 3 |
| 0 | 1 | 0 | 0 | 4 | 4 |
| 0 | 1 | 0 | 1 | 5 | 5 |
| 0 | 1 | 1 | 0 | 6 | 6 |
| 0 | 1 | 1 | 1 | 7 | 7 |
| 1 | 0 | 0 | 0 | 8 | 8 |
| 1 | 0 | 0 | 1 | 9 | 9 |
| 1 | 0 | 1 | 0 | * | 10 |
| 1 | 0 | 1 | 1 | # | 11 |
| 1 | 1 | 0 | 0 | A | 12 |
| 1 | 1 | 0 | 1 | B | 13 |
| 1 | 1 | 1 | 0 | C | 14 |
| 1 | 1 | 1 | 1 | D | Forbidden input |

**Table 1.**

### Input Data vs. Output Signal in Test Mode

The IN91531 provides a high speed pulse/tone output for testing consideration. If the M/B input changes state after the IN91531 is enabled, the test mode is initiated and the device will remain in test mode unless disabled. Table 2 shows input data vs. output signal in pulse/tone test mode.

| D3, D2, D1, D0 | Tone O/P Frequencies and Test Mode | | | | Quantity of Pulses (Pulse O/P Frequencies and Test Mode, Frequency 480 Hz) |
|---|---|---|---|---|---|
| Input In Hex Code | Tone Pin O/P | Unit | $\overline{DP}$ Pin O/P | Unit | $\overline{DP}$ Pin O/P |
| 0 | 948.0 | Hz | 1,331.7 x 8 | Hz | 10 |
| 1 | 699.1 | Hz | 1,215.9 x 8 | Hz | 1 |
| 2 | 1,331.7 | Hz | 699.1 x 8 | Hz | 2 |
| 3 | 1,417.9 | Hz | 699.1 x 8 | Hz | 3 |
| 4 | 1,215.9 | Hz | 766.2 x 8 | Hz | 4 |
| 5 | 1,331.7 | Hz | 766.2 x 8 | Hz | 5 |
| 6 | 766.2 | Hz | 1,471.9 x 8 | Hz | 6 |
| 7 | 847.4 | Hz | 1,215.9 x 8 | Hz | 7 |
| 8 | 1,331.7 | Hz | 847.4 x 8 | Hz | 8 |

**Input Data vs. Output Signal in Test Mode** (Continued)

| D3, D2, D1, D0 | Tone O/P Frequencies and Test Mode | | | | Quantity of Pulses (Pulse O/P Frequencies and Test Mode, Frequency 480 Hz) |
|---|---|---|---|---|---|
| Input In Hex Code | Tone Oin O/P | Unit | $\overline{DP}$ Pin O/P | Unit | $\overline{DP}$ Pin O/P |
| 9 | 1,471.9 | Hz | 847.4 x 8 | Hz | 9 |
| A | 1,215.9 | Hz | 948.0 x 8 | Hz | 10 |
| B | 1,471.9 | Hz | 948.0 x 8 | Hz | 11 |
| C | 1,645.0 | Hz | 699.1 x 8 | Hz | 12 |
| D | 1.645.0 | Hz | 766.2 x 8 | Hz | 13 |
| E | 1.645.0 | Hz | 847.4 x 8 | Hz | 14 |
| F | 1.645.0 | Hz | 948.0 x 8 | Hz | 0 |

Note: Tone Pin O/P in sine wave, $\overline{DP}$ Pin O/P in square ware. The normal timing is reduced to 1/8 at tone test mode and 1/48 at pulse test mode.

**Table 2.** (continued)

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | -0.3 to +6.0 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | -0.3 to $V_{CC}$ +0.3 | V |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND) | -0.3 to $V_{CC}$ +0.3 | V |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP ** | 600 | mW |
| Tstg | Storage Temperature | -55 to +125 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
** Derating: -10 $^{mW}/_{°C}$ from 65°C to 70°C.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 2.5 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature | -10 | +70 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND≤($V_{IN}$ or $V_{OUT}$)≤$V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND, $T_A$ = -10 to +70°C)

| Symbol | Parameter | Test Conditions | Guaranteed Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IH}$ | High-Level Input Voltage | | 0.8 | 1 | V |
| $V_{IL}$ | Low-Level Input Voltage | | 0 | 0.2 | V |
| $I_{IN}$ | Maximum Input Leakage Current | | | ±1.0 | µA |
| $I_{OL1}$ | Minimum Output Sink Current, $\overline{DP}$ | $V_{CC}$ =2.5 V, $V_{OL}$ = 0.4V | 1 | | mA |
| $I_{OL2}$ | Minimum Output Sink Current, $\overline{DP}$ | $V_{CC}$ =5.0 V, $V_{OL}$ = 0.4V | 3 | | mA |
| $I_{CC}$ | Maximum Supply Current Standby | $\overline{CE}$=$V_{CC}$ All outputs unloaded | | 8 | µA |
| $I_{CCP}$ | Maximum Supply Current Pulse | $\overline{CE}$=GND All outputs unloaded $V_{CC}$ = 3.5 V $F_{OSC}$ = 3.58 MHz | | 1 | mA |
| $I_{CCT}$ | Maximum Supply Current Tone | CE=GND All outputs unloaded $V_{CC}$ = 3.5 V $F_{OSC}$ = 3.58 MHz | | 1 | mA |
| $I_{OHACK}$ | Minimum Output Current, ACK Source | $V_{CC}$ = 5.0 V, $V_{OH}$ = 2.4 V | 1.6 | | mA |
| $I_{OLACK}$ | Minimum Output Current, ACK Sink | $V_{CC}$ = 5.0 V, $V_{OL}$ = 0.4 V | 4.0 | | mA |
| $V_{OR}$ | Single Row Tone Output Amplitude | $V_{CC}$ = 2.5 V, $R_L$ = 2.2 kΩ | 500 | | mVp-p |
| | | $V_{CC}$ = 5.5 V, $R_L$ = 2.2 kΩ | | 1500 | |
| $V_{OC}$ | Single Column Tone Output Amplitude | $V_{CC}$ = 2.5 V, $R_L$ = 2.2 kΩ | 500 | | mVp-p |
| | | $V_{CC}$ = 5.5 V, $R_L$ = 2.2 kΩ | | 1600 | |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 2.5 to 5.5 V, $T_A$ = -10 to +70°C)

| Parameter | Symbol | Condition | Guaranteed Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Make/break Ratio, (Figure 1) | M/B | M/B = $V_{CC}$ | | 1/2 | | |
| | | M/B = GND | | 2/3 | | |
| Make Time, (Figure 1) | $T_M$ 0.2$V_{CC}$ | M/B = 1/2 | 31.6 | | 3.5 | ms |
| | $T_M$ 0.8$V_{CC}$ | M/B = 2/3 | 38 | | 4.2 | |
| Break Time, (Figure 1) | $T_B$ 0.2$V_{CC}$ | M/B = 1/2 | 63.3 | | 69.9 | ms |
| | $T_B$ 0.8$V_{CC}$ | M/B = 2/3 | 57 | | 63 | |
| Inter-Digit Pause Time, (Figure 1) | $T_{IDP}$ 0.2$V_{CC}$ | M/B = 1/2 | 750 | | 829 | ms |
| | $T_{IDP}$ 0.8$V_{CC}$ | M/B = 2/3 | 725 | | 801 | |
| Predigit Pause, (Figure 1) | $T_{PDP}$ 0.2$V_{CC}$ | M/B = 1/2 | 33.2 | | 36.8 | ms |
| | $T_{PDP}$ 0.8$V_{CC}$ | M/B = 2/3 | 20 | | 22 | |
| Minimum Tone Duration, (Figure 1) | $T_{MFD}$ | | 66.5 | | 73.5 | ms |
| Minimum Tone Inter-digit Pause, (Figure 1) | $T_{TIDP}$ | | 66.5 | | 73.5 | ms |
| Tone Output Pre-digit Pause, (Figure 1) | $T_{TPDP}$ | | 0 | | 0.5 | ms |
| Oscillator Set-up Time, (Figure 1) | $T_{START}$ | | 4.75 | | 5.25 | ms |

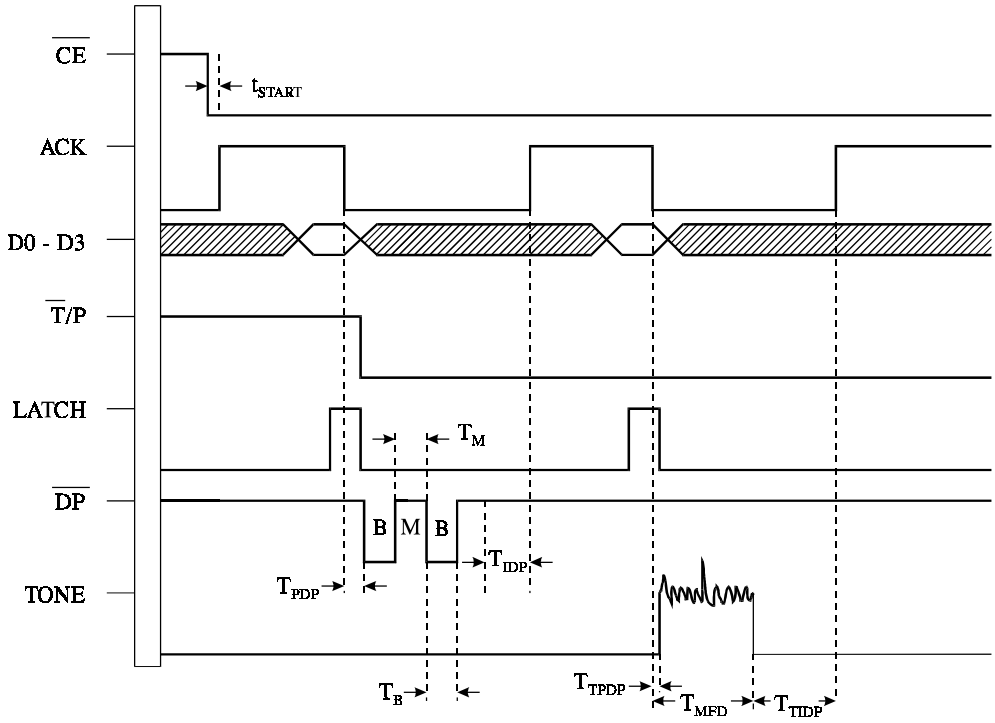



**Figure 1. Switching diagram**

## EXPANDED LOGIC DIAGRAM