PRELIMINARY

8XC196KB
ADVANCED 16-BIT CHMOS MICROCONTROLLER
ROMless OR ROM

Automotive

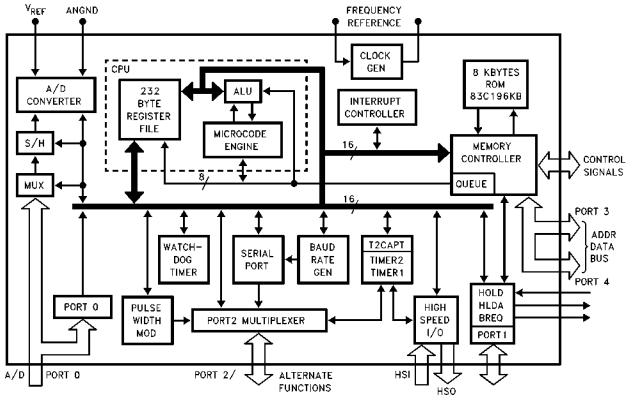
- **−40°C to +125°C Ambient**
- **232 Bytes of On-Chip Register RAM**
- **8 Kbytes of On-Chip ROM (Optional)**
- **High-Performance CHMOS Process**
- **Register-to-Register Architecture**
- **10-Bit A/D Converter with S/H**
- **Five 8-Bit I/O Ports**
- **28 Interrupt Sources**
- **Pulse Width Modulated Output**
- **Powerdown and Idle Modes**
- **High Speed I/O Subsystem**
- **Dynamically Configurable 8/16-Bit Buswidth**
- **Full Duplex Serial Port**
- **Dedicated Baud Rate Generator**
- **1.725 μs 16 x 16 Multiply**
- **3 μs 32/16 Divide**
- **16-Bit Watchdog Timer**
- **16-Bit Timer**
- **16-Bit Up/Down Counter w/Capture**
- **Four 16-Bit Software Timers**
- **HOLD/HOLDA Bus Protocol**

The 8XC196KB 16-bit microcontroller comes with 8 Kbytes of on-chip mask programmable ROM or in ROM-less versions. All devices are high performance members of the 8096 microcontroller family. The 8XC196KB is pin-to-pin compatible and uses a true superset of the 8096 instructions. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

Bit, byte, word and some 32-bit operations are available on the 8XC196KB. With a 16 MHz oscillator, a 16-bit addition takes 0.495 μs, and the instruction times average 0.375 μs to 1.125 μs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. 4 + 2 high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the 16-bit timer or a 16-bit up/down counter.

Also provided on-chip are an 8 channel, 10-bit A/D converter with Sample and Hold, a serial port with synchronous/asynchronous modes and on-chip baud rate generator, a 16-bit watchdog timer, pulse width modulated output with prescaler and an on-chip clock failure detect circuitry.



270679–1

Figure 1. 8XC196KB Block Diagram

February 1995 **Order Number: 270679-005**

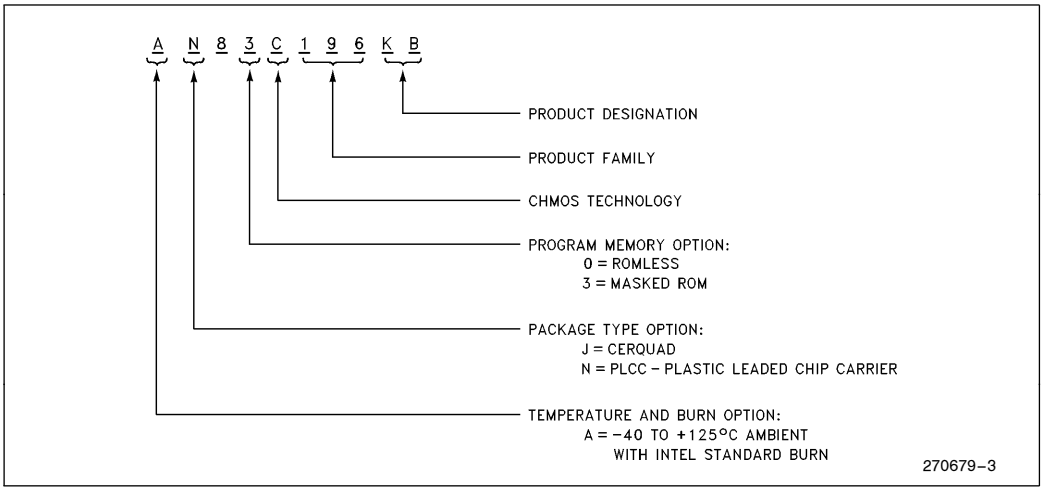


Figure 2. The 8XC196KB Family Nomenclature

ARCHITECTURE

The 8XC196KB is a member of the 8096 family, as such has the same architecture and uses the same instruction set as the 8096. Many new features have been added on the 8CX196KB including:

CPU FEATURES

Divide by 2 instead of divide by 3 clock for a 1.5× performance improvement

Faster instructions, especially indexed/indirect data operations

1.725 μs 16 x 16 multiply with 16 MHz clock (is 6.25 μs on the 8096)

Faster interrupt response (almost twice as fast)

Powerdown and Idle Modes

6 new instructions

8 new interrupt vectors/6 new interrupt sources

PERIPHERAL FEATURES

SFR window switching allows read-only SFRs to be written and vice-versa

Timer 2 can count up and down by external selection

Timer 2 has an independent capture register on rising edges of (P2.7)

HSO line events are stored in a register

HSO has CAM lock and CAM clear commands

New baud rate values are needed for serial port, which enables higher speeds in all modes.

Double buffered serial port transmit register (before, only receive was double buffered)

Serial port receive overrun and framing error detection

PWM has a divide by 2 prescaler

HOLD/HLDA bus protocol

THERMAL CHARACTERISTICS

	PLCC
θ_{JA}	35°C/W
θ_{JC}	12°C/W
Max Case Temperature	135°C

NEW INSTRUCTIONS

PUSHA PUSHes the PSW, IMASK, IMASK1 and WSR (used instead of PUSHF when using the new interrupts and registers)

POPA POPs the PSW, IMASK, IMASK1 and WSR (used instead of POPF when using the new interrupts and registers)

IDLPD Sets the device into Idle or Powerdown Mode. The instruction has the following format: IDLPD #key (where key = 1 for Idle and key = 2 for Powerdown. Illegal keys are processed, but no action is taken.

CMPL Compare 2 long direct values. Only the direct addressing mode is supported for this instruction and the format follows the CMP format.

BMOV Block move using 2 auto-incrementing pointers and a counter. The instruction has the following format: BMOV IPTR.wCNT. The IPTR is a long word, with the low word being the address of the source and the upper word being the address of the destination. wCNT is the number of words to be transferred.

DJNZW* Decrement Jump Not Zero using a word counter. The instruction format follows the DJNZ instruction.

*See the Functional Deviations section for details.

SFR OPERATION

All of the registers that were present on the 8096 work the same way as they did, except that the baud rate value will be different on the 8XC196KB. The new registers shown in the memory map control new functions. The most important register is the Window Select Register (WSR) which allows the reading of the formerly write-only registers, and vice-versa.

PACKAGING

The 8XC196KB is available in 68-pin plastic leaded chip carrier (PLCC) and 68-pin CERQUAD packages. Contact your local sales office to determine the exact ordering code for the part desired.

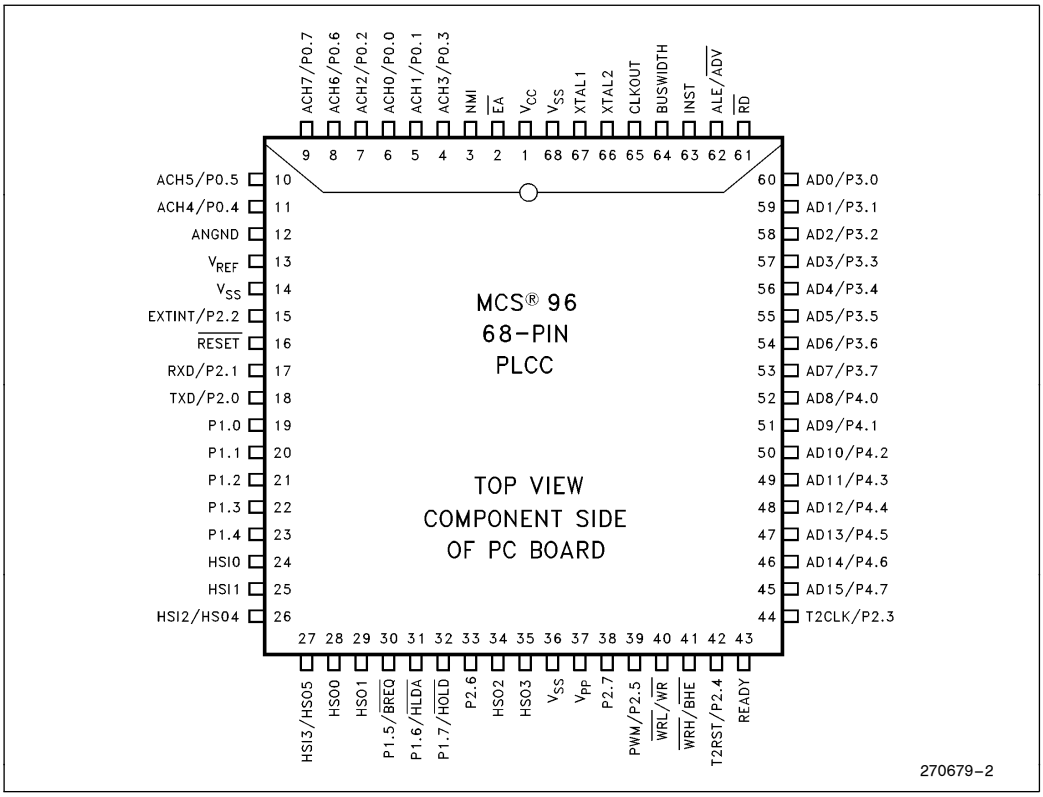


Figure 3. 68-Pin PLCC Package

PLCC	Description
9	ACH7/PO.7/PMD3
8	ACH6/PO.6/PMD2
7	ACH2/PO.2
6	ACH0/PO.0
5	ACH1/PO.1
4	ACH3/PO.3
3	NMI
2	$\overline{EA}$
1	V_{CC}
68	V_{SS}
67	XTAL1
66	XTAL2
65	CLKOUT
64	BUSWIDTH
63	INST
62	ALE/$\overline{ADV}$
61	$\overline{RD}$
60	AD0/P3.0
59	AD1/P3.1
58	AD2/P3.2
57	AD3/P3.3
56	AD4/P3.4
55	AD5/P3.5
54	AD6/P3.6
53	AD7/P3.7
52	AD8/P4.0
51	AD9/P4.1
50	AD10/P4.2
49	AD11/P4.3
48	AD12/P4.4
47	AD13/P4.5
46	AD14/P4.6
45	AD15/P4.7
44	T2CLK/P2.3

PLCC	Description
43	READY
42	T2RST/P2.4/$\overline{AINC}$
41	$\overline{BHE}$/$\overline{WRH}$
40	$\overline{WR}$/$\overline{WRL}$
39	PWM/P2.5
38	P2.7/T2CAPTURE/$\overline{PACT}$
37	V_{PP}
36	V_{SS}
35	HSO.3
34	HSO.2
33	P2.6
32	P1.7/$\overline{HOLD}$
31	P1.6/$\overline{HLDA}$
30	P1.5/$\overline{BREQ}$
29	HSO.1
28	HSO.0
27	HSO.5/HSI.3/SID3
26	HSO.4/HSI.2/SID2
25	HSI.1/SID1
24	HSI.0/SID0
23	P1.4
22	P1.3
21	P1.2
20	P1.1
19	P1.0
18	TXD/P2.0/PVER
17	RXD/P2.1/$\overline{PALE}$
16	$\overline{RESET}$
15	EXTINT/P2.2/$\overline{PROG}$
14	V_{SS}
13	V_{REF}
12	ANGND
11	ACH4/P0.4/PMD0
10	ACH4/P0.5/PMD1

Figure 4. PLCC Functional Pinouts

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main Supply Voltage (+5V)
V_{SS}	Digital Circuit Ground (0V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D Converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference Ground for the A/D Converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming Voltage for the EPROM Parts. It should be +12.75V for programming. This pin was V_{BB} on 8X9X-90 parts. It is also the timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, V_{PP} may be tied to V_{CC}.
XTAL1	Input of the Oscillator Inverter and the Internal Clock Generator
XTAL2	Output of the Oscillator Inverter
CLKOUT	Output of the Internal Clock Generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset Input to the Chip. Input low for at least 4 state times will reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence in which the PSW is cleared, a byte is read from 2018H loading the CCB, and a jump to location 2080H is executed. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
BUSWIDTH	Input for Bus Width Selection. If CCR bit 1 is a one, this pin selects the buswidth for the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. This pin is the $\overline{\text{TEST}}$ pin on the 8X9X-90 parts. Systems with $\overline{\text{TEST}}$ tied to V_{CC} need NOT change.
NMI	A positive transition causes an interrupt vector through external memory location 203EH.
INST	Output High during an External Memory Read. Indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches, during internal EPROM/ROM fetches INST is held low.
$\overline{\text{EA}}$	Input for Memory Select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip EPROM/ROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{\text{EA}}$ = +12.75V causes execution to begin in the Programming Mode. $\overline{\text{EA}}$ has an internal pulldown, so it defaults to execute from external memory, unless otherwise driven. $\overline{\text{EA}}$ is latched at reset.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid Output, as Selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive (high) at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is active only during external memory accesses.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
$\overline{RD}$	Read Signal Output to External Memory. $\overline{RD}$ is active only during external memory reads.
$\overline{WR}$/$\overline{WRL}$	Write and Write Low Output to External Memory, as Selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is active during external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Byte High Enable or Write High Output as Selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects that bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{BHE}$ = 1), to the high byte only (A0 = 1, $\overline{BHE}$ = 0) or both bytes (A0 = 0, $\overline{BHE}$ = 0). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory write cycles.
READY	Ready Input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The number of wait states inserted into the bus cycle is controlled by the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2, HSI.3. Two of which are shared with the HSO Unit (HSI.2 and HSI.3). The HSI pins are also used as the SID in Slave Programming Mode.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available (HSO.0 through HSO.5). HSO.4 and HSO.5 are shared with HSI.
PORT 0	8-Bit High Impedance Input-Only Port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts to select the Programming Mode.
PORT 1	8-Bit Quasi-Bidirectional I/O Port.
PORT 2	8-Bit Multi-Functional Port. All of its pins are shared with other functions.
PORT 3 and 4	8-Bit Bidirectional I/O Ports with Open Drain Outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{HOLD}$	Bus Hold Input Requesting Control of the Bus. Enabled by Setting WSR.7
$\overline{HLDA}$	Bus Hold Acknowledge Output Indicating Release of the Bus. Enabled by setting WSR.7.
$\overline{BREQ}$	Bus Request Output. Activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.

ELECTRICAL CHARACTERISTICS

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings*

Storage Temperature . . . . . −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND . . . . . −0.5V to +13.0V

Voltage on Any Pin to V_{SS} or ANGND . . . . . −0.5V to +7.0V

This includes V_{PP} on ROM and CPU devices.

Power Dissipation 1.5W

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature under Bias	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	3.5	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Under Listed Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current (−40°C to +125°C Ambient)		50	70	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current		5		μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Reference Supply Current		2	5	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current		10	35	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
V_{IL}	Input Low Voltage	−0.5V		+0.8	V	
V_{IH}	Input High Voltage(1)	0.2 V_{CC}+1.1		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input on High Voltage on RESET	2.6		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7.0 mA
V_{OH1}	Output High Voltage (Quasi-Bidirectional Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −15 μA I_{OH} = − 30 μA I_{OH} = −60 μA

DC CHARACTERISTICS (Under Listed Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Leakage Current (Std. Inputs)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−800	μA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)			−50	μA	$V_{IN} = 0.45V$
I_{IL1}	Logical 0 Input Current in Reset (ALE, $\overline{RD}$, INST)			−9	mA	$V_{IN} = 0.45V$
I_{IL2}	Logical 0 Input Current in Reset (WR, P2.0, BHE)			−700	μA	$V_{IN} = 0.45V$
HYST	Hysteresis on RESET Pin	250			mV	
R_{RST}	Reset Pullup Resistor	6K		50	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	$F_{TEST} = 1.0$ MHz

NOTES: (Notes apply to all specifications)
1. All pins except RESET and XTAL1. QBC (Quasi-bidirectional) pins include Port 1, P2.6, P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Port 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open drain outputs.
3. Standard Inputs include HSI pins, CDE, $\overline{EA}$, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below $V_{CC} - 0.7V$:
   I_{OL} on Output pins: 10 mA
   I_{OL} on QBD pins: self limiting
   I_{OL} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH}: is Self Limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST, CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

7. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.

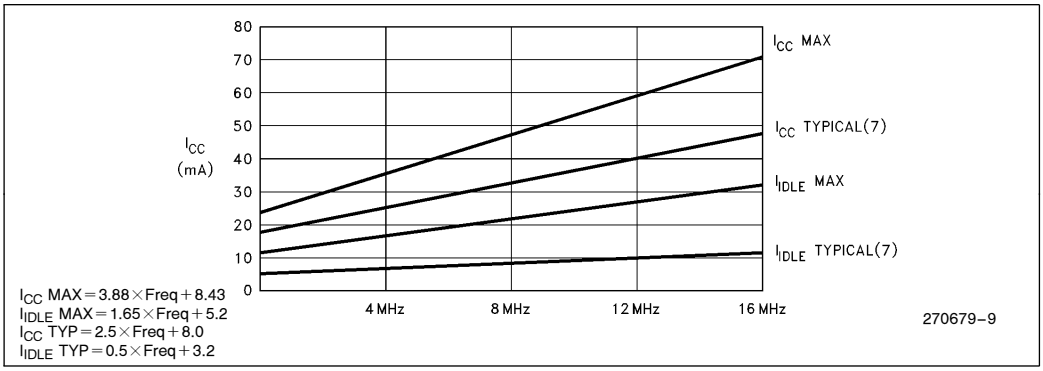


Figure 5. I_{CC} vs Frequency

AC CHARACTERISTICS Over Specified Operating Conditions

Test Conditions: Capacitance load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 8XC196KB

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} − 75	ns
T_{LLYV}	ALE Low to READY Setup		T_{OSC} − 60	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns(1)
T_{LLYX}	READY Hold after ALE Low	T_{OSC} − 15	2 T_{OSC} − 40	ns(1)
T_{AVGV}	Address Valid to Buswidth Setup		2 T_{OSC} − 75	ns
T_{LLGV}	ALE Low to Buswidth Setup		T_{OSC} − 60	ns
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 55	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 23	ns
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 50	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC} − 20	ns
T_{RXDX}	Data hold after $\overline{RD}$ Inactive	0		ns
F_{XTAL}	Oscillator Frequency	3.5	16	MHz
T_{OSC}	Oscillator Period ($1/f_{XTAL}$)	62.5	286	ns
T_{XHCH}	XTAL1 High to CLKOUT High or LOW(1)	20	110	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 10	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	10	ns
T_{LLCH}	ALE/$\overline{ADV}$ Falling Edge to CLKOUT Rising	−15	15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns
T_{LHLL}	ALE/$\overline{ADV}$ High Period	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Setup to ALE/$\overline{ADV}$ Falling Edge	T_{OSC} − 30		ns
T_{LLAX}	Address Hold after ALE/$\overline{ADV}$ Falling Edge	T_{OSC} − 40		ns
T_{LLRL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 35		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	25	ns
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 10	T_{OSC} + 25	ns
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge(3)	T_{OSC}	T_{OSC} + 25	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	15	ns
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 15	T_{OSC} + 5	ns

AC CHARACTERISTICS Over Specified Operating Conditions (Continued)

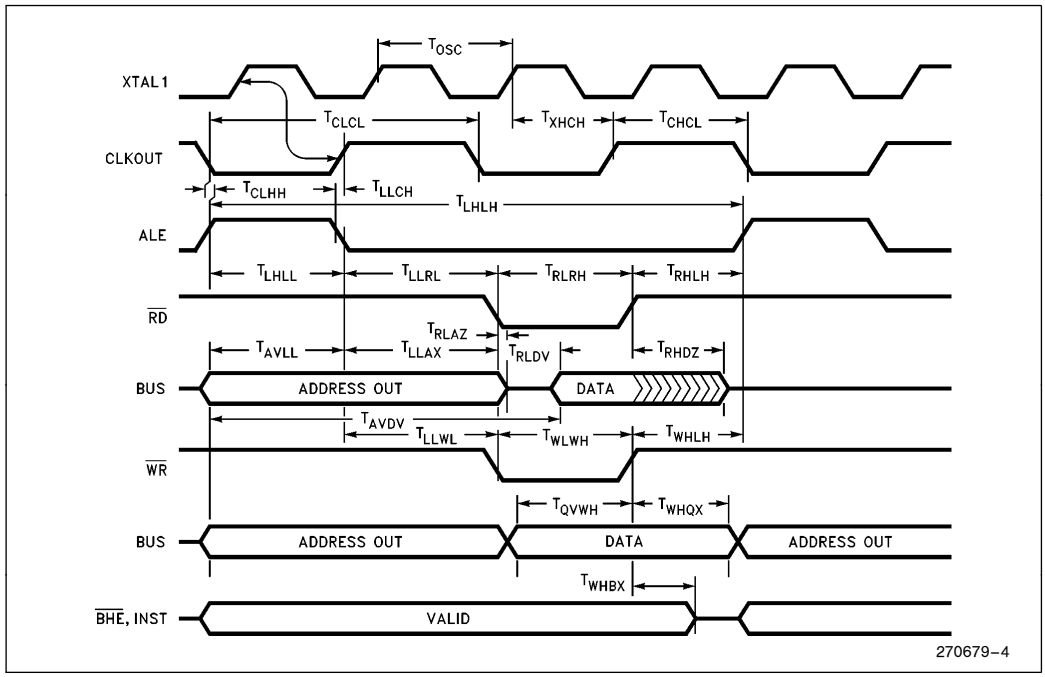
Test Conditions: Capacitance load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 8XC196KB

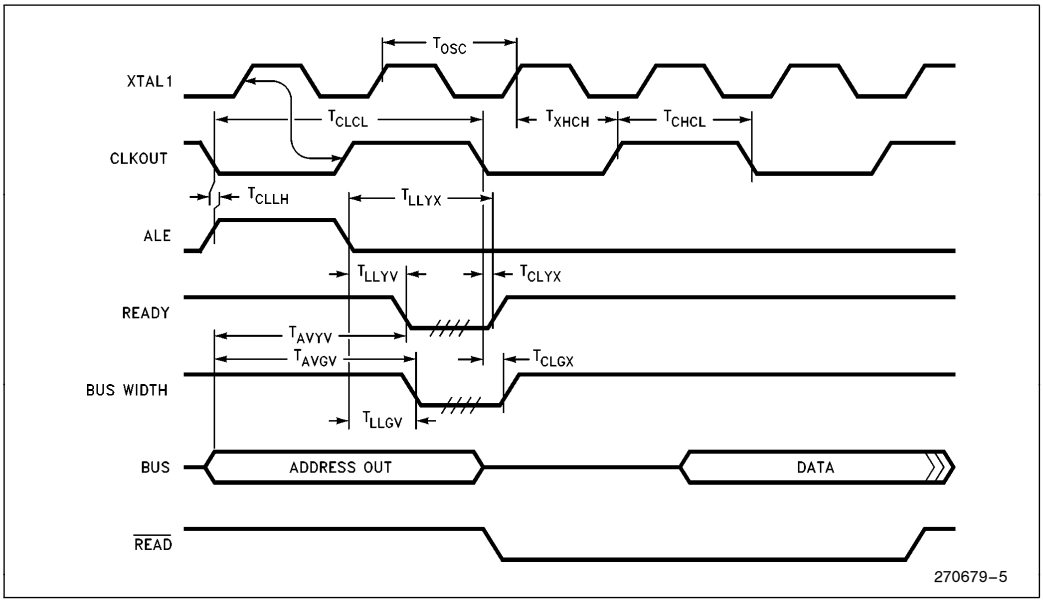
Symbol	Parameter	Min	Max	Units
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge(3)	T_{OSC} − 20	T_{OSC} +10	ns
T_{WHBX}	$\overline{BHE}$, INST, HOLD after $\overline{WR}$, $\overline{RD}$ Rising Edge	T_{OSC} − 15		ns
T_{WHAX}	AD8–15 Hold after $\overline{WR}$/RD Rising Edge	T_{OSC} − 30		ns
T_{RHBX}	$\overline{BHE}$, INST HOLD after $\overline{RD}$ Rising	T_{OSC} − 10		ns
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	T_{OSC} − 25		ns

NOTES:
1. Typical specification, not guaranteed.
2. Assuming back-to-back bus cycles.
T_{OSC} = 62.5 ns at 16 MHz; T_{OSC} = 100 ns at 10 MHz; T_{OSC} = 125 ns at 8 MHz.

System Bus Timing



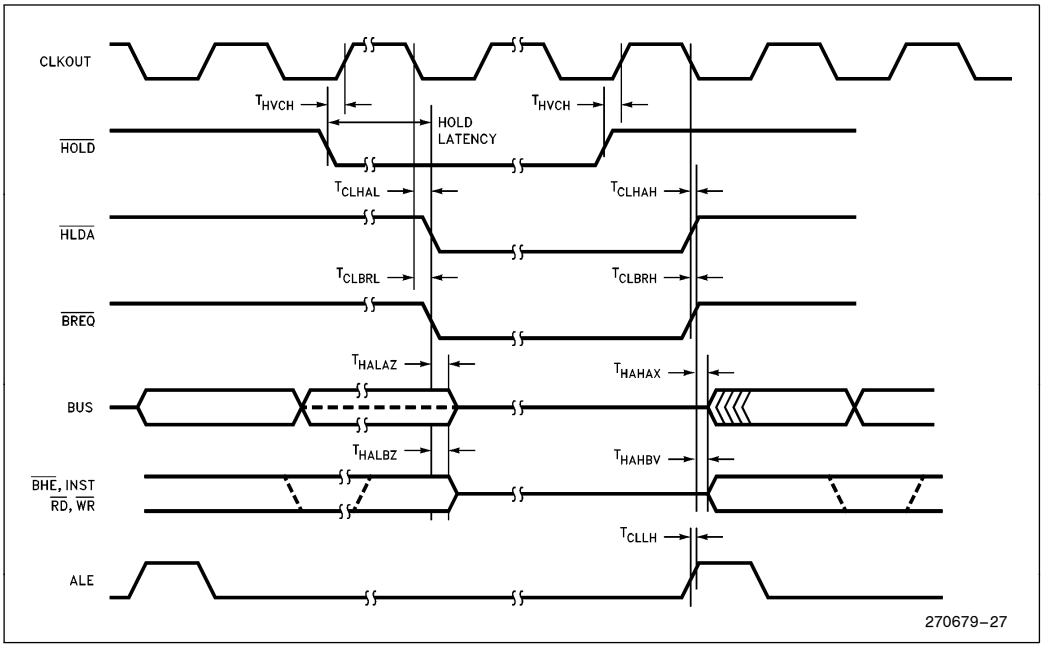
Ready/Buswidth Timing



HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup 80C196KB 83C196KB	 75 85		 ns	1
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	15	ns	
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	15	ns	
T_{HALAZ}	HLDA Low to Address Float 80C196KB 83C196KB		 15 20	 ns	
T_{HALBZ}	HLDA Low to BHE, INST, RD, WR Float			ns	
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	
T_{HAHAX}	HLDA High to Address No Longer Float	−5		ns	
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	−20		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

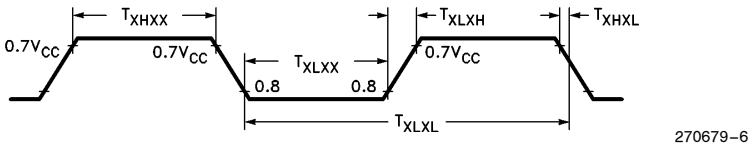
NOTE:
1. To guarantee recognition at next clock.



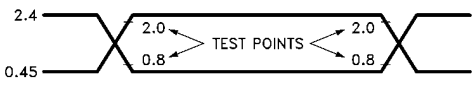
External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	3.5	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	286	ns
T_{XHXX}	High Time	T_{OSC} − 51		ns
T_{XLXX}	Low Time	T_{OSC} − 51		ns
T_{XLXH}	Rise Time		T_{OSC} − 73	ns
T_{XHXL}	Fall Time		T_{OSC} − 73	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



AC TESTING INPUT, OUTPUT WAVEFORMS



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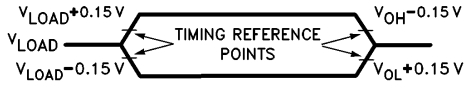
AC Testing inputs are driven at 2.4V for logic ''1'' and 0.45V for a logic ''0''. Timing measurements are made at 2.0V for a logic ''1'' and 0.8V for logic ''0''.

FLOAT WAVEFORMS



270679–8

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by ''t'' for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:
H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:
A— Address
B— $\overline{BHE}$
C— CLKOUT
D— Data
G—Buswidth
L— ALE/$\overline{ADV}$
R— $\overline{RD}$
W— $\overline{WR}/\overline{WRH}/\overline{WRI}$
X— XTAL1
Y— Ready

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: $T_C = -40°C$ to $+125°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0.0V$; Load Capacitance = 80 pF

Symbol	Parameter	Min	Max	Unit
T_{XLXL}	Serial Port Clock Period(9)	6 T_{OSC}/4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge(9)	4 $T_{OSC}-50$/2 $T_{OSC}-50$	4 $T_{OSC}+50$/2 $T_{OSC}-50$	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 $T_{OSC}-50$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 $T_{OSC}-50$		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 $T_{OSC}+50$	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	$T_{OSC}+50$		ns
T_{XHDX}(8)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(8)	Last Clock Rising to Output Float		T_{OSC}	ns

NOTES:
8. Parameter not tested.
9. Baud Rate Register ≥ 8002H/Baud Rate Register = 8001H.

A to D CHARACTERISTICS

There are two modes of A/D operation: with and without clock prescaler. The modes are shown in the table below. In mode 2, with the clock prescaler disabled, the maximum XTAL1 frequency is 8.0 MHz. Accuracy will degrade at higher frequencies in this mode. The frequency divider option is provided to obtain higher accuracy outside of the currently specified operating conditions.

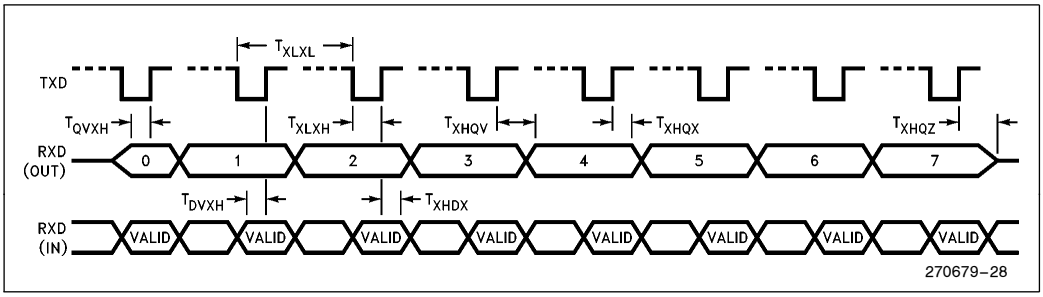
The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resister ladder and the digital section of the converter.

A/D Converter Specifications

The specifications given below assume adherence to the operating conditions section of this data sheet. Testing is performed in mode 2 with V_{REF} = 5.12V and 8 MHz operating clock frequency.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



Clock Prescaler ON IOC2.4 = 0	Clock Prescaler OFF IOC2.4 = 1
Mode 1— 158 States for Execution 26.33 μs @ 12 MHz	Mode 2— 91 States for Execution 22.75 μs @ 8 MHz (Maximum)

NOTE:
IOC2.3 = 0, The No Sample and Hold feature is not available on the 8XC196KB device.

Parameter	Typical*(1)	Minimum	Maximum	Units**
Resolution		512 9	1024 10	Level Bits
Absolute Error		0	±6	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	−0.25 ±0.5			LSBs
Non-Linearity	1.5 ± 2.5	0	±4	LSBs
Differential Non-Linearity		> −1	+2	LSBs
Channel-to-Channel Matching	±0.1	0	±1	LSBs
Repeatability	±0.25			LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1, 2, 4)
Feedthrough	−60			dB(1, 2)
V_{CC} Power Supply Rejection	−60			dB(1, 2)
Input Resistance		1K	5K	Ω(1)
DC Input Leakage		0	3	μA
Sample Time (Prescaler on/off)	15/8			States (3)
Input Capacitance	3			pF

NOTES:
*These values are expected for most parts at 25°C but are not tested or guaranteed.
**An ''LSB'', as used here, has a value of approximately 5 mV. (See Automotive Handbook, for A/D glossary of terms.
1. These values are not tested in production and are based on theoretical estimates and/or laboratory test.
2. DC to 100 KHz.
3. One state = 125 ns @ 16 MHz; 333 ns @ 6 MHz.
4. Multiplexer Break-Before-Make Guaranteed.

80C196KB FUNCTIONAL DEVIATIONS

The 80C196KB has the following problems.

1. The HSI unit has two errata: one dealing with resolution and the other with first entries into the FIFO.

   The HSI resolution is 9 states instead of 8 states. Events on the same line may be lost if they occur faster than once every 9 state times.

   There is a mismatch between the 9 state time HSI resolution and the 8 state time timer. This causes one time value to be unused every 9 timer counts. Events may receive a time-tag one count later than expected because of this ''skipped'' time value.

   If the first two events into an empty FIFO (not including the Holding Register) occur in the same internal phase, both are recorded with one time-tag. Otherwise, if the second event occurs within 9 states after the first, its time-tag is one count later than the first's. If this is the ''skipped'' time value, the second event's time-tag is 2 counts later than the first's.

   If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register after 8 state times, leaving the FIFO empty again. If the second event occurs after this time, it will act as a new first event into an empty FIFO.

2. If an A/D conversion in progress is aborted by starting a new A/D conversion, results of the second conversion may be inaccurate.

The work-around is to wait for the conversion in progress to finish before starting the second conversion. Polling or an interrupt will detect the conversion completion.

3. If the unsigned divide instruction (word or byte) is in the queue as HOLD or READY is asserted, the result may be incorrect. TechBit (MC1791). (B-step only.)

DIFFERENCES BETWEEN THE 80C196KA AND THE 80C196KB

The 8XC196KB is identical to 8XC196KA except for the following differences.

1. ALE is high after reset on the 80C196KB instead of low as on the 80C196KA.
2. The DJNZW instruction is not guaranteed to work on the 80C196KB. (A-step only.)
3. The $\overline{HOLD}$/$\overline{HLDA}$ bus protocol is available on the 80C196KB.

CONVERTING FROM OTHER 8096BH FAMILY PRODUCTS TO THE 80C196KB

The following list of suggestions for designing an 809XBH system will yield a design that is easily converted to the 80C196KB.

1. Do not base critical timing loops on instruction or peripheral execution times.
2. Use equate statements to set all timing parameters, including the baud rate.
3. Do not base hardware timings on CLKOUT or XTAL1. The timings of the 80C196KB are different than those of the 8X9XBH, but they will function with standard ROM/EPROM/Peripheral type memory systems.
4. Make sure all inputs are tied high or low and not left floating.
5. Indexed and indirect operations relative to the stack pointer (SP) work differently on the 80C196KB than on the 8096BH. On the 8096BH, the address is calculated based on the un-updated version of the stack pointer. The 80C196KB uses the updated version. The offset for POP[SP] and POP nn[SP] instructions may need to be changed by a count of 2.
6. The V_{PD} pin on the 8096BH has changed to a V_{SS} pin on the 80C196KB.

OTHER DESIGN CONSIDERATIONS (KB B-0 to KB C-1)

1. The NMI pin on the KB ROM (C-1) has a weak pulldown. I_{IH1} max is 100 μA. The KB ROM (B-0) did not have a pulldown on NMI. If KB ROM (B-0) designs have NMI tied to V_{CC}, the NMI pin must be tied to V_{SS}. If NMI is tied to V_{SS} or is floating, it is okay.
2. The ALE, RD, and INST pins on the KB ROM (C-1) have stronger pullups during RESET than on the KB ROM (B-0). I_{IL1} is -7 mA on the KB ROM (C-1) compared to -1.2 mA on the KB ROM (B-0). Designs which pull these pins low to enter ONCE mode must have strong enough pulldowns to overcome the pullups.
3. Pin on the PLCC package on the KB ROM (B-0) was the CDE pin. That function did not work so the pin was assigned to V_{SS}. On the KB ROM (C-1) this pin is tied directly to V_{SS} on the device and MUST be tied to V_{SS} externally.
4. Several AC/DC specifications have changed. (See Data Sheet Revision History; review them carefully.)

DATA SHEET REVISION HISTORY

This is the -005 revision of the 8XC196KB data sheet and is valid for devices marked with a ''F'' or ''G'' at the end of the topside tracking number. The following differences exist between the -004 revision and the -005 revision:

1. All performance related data is now quoted at 16 MHz. The maximum clock rate has changed from 12 MHz to 16 MHz.
2. Max power dissipation changes from 0.43W to 1.5W.
3. I_{CC} max has changed from 60 mA to 70 mA.
4. I_{CC} typical has changed from 40 mA to 50 mA.
5. I_{REF} typical has changed from 1 mA to 2 mA.
6. I_{IDLE} has changed from 25 mA to 35 mA.
7. V_{IH2} min has changed from 2.4V to 2.5V.
8. V_{OH1} test condition for $V_{CC} - 0.3V$ has changed from $-7\ \mu A$ to $-15\ \mu A$.
9. I_{TL} has changed from $-650\ \mu A$ to $-800\ \mu A$.
10. I_{IL1} has changed from -1.2 mA to -9 mA.
11. I_{IL1} now only applies to ALE, $\overline{RD}$ and INST.
12. R_{RST} max has changed from 100 KΩ to 50 KΩ.
13. Added spec for RESET pin hysteresis and I_{IL2} for WR, P2.0, and BHE.
14. T_{AVYV} has changed from 2 T_{OSC} − 85 ns to 2 T_{OSC} − 75 ns.
15. T_{LLYV} has changed from T_{OSC} − 72 ns to T_{OSC} − 60 ns.
16. T_{AVGV} has changed from 2 T_{OSC} − 85 ns to 2 T_{OSC} − 75 ns.
17. T_{AVDV} has changed from 3 T_{OSC} − 65 ns to 3 T_{OSC} − 55 ns.
18. F_{XTAL} max has changed from 12 MHz to 16 MHz.
19. T_{OSC} min has changed from 83 ns to 62.5 ns.
20. T_{XHCH} min has changed from 40 ns to 20 ns.
21. T_{CLLH} min/max has changed from −5 ns/15 ns to −10 ns/10 ns.
22. T_{LHLL} min/max has changed from T_{OSC} ±12 ns to T_{OSC} ±10 ns.
23. T_{AVLL} has changed from T_{OSC} − 20 ns to T_{OSC} − 30 ns.
24. T_{LLRL} has changed from T_{OSC} − 40 ns to T_{OSC} − 35 ns.
25. T_{RLCL} min/max has changed from 5 ns/30 ns to 4 ns/25 ns.
26. T_{RLRH} has changed from T_{OSC} − 5 ns to T_{OSC} − 10 ns.
27. T_{RLAZ} has changed from 12 ns to 5 ns.
28. T_{CHWH} min/max has changed from −10 ns/10 ns to −5 ns/15 ns.
29. T_{WLWH} min/max has changed from T_{OSC} − 30 ns to T_{OSC} − 15 ns.
30. T_{WHQX} has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
31. T_{WHLH} min/max has changed from T_{OSC} − 10 ns/T_{OSC} + 15 ns to T_{OSC} − 20 ns/T_{OSC} + 10 ns.
32. T_{WHBX} has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
33. T_{WHAX} has changed from T_{OSC} − 50 ns to T_{OSC} − 30 ns.
34. T_{RHAX} has changed from T_{OSC} − 50 ns to T_{OSC} − 25 ns.
35. Functional deviation number 1 has been removed (DJWZ is now functional).
36. Functional deviation number 3 has been removed (SIO framing flag now works correctly).
37. Functional deviation number 5 has been removed (SIO RI now correctly generated).
38. Functional deviation number 6 has been corrected. The divide during HOLD bug has been fixed.
39. The section ''Other Design Considerations KB B-0 to KB C-1'' has been added.