Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVERS (3-STATE)

IDT54/74FCT623T/AT/CT

FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1µA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 64mA I_{OL})
- Power off disable outputs permit “live insertion”
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

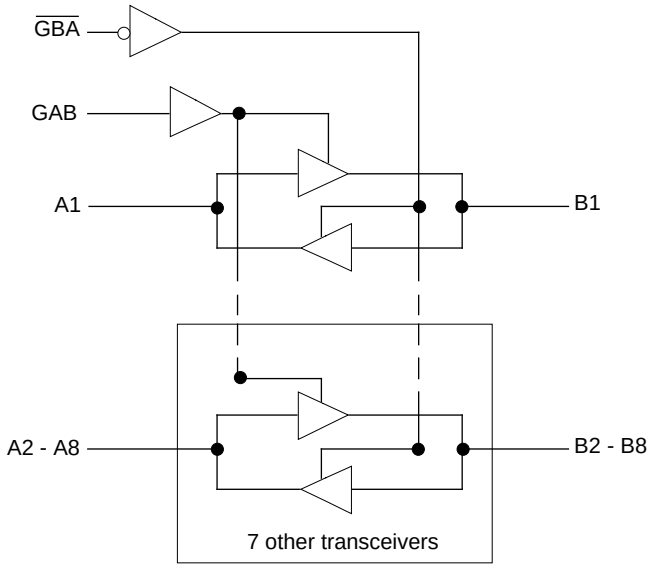
DESCRIPTION

The FCT623T/AT/CT is a non-inverting octal transceiver with 3-state bus-driving outputs in both the send and receive directions. The B bus outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

One important feature of the FCT623T/AT/CT is the Power Down Disable capability. When the GAB and $\overline{GBA}$ inputs are conditioned to put the device in high-Z state, the I/O ports will maintain high impedance during power supply ramps and when V_{CC} = 0V. This is a desirable feature in back-plane applications where it may be necessary to perform “live” insertion and removal of cards for on-line maintenance. It is also a benefit in systems with multiple redundancy where one or more redundant cards may be powered-off.

FUNCTIONAL BLOCK DIAGRAM



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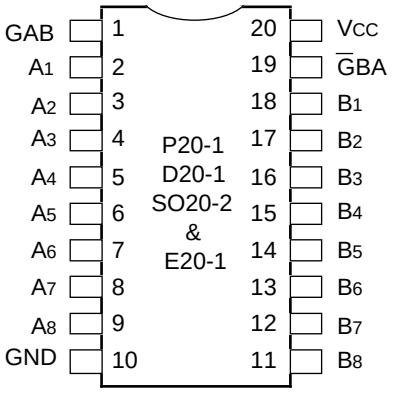
PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW

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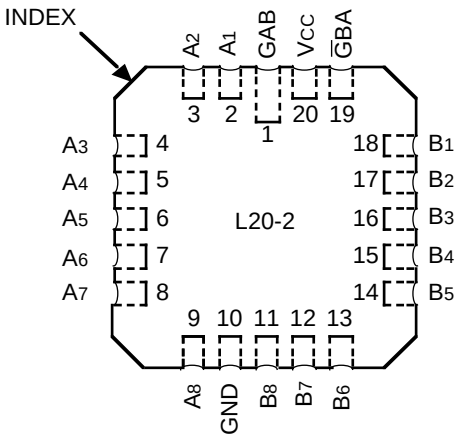

LCC TOP VIEW

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DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{G}$BA, GAB	Enable Inputs
A_1 - A_8	A Bus Inputs or 3-State Outputs
B_1 - B_8	B Bus Inputs or 3-State Outputs

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FUNCTION TABLE(1)

Enable Inputs		
$\overline{G}$BA	GAB	Outputs
L	L	B data to A bus
H	H	A data to B bus
H	L	Z
L	H	B data to A bus A data to B bus

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NOTES:
1. H = HIGH Voltage Level
2. L = LOW Volage Level
3. Z = High-Impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[5]	V_{CC} = Max., V_I = 2.7V		—	—	±1	µA
I_{IL}	Input LOW Current[5]	V_{CC} = Max., V_I = 0.5V		—	—	±1	µA
I_I	Input HIGH Current[5]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage (A and B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage (A Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.[4] I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_{OL}	Output LOW Voltage (B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.[4] I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage[6]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	µA

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.
5. The test limit for this parameter is ±5µA at T_A = –55°C.
6. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{G}BA$ = GAB = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{G}BA$ = GAB = GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	6.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	14.0[5]	

NOTES: 2563 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

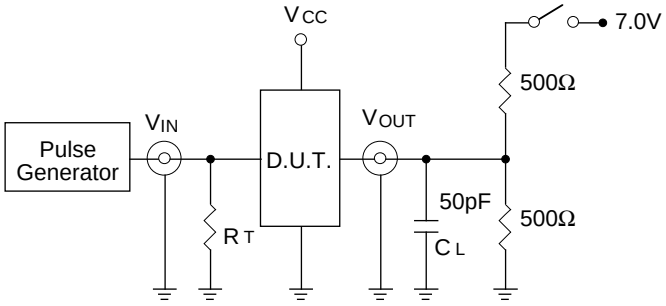
			54/74FCT623T				54/74FCT623AT				54/74FCT623CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay An to Bn	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
t_{PLH} t_{PHL}	Propagation Delay Bn to An		1.5	7.5	1.5	9.5	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{G}BA$ to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}BA$ to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
t_{PZH} t_{PZL}	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

NOTES: 2563 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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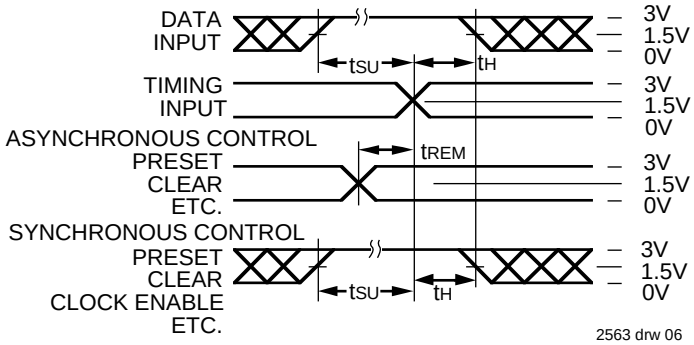
DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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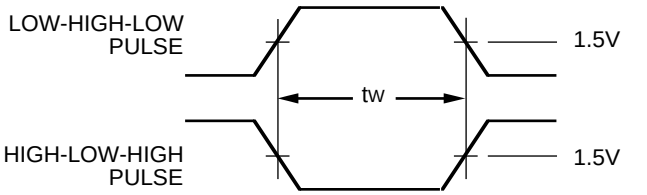
PULSE WIDTH



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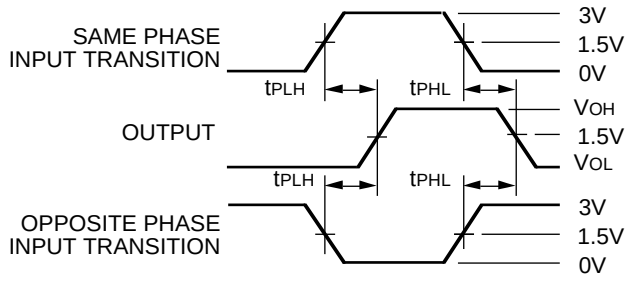
PROPAGATION DELAY



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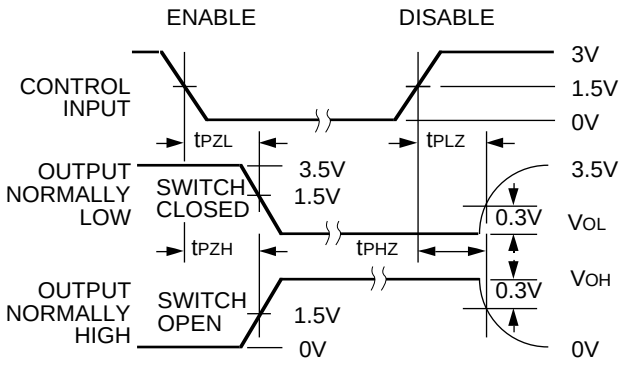
ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION