Integrated Circuit Systems, Inc.

ICS2002

Wavedec™ Digital Audio Codec

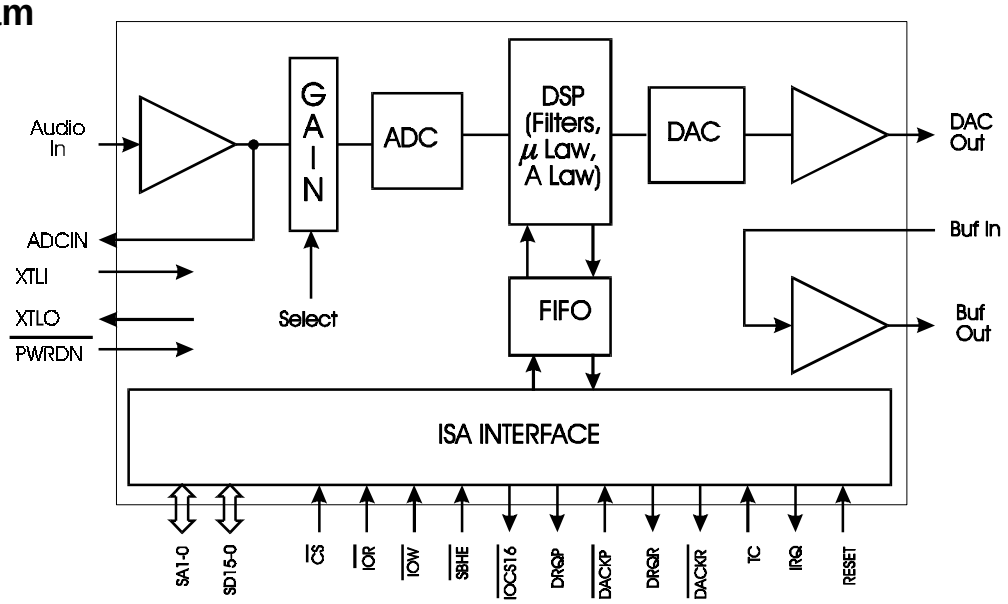
Description

The **ICS2002** is a mixed-signal integrated circuit providing a low-cost recording and playback solution for multimedia audio applications. These applications include document annotation, voice mail, interactive games, multimedia sound record/playback, and Windows™ sound production. The **ICS2002** supports the record and playback of 16-bit audio data, and provides a 8/16-bit parallel interface to the industry standard PC bus.

Features

- Digital audio 8/16-bit record/playback
- Fully programmable sample rates including industry standards:
  - 44.1 kHz
  - 22.050 kHz
  - 11.025 kHz
  - 8.00 kHz
  - 5.513 kHz
- DAC output oversampled to simplify external filtering.
- Four data formats:
  - 16 bit linear
  - 8 bit linear
  - 8 bit u-law
  - 8 bit a-law
- 16 step analog output level control, -1.5dB/step
- 8-bit log scale digital volume control
- Oversampling ADC with input filter.
- Programmable IIR filters for input anti-aliasing and output reconstruction.
- ISA bus interface
- 8/16-bit DMA and I/O transfer modes
- Input/output FIFO buffer
- Power-down mode
- 44-pin PLCC package

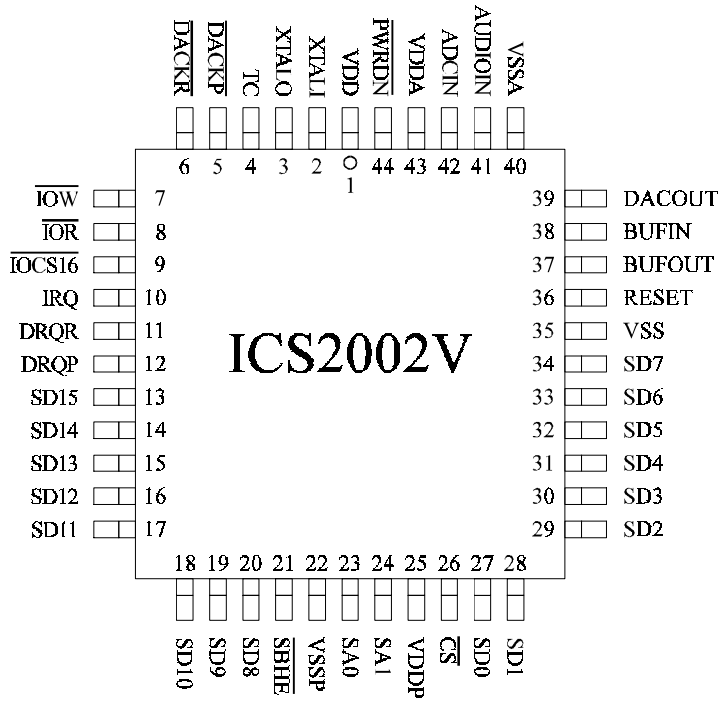
Block Diagram



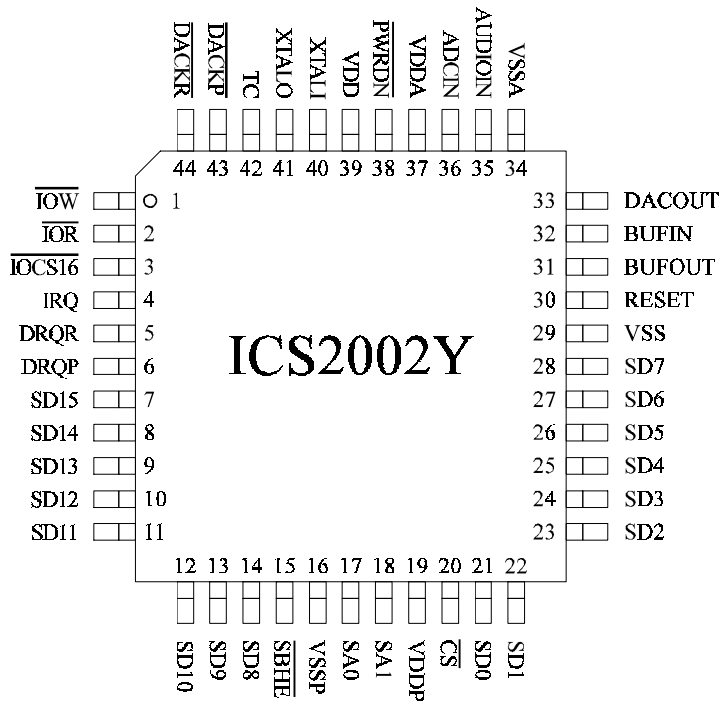
Pin Descriptions

PIN	TYPE	DESCRIPTION
SD15 - SD0	I/O	Data bus
SA1 - SA0	I	Address
$\overline{CS}$	I	Chip select (active low)
$\overline{IOW}$	I	Write strobe (active low)
$\overline{IOR}$	I	Read strobe (active low)
$\overline{SBHE}$	I	System High Byte Enable (active low)
$\overline{IOCS16}$	OC	Indicates that the access register can support 16 bit transfer.
DRQP	O	DMA Request (play channel)
DRQR	O	DMA Request (record channel)
$\overline{DACKP}$	I	DMA Acknowledge (play channel)
$\overline{DACKR}$	I	DMA Acknowledge (record channel)
TC	I	DMA terminal count
IRQ	O	Interrupt request (active high, open drain)
RESET	I	Reset (active high)
XTLI	I	Crystal oscillator
XTLO	O	Crystal oscillator
$\overline{PWRDN}$	I	Power-down (active low)
AUDIOIN	AI	Audio buffer input
ADCIN	AO	Audio buffer output/input to ADC
DACOUT	AO	DAC audio output
BUFIN	AI	Uncommitted audio buffer input
BUFOUT	AO	Uncommitted audio buffer output
VDD	P	Digital +5V supply
VDDA	P	Analog +5V supply
VDDP	P	Digital +5V supply
VSS	P	Digital GND
VSSA	P	Analog GND
VSSP	P	Digital GND

Package Pinout



44-Pin PLCC



44-Pin TQFP

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to 7.0V
Logic Inputs . . . . . -0.5V to V_{DD} + 0.5V
Ambient Operating Temperature. . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = 5.0V ± 10%; GND = 0V; T_A = 0°C to +70°C

DC/STATIC					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Digital Inputs					
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.0		V_{DD} + 0.3	V
Input Leakage Current	I_{LI}			1	µA
Input Capacitance	C_{IN}			7	pF
Digital Outputs					
Output Low Voltage (I_{OL} = 4.0mA)	V_{OL}			0.4	V
Output High Voltage (I_{OH} = 0.4mA)	V_{OH}	2.4			V
Tristate Current	I_{OZ}			10	µA
Output Capacitance				10	pF
Bi-directional Capacitance				10	pF
Analog Inputs					
Audio Input Voltage			0.7		Vrms
Audio Input Impedance		500k			ohm
Buffer Input Impedance		500k			ohm
Audio Outputs					
Audio Output Voltage			0.7		Vrms
DACOUT, BUFOUT Output Impedance				1k	ohm
Digital Supply Current	I_{CC1}			1	mA
Analog Supply Current	I_{DD2}			35	mA
Power-Down Mode				1	mA
Play Only Mode				15	mA
Record Mode				30	mA

Electrical Characteristics

V_{DD} = 5.0V ± 10%; GND =0V; T_A = 0°C to +70°C

AC/DYNAMIC					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Address setup to command	t_{AS}	10			ns
Address hold from command	t_{AH}	10			ns
Command cycle time	t_{CCY}	100			ns
Address valid to /IOCS16 delay	t_{AID}			50	ns
IOCS16 hold from address invalid	t_{IH}	0			ns
Data valid to /IOW	t_{DS}	50			ns
/IOR active to valid data	t_{DAC}			60	ns
Data hold after /IOR	t_{DHR}	0			ns
Data hold after /IOW	t_{DHW}	10			ns
/DACK setup to /IOR	t_{DAR}	30			ns
/DACK setup to /IOW	t_{DAW}	50			ns
/DACK hold from command	t_{DAH}	50			ns
/CS setup to command	t_{CS}	10			ns
/CS hold from command	t_{CH}	10			ns
TC setup to command inactive	t_{TS}	25			ns
TC hold from command	t_{TH}	0			ns

Digital Audio Playback

To play digital audio files, the chip is programmed for the desired sample rate, data type, DMA channel width, and output volume.

For DMA mode playback, DRQ generation is programmable for servicing the FIFO at several levels. This allows optimal performance with a variety of hosts. When TC is received, the chip will optionally generate an interrupt to the host to indicate the need to service the DMA controller.

For I/O Mode playback, data is written to the FIFO until it is full. This is determined by polling the "DIR" bit of the status register. Once the FIFO is full, an interrupt will be generated optionally at one of several selectable points: 1/4, 1/2, or 3/4 full. The host can then burst a predetermined amount of data to the FIFO and wait for the next interrupt.

Digital Audio Recording:
Audio recording operates in a DMA or I/O mode similarly to audio playback with the audio input programmable as a line or microphone level input. Simultaneous record and playback is supported and permits the recorded file to be synchronized to an existing file. The new and existing file can then be mixed digitally for high quality results.

Data Processing:
To simplify the external circuitry associated with the analog input and output signals of the chip, input and output sample rates are oversampled. This allows simple RC filters to be used.

For playback, the output data is oversampled, interpolated, filtered and scaled. Since the DSP is fully programmable, various sample rates and filter shapes can be implemented. The processed data is then output to the DAC. The DAC output passes through an analog volume control (4 bits, 1.5dB steps) before being passed to the analog filter stage.

For recording, the input data is first filtered, removing most of the frequency content above the Nyquist frequency. The resulting data stream is then undersampled to the desired sample rate and fed into the FIFO for transfer to the host.

Power Management:
The $\overline{\text{PWRDN}}$ input can be programmed to act as an immediate hardware power control, or as an interrupt source for a software driven power management routine. The software driven option allows the driver to cleanly shut down to chip, thus preventing unwanted noise. When active, the power-down function disables all analog components including the oscillator, and causes the chip to enter a low power mode.

Miscellaneous Functions:
The chip has a full complement of status and control functions. All significant functions are capable of generating interrupts and/or being polled.

The DMA can be run in single or demand mode (for bursts of data in programmed sizes).

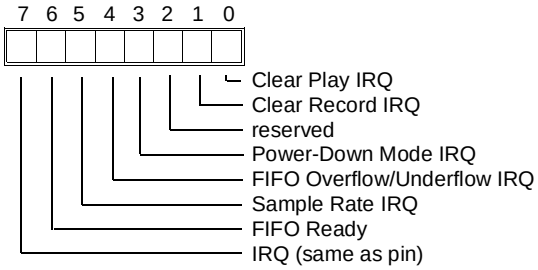
The FIFO has programmable interrupt and DMA request capacities, and also indicates when overflow or underflow conditions occur.

The processor interface is designed for simple connection to the ISA bus. For best noise performance, isolating the data lines from the ISA bus is recommended. In general, feed through of digital noise is reduced by minimizing the load which the digital outputs are driving.

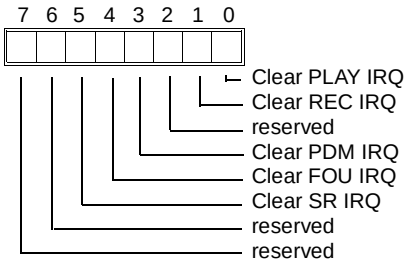
Direct Register Descriptions

The base address is determined externally by an address decoder which selects the chip via the $\overline{CS}$ input.

Status (Base + 0 read)



IRQ Reset (Base + 0 write)



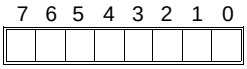
This register provides the driver software easy access to the interrupt source when read. Note that bit 7 indicates the state of the IRQ pin, and hence will be zero when the MIE bit is zero (see "Interrupt Enable" register).

A write to the register is performed to clear interrupts. Writing a one to a given bit will cause the associated interrupt to be cleared. To release the clear interrupt bit and allow further interrupts to occur, a zero must be written back to the bit of interest (some bits have alternate methods of clearing described later). This feature ensures that if the interrupt condition still exists, an edge will be generated on the IRQ pin, thus ensuring recognition on platforms that are edge sensitive. This also allows for a return from interrupt instruction to be executed on the platform while the IRQ line is inactive.

Bit 6 is a special case. There is no IRQ associated with this bit. It is located here for use in Sound Source Emulation Mode, and represents the BUSY status of a Sound Source. When the STATUS is read and tested with 40h, a zero result indicates that the play FIFO is full.

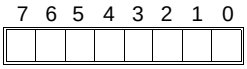
Note that this register can only be read in STAND ALONE mode. Hence, indirect access to this register has been provided at RA=83h for use in COMPANION mode.

Register Address (RA) (Base + 1)

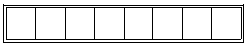


This register is the indirect pointer to direct data transfers to and from the data registers. It is a read/write register. Note that this register can only be read if the chip is in STAND ALONE mode.

Data Low Byte/Word (DLW)



Data High Byte (DH) (Base + 3)



These two addresses are used to accomplish all internal register reading and writing. Most internal registers are 8-bit or less. These are accessed by first writing the appropriate value to the DW, then writing (reading) the data byte to (from) DLW.

I/O Mode FIFO data (RA=0Bh), Algorithm RAM, and Coefficient RAM are always treated as 16-bit entities, and can be transferred in two ways:

- a single operation to/from DLW with $\overline{SBHE}$ = 0
- two successive operations, low byte to/from DLW with $\overline{SBHE}$ = 1, then high byte to/from DH.

Indirect Register Map

Indirect Address	Register
4E	Companion Select Register (write only)
80	Chip Control
81	Interrupt Enables
82	reserved
83	Interrupt status
84	Sample Rate Low 8 bits
85	Sample Rate High 4 bits
86	Sample Rate Control/Status
87	reserved
88	Play DMA Control
89	Play DMA Burst Count
8A	Play DMA Mode
8B	DMA IO Mode Data Port
8C	FIFO Enable/Status
8D	FIFO IRQ Mode
8E	reserved
8F	reserved
90	Power Enable/Status
91	Power Mode
92	reserved
93	reserved
94	DSP Control/Status
95	DSP RAM Address Latch
96	Code RAM Data Port (8/16-bit)
97	Data RAM Data Port (8/16-bit)
98	Record DMA Control
99	Record DMA Burst Count
9A	Record DMA Mode
9B	reserved

Indirect Address	Register
9C	Record FIFO Enable/Status
9D	Record FIFO IRQ Mode
9E	reserved
9F	reserved
A0	Digital Master Volume
A1	DAC Deglitcher Control
A2	reserved
A3	reserved
A4	ADC Control
A5	Analog Volume/Mute
A6	ADC Timing Control
A7	reserved

Indirect Register Definitions

All writeable bits/registers are also readable. In addition, there are some read only bits/registers, which are noted where appropriate.

Reserved bits should be written to zero, and read back zeros. Reserved registers should not be written or read.

Except where noted, registers should be accessed as 8 bit registers via address BASE+2.

General Purpose Registers

IR4E Register Access Mode Select

This register must be written to 01h for any other indirect (or direct) accesses to occur, except for RA writes, which always occur based on chip select. This indirect address allows multiple companion chips to share resources in a system (such as bus buffers, address decodes, interrupts, and DMA channels).

This register is cleared only by hardware reset, and in unaffected by MCR (see below).

IR80 Chip Control

Bits 7:3 - reserved

Bit 2 - Sound Source Emulation Mode (SSMODE)

This bit sets the chip to operate in Sound Source Emulation mode. In Sound Source Emulation Mode, the two address pins (SA1, SA0) are mapped to match the PC parallel port as used by the Sound Source as follows:

Chip Address	Sound Source	IC2002
0	Data	DH
1	Status	Status
2	Control	DL
3	unused	RA

To use this mode, the chip must be configured before the Sound Source compatible application is run (I/O Mode DMA, DSP loaded and running, SR running, etc.). Then, the **IC2002** is put in SSMODE and RA (now at address 3) is written to 8Bh. In the PC, the BIOS pointer to the parallel port is changed to the base address of the **IC2002** chip, and the application can then be started.

This bit is reset by MCR. Hence, it must be set after MCR is set, on a second write to this register.

Bit 1 - Chip STAND ALONE Mode

This bit sets the chip to operate in STAND ALONE mode. In STAND ALONE mode, the STATUS and RA registers are accessible at BASE+0 and BASE+1. This mode should be used to speed register access when the **ICS2002** is being used by itself, without other ICS chips sharing resources (such as address decodes, interrupts, DMA channels, bus buffers, etc.).

When bit 1 is zero, the **ICS2002** will operate in COMPANION mode. In this mode, the STATUS register is mapped only to indirect address 83h. This is done to avoid conflict with other ICS chips that will provide STATUS and RA read back at the first two base addresses.

In addition, STAND ALONE mode configures the DRQP, DRQR, and IRQ pins to operate as outputs, with both one and zero levels being actively driven. When in COMPANION mode, these pins have a strong source for the high state and a weak sink for the low state to allow wire-and connections to other ICS chips.

This bit is reset by hardware reset only, not by MCR.

Bit 0 - Master Chip Reset (MCR)

0 - Hold chip in reset

1 - Remove reset

This bit is cleared to zero by a hardware reset. Thus, any functions reset by MCR are also reset by the RESET pin.

IR81 Interrupt Enables

Bit 7 - Master Interrupt Enable (MIE)

In the zero state, this bit prevents the IRQ pin from going active (high) regardless of the state of any of the individual interrupt sources. It is cleared to zero by MCR. A zero in this bit does not prevent an individual interrupt source from being active in the STATUS register. This allows interrupts to be masked while allowing their status to be polled.

Bit 6 - reserved

Bit 5 - Sample Rate Interrupt Enable (SRIE)

Bit 4 - FIFO Overflow/Underflow Interrupt Enable (FOUIE)

Bit 3 - Power-down Mode Change Interrupt Enable (PMCIE)

Bit 2 - reserved

Bit 1 - Record FIFO Interrupt Enable (RFIE)

Bit 0 - Play FIFO Interrupt Enable (PFIE)

Each of these bits individually enables, one, or disables, zero, their respective interrupt sources from being active in the STATUS register. In addition, there will be no IRQ generated if MIE is one when an individual enable bit is zero. The state of this bit does not affect the source of these interrupts in any way, and they may be polled for activity in the appropriate register for each interrupt type. These bits are all cleared to zero by MCR.

IR83 Status

This register is the same as the direct access status register, except that it can be read in COMPANION mode.

Sample Rate Generator Registers

IR84 Sample Rate Low 8 bits (SRL)

Bits 7:0 - Sample Rate Bits 7:0

IR85 Sample Rate High 4 bits (SRH)

Bits 3:0 - Sample Rate Bits 11:8

Together, these two registers define the record and playback sample rate. Based on the crystal frequency FXtal, and a 12 bit value SR (the concatenation of the two registers), the sample rate will be:

Sample Rate = FXtal * SR / 524288

These registers are **not** initialized by any of the reset mechanisms. Note that the Sample Rate Counter should always be stopped via SRCS bit 0 when these two registers are changed.

IR86 Sample Rate Control/Status (SRCS)

Bits 7:2 - reserved

Bit 1 - Sample Rate Interrupt (SRIRQ) - Read Only

This is set by the hardware whenever the sample rate counter overflows, indicating that a new sample is being input or generated. This bit is cleared by any of the following actions:

- Master Chip Reset
- Sample Rate Run = 0 (SRR bit 0)
- a write to STATUS with bit 5 = 1
- any write to SRCS

Bit 0 - Sample Rate Run (SRR)

This bit resets the Sample Rate Counter, the SRIRQ bit, and shuts down the sampling and playback pro-cesses when written to a zero. When written to a one, the sample rate generator runs at the programmed rate. SRR is internally synchronized to the master clock to provide clean starts and stops of the counter. MCR clears this bit.

Play DMA Control and Status Registers

IR88 Play DMA Control (DMACTL)

Bits 7 - reserved

Bit 6 - TC Reset Mask

When set to 1, this bit masks the 'DMA Run' bit reset upon receipt of TC, terminal count, signal from the ISA bus. When reset to 0, the 'DMA Run' bit will be reset upon receipt of TC.

Bits 5:1 - reserved

Bit 0 - DMA Run

This bit enables the DMA hardware to begin transferring data when set to one. It is cleared by either MCR or receipt of a TC when 'TC Reset Mask' is a zero (see the DMAMODE register for details).

IR89 Play DMA Burst Count (DMABC)

Bits 7:6 - reserved

Bits 5:0 - DMA Burst Count

This value determines the number of DMA transfers that take place for each DMA request issued to the host. The actual number of transfers will be DMABC+1. Thus, for single transfer mode, program this register to zero. The burst counter is automatically preset to the burst count whenever the $\overline{\text{DACKP}}$ input is high. Thus, there is no need to reprogram the count value after TC, since the next transfer will use the full programmed count value. This register has no affect on I/O Mode data transfers, since its only influence is over the DRQP output. This register is not initialized by any means other than a direct write, and hence must be written to before DMA is enabled.

IR8A Play DMA Mode (DMAMODE)

All bits in this register are cleared by MCR.

Bits 7:6 - reserved

Bit 5 - Terminal Count Interrupt (TCIRQ) - (read only)

This bit indicates that a Terminal Count has been received on the last DMA operation. If the PFIE and PLAYIRQ bits have been programmed to a one, an interrupt will be generated at the end of the last DMA operation. This bit is cleared by MCR or a write to STATUS with bit 0 = one. The reset state is then removed by either writing the STATUS bit 0 to zero.

Bit 4 - I/O Mode Transfer (IOXFER)

When this bit is a one, the DMA hardware (DRQP and TCIRQ) is disabled. Data transfers take place via IR8Bh, and are required to be treated as 16-bit transfers. Thus, data should be written to DLW (with $\overline{\text{SBHE}}$ = low, 16-bit data) or to DLW (with $\overline{\text{SBHE}}$ = high, 8-bit data low byte) followed by DH (8-bit data, high byte). It is also the programmers responsibility to ensure that DMAMODE bit 2 (DMA16) is set to a one for all I/O mode transfers.

Bit 3 - Unsigned Data (USIGN)

When set to a one, this bit expects to receive (and will generate) unsigned data. The native data format is Signed Binary Twos Complement. This bit will invert the most significant bit of each data byte (or word, depending on the state of DATATYPE). Note that this bit should be zero when the DATATYPE indicates u-law or A- law data formats.

Bit 2 - 16 Bit Data (DMA16)

When set to a one, this bit causes the hardware to expect data to be sent in 16-bit words. When low, the hardware expects 8-bit bytes. This bit must be set to one when performing I/O mode transfers, as all I/O transfers are treated as 16 bit values.

Bit 1:0 - Data Type (DATATYPE)

These bits direct the hardware how to interpret the outgoing data. This is independent of the DMA or I/O data width. It effects how data is signed and how data is packed to and unpacked from the Play FIFO. The DATATYPE field selects the format of data for playback.

Value	Data Type
00	8-bit linear
01	16-bit linear
10	8-bit μ256 Law
11	8-bit A-Law

IR8B DMA I/O Mode Data Port (DMADATA) (8/16-bit)

This register address is used to trap I/O mode data to and from the FIFOs. It is only used in I/O mode. See the description of the IOXFER bits for more details.

When DMA16 is one, this register MUST be accessed as a sixteen bit value. Note that this can be done from either an eight or sixteen bit ISA slot, since the chip used $\overline{\text{SBHE}}$ to determine the proper byte swapping.

FIFO Control/Status Registers

IR8C FIFO Enable/Status (FES)

Bit 0 - FIFO Enable (FE)
This bit holds the FIFO in a reset state when low, and enables the FIFO to operate when high. This bit is reset by MCR. This bit, when low, also resets all FIFO related conditions (see the following bits) and prevents DMA start requests from being issued. It does not reset the FIFO IRQ Mode register.

Bit 1 - FIFO Overflow (read only)
This bit is set when a FIFO shift in command is generated (by either DMA, I/O, or the DSP) with the FIFO full, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 2 - FIFO Underflow (read only)
This bit is set when a FIFO shift out command is generated (by either DMA, I/O, or the DSP) with the FIFO empty, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 3 - FIFO 25% Full (read only)
This bit goes high after 4 words (or 8 bytes) have been loaded into the FIFO, and low again when 13 words (or 26 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 4 - FIFO 50% Full (read only)
This bit goes high after 8 words (or 16 bytes) have been loaded into the FIFO, and low again when 9 words (or 18 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 5 - FIFO 75% Full (read only)
This bit goes high after 12 words (or 24 bytes) have been loaded into the FIFO, and low again when 5 words (or 10 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 6 - FIFO DIR (read only)
This bit goes high when a single word (or two bytes) may be written to the FIFO. There is no interrupt associated with this bit directly. Note that this bit resets to a one because when the FIFO is reset it is forced to be empty, and hence is ready to accept data.

Bit 7 - FIFO DOR (read only)
This bit goes high when a single word (or two bytes) may be read from the FIFO. There is no interrupt associated with this bit directly.

IR8D FIFO IRQ Mode

This register must never be written to when the FIFO is enabled. Invalid interrupts and DMA requests could be generated as a result.

Bits 7:4 - reserved

Bit 3 - FIFO IRQ Enable (FIE)
This bit enables the various FIFO capacity thresholds to generate interrupts (as PLAYIRQ) when one. When zero, this bit prevents FIFO capacity IRQ generation when operating in DMA mode, which only needs TCIRQ.

Bits 2:0 - FIFO Ready IRQ Mode Selection
This field defines FIFO utilization for both DMA and I/O mode data transfers. In I/O mode, it is used to generate interrupts (FRDYIRQ) when the FIFO capacity reaches a predefined point. For DMA transfers, it signals the DMA logic to request a transfer at those same predefined points. By programming the DMA Burst Count appropriately, the FIFO may be easily kept near the desired capacity.

The following table describes the selections available:

Bits 2:0	IRQ/DRQ Source	Notes
000	DIR	Ready to take 1 word from HOST
001	EMPTY 75%	Ready to take 13 words from HOST
010	EMPTY 50%	Ready to take 9 words from HOST
011	EMPTY 25%	Ready to take 5 words from HOST
100	DOR	Ready to provide 1 word to DSP
101	FULL 25%	Ready to provide 4 words to DSP
110	FULL 50%	Ready to provide 8 words to DSP
111	FULL 75%	Ready to provide 12 words to DSP

Note that for byte transfers (DMA16=0), the numbers listed above should be doubled.

This must be programmed before the FIFO is enabled. It may be changed while the FIFO is enabled, if necessary. This register is cleared by MCR, but not by FE low.

IR8E reserved

IR8F Play FIFO Output Data Read Back (8/16 bit)

This register is provided for test use only, although it may find system level use as a diagnostic tool.

Power Control and Status

IR90 Power Enable/Status (PEST)

Bit 7 - PWRIRQ (read only)

This bit is a one when either edge has occurred on the $\overline{\text{PWRDN}}$ pin, and the edge enable in the Power Mode register is set. If bit 3 of the MIE is one, this will also generate an external interrupt. In any case, this bit is also visible as STATUS register bit 3. PWRIRQ is reset by disabling both edge enable bits or resetting the edge interrupts (see below).

Bits 6:5 - reserved

Bit 4 - ADCPWR Disable

This bit controls the power state of the ADC analog circuitry. When 0, ADC analog power is controlled by the SOFTPWR bit the same as the DAC analog power is. When this bit is set to a 1, the ADC analog power is turned off independent of the state of SOFTPWR.

This feature is included for advanced power management routines, as chip power dissipation can be reduced by almost half by turning ADC power off when not in use. Note, however, that several milliseconds of settling time is required after power is turned on before the ADC functions properly.

Bit 3 - $\overline{\text{PWRDN}}$ Pin Value (read only)

This bit indicates the state of the $\overline{\text{PWRDN}}$ pin.

Bit 2 - FALLIRQ (read only)

This bit is set when the $\overline{\text{PWRDN}}$ pin makes a transition from high to low. If PWRMODE bit 2 (FALLIE) is one, this will cause PWRIRQ to go high as well. This bit is reset by one of the following:

- MCR
- any write to PEST
- a write to STATUS with bit 3 set to one. This will hold the bit reset until released by a write to STATUS with bit 3 cleared to zero.

Note that FALLIE does not mask this bit, allowing polling to be performed.

Bit 1 - RISEIRQ (read only)

This bit is set when the $\overline{\text{PWRDN}}$ pin makes a transition from low to high. If PWRMODE bit 1 (RISEIE) is one, this will cause PWRIRQ to go high as well. This bit is reset by one of the following:

- MCR
- any write to PEST
- a write to STATUS with bit 3 set to one. This will hold the bit reset until released by a write to STATUS with bit 3 cleared to zero.

Note that RISEIE does not mask this bit, allowing polling to be performed.

Bit 0 - Soft Power (SOFTPWR)

The function of this bit depends on the status of the "SWMODE" bit (bit 0 of PWRMODE). When SWMODE is zero, writes to this bit have no affect. Reads will return the state of the PWRDN* pin, which is also the state of the on chip PWRON control signal. When SWMODE is a one, a write of one to this bit turns on power to the chip analog circuitry, while a zero clears this bit and puts the chip in a low power mode. Reads will return the last value written.

IR91 Power Mode (PWRMODE)

All bits in this register are cleared by MCR.

Bits 7:3 - reserved

Bit 2 - Fall IRQ Enable (FALLIE)

When set to one, this bit allows a falling edge on $\overline{\text{PWRDN}}$ to cause PWRIRQ to go high. It does not mask PEST bit 2.

Bit 1 - Rise IRQ Enable (RISEIE)

When set to one, this bit allows a rising edge on $\overline{\text{PWRDN}}$ to cause PWRIRQ to go high. It does not mask PEST bit 1.

Bit 0 - Software Mode (SWMODE)

When cleared to zero, this bit causes the chip to operate in a "hardware driven" mode; that is, the $\overline{\text{PWRDN}}$ pin directly controls the chip analog power (for low power consumption). In this mode, a low on $\overline{\text{PWRDN}}$ puts the chip in low power mode, while a high enables normal operation. When set to a one, this bit causes the chip to operate in a "software driven" mode. In this mode, changes on the $\overline{\text{PWRDN}}$ pin only generate interrupts. The hardware low power mode is then controlled (via software) by SOFTPWR (bit 0 of PEST). This function allows "clean" software controlled turn on and off of the analog circuitry power.

IR92 reserved

IR93 reserved

IR94 DSP Control/Status (DSPCS)

Bits 7:4 - Index Counter Value (Read Only)

This value indicates the current contents of the DSP address Index Counter, and is provided as a code debug aid for use in Step Mode. In normal operation it should be ignored. It is reset to zero when the DSP is not running, and increments by one at the completion of each "pass" of the DSP engine.

Bit 3 - DSP Sequence Complete (Read only)

This bit is set each time the DSP completes its sequence and restarts. It is reset to zero when the DSPRUN bit is zero or after a read of this register.

Bit 2 - DSP Output Saturation Detect

This bit is set to one whenever the DSP output value written to any output destination (DATA RAM, DAC, or Record FIFO) exceeds a sixteen bit signed range. In these cases, the DSP output saturates to $7FFF or $8000 (for positive or negative values) rather than overflowing. It is reset to zero when the DSPRUN bit is zero or after a read of this register.

Bit 1 - DSP Step Mode

This bit is intended as a DSP code debug aid only. When set to a one, this bit halts the DSP microcode sequencer at the end of each "pass" of code. This enables the host to read the DATA RAM contents to check the results of the previous calculations. Note that writes to the Record FIFO and DAC will be captured by the DATA RAM "under" them to aid with debug efforts. For normal operation, this bit **MUST** be set to a zero.

Bit 0 - DSP Run

When written to one, this bit starts the DSP engine running. A zero stops and resets the DSP engine execution. This bit is reset by MCR.

Before running the DSP, the Code and Data RAMs must be loaded. To do this, perform the following:

1) write 95h (DSPRA) to the desired address
2) write 96h (Code Ram data) or 97h (Data RAM data) to the desired 16-bit value.
3) repeat 1 and 2 for all RAM locations of both RAMs.
4) when done, write any data to DSPRA to reset the load logic.

ICS will provide algorithm and constants data supporting filtering functions for various sample rates.

Note that when the DSP is running, it is forbidden to read or write either the Code or Data RAMs (except when halted in STEP mode, see above). Also, after writing to the Code or Data RAMs to load them, and before starting the DSP, you must reset the RAM load hardware by writing to the DSPRA register (the value written is ignored).

IR95 DSP RAM Address Latch (DSPRA) (write only)

Bit 7 - Read

When one, this bit indicates that the next DSP RAM operation is a read. Zero indicates a write operation.

Bits 5:0 - DSP RAM Address

These bits are the address for the next DSP RAM data transfer. Note that the Code RAM address can be $00 through $3f, and the Data RAM address can be $00 through $1F.

IR96 Code RAM Data Port (8/16-bit)

Bits B:0 - Code RAM Data

This 8/16-bit port is data to be read from/written to the DSP Code RAM. The data is the low 12 bits of the word.

IR97 Data RAM Data Port (8/16-bit)

Bits F:0 - Data RAM Data

This 8/16-bit port is the data to be read from/written to the DSP Data RAM. The data is a full 16-bit word.

Record DMA Control and Status Registers

IR98 Record DMA Control (DMACTL)

Bits 7 - reserved

Bit 6 - TC Reset Mask

When set to 1, this bit masks the 'DMA Run' bit reset upon receipt of TC, terminal count, signal from the ISA bus. When reset to 0, the 'DMA Run' bit will be reset upon receipt of TC.

Bits 5:1 - reserved

Bit 0 - DMA Run

This bit enables the DMA hardware to begin transferring data when set to one. It is cleared by either MCR or receipt of a TC when 'TC Reset Mask' is a zero (see the DMAMODE register for details).

IR99 Record DMA Burst Count (RDMABC)

Bits 7:6 - reserved

Bits 5:0 - Record DMA Burst Count

This value determines the number of DMA transfers that take place for each DMA request issued to the host. The actual number of transfers will be RDMABC + 1. Thus, for single transfer mode, program this register to zero. The burst counter is automatically preset to the burst count whenever the $\overline{\text{DACKR}}$ input is high. Thus, there is no need to reprogram the count value after TC, since the next transfer will use the full programmed count value. This register has no affect on I/O Mode data transfers, since its only influence is over the DRQR output. This register is not initialized by any means other than a direct write, and hence must be written to before DMA is enabled.

IR9A Record DMA Mode (RDMAMODE)

All bits in this register are cleared by MCR.

Bits 7:6 - reserved

Bit 5 - Terminal Count Interrupt (RTCIRQ) (read only)

This bit indicates that a Terminal Count has been received on the last DMA operation. If the RECIE bit has been programmed to a one, an interrupt will be generated at the end of the last DMA operation. This bit is cleared by MCR or a write to STATUS with bit 1 = 1. The reset state is then removed by either writing the STATUS bit 0 to 0, or by the next DMA operation. Hence, there is no need to "remove" this reset as there is for other IRQ reset operations.

Bit 4 - Record I/O Mode Transfer (RIOXFER)

When this bit is a one, the DMA hardware (DRQR and RTCIRQ) is disabled. Data transfers take place via RA $8B (NOT $9B), and are required to be treated as 16-bit transfers. Thus, data should be read from DLW (with $\overline{\text{SBHE}}$ = 0, 16-bit data) or from DLW (with $\overline{\text{SBHE}}$ = 1, 8-bit data low byte) followed by DH (8-bit data, high byte). It is also the programmers responsibility to ensure that RDMAMODE bit 1 (RDMA16) is set to a one for all I/O mode transfers.

Bit 3 - Unsigned Data (RUSIGN)

When set to a one, the record FIFO will generate unsigned data. The native data format is Signed Binary Twos Complement. This bit will invert the most significant bit of each data byte (or word, depending on the state of RDATATYPE).

Bit 2 - 16-Bit DMA (RDMA16)

When set to a one, this bit causes the hardware to expect data to be sent in 16-bit words. When low, the hardware expects 8-bit bytes. This bit must be set to one when performing I/O mode transfers, as all I/O transfers are treated as 16-bit entities.

Bits 1:0 - Record Data Type (RDATATYPE)

These bits direct the hardware how to interpret the incoming data. Note that this is independent of the DMA or I/O data width. It effects how data is "signed" and how data is packed to/unpacked from the Record FIFO.

Value	Data Type
00	8-bit linear
01	16-bit linear
10	reserved
11	reserved

IR9B reserved

Record FIFO Control/Status Registers

IR9C Record FIFO Enable/Status (RFES)

Bit 0 - Record FIFO Enable (RFE)

This bit holds the record FIFO in a reset state when low, and enables the FIFO to operate when high. This bit is reset by MCR. This bit, when low, also resets all FIFO related conditions (see the following bits) and prevents DMA start requests from being issued. It does not reset the Record FIFO IRQ Mode register.

Bit 1 - FIFO Overflow (read only)

This bit is set when a FIFO shift in command is generated (by either DMA, I/O, or the DSP) with the FIFO full, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 2 - FIFO Underflow (read only)

This bit is set when a FIFO shift out command is generated (by either DMA, I/O, or the DSP) with the FIFO empty, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 3 - FIFO 25% Full (read only)
This bit goes high after 4 words (or 8 bytes) have been loaded into the FIFO, and low again when 5 words (or 10 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 4 - FIFO 50% Full (read only)
This bit goes high after 8 words (or 16 bytes) have been loaded into the FIFO, and low again when 9 words (or 18 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 5 - FIFO 75% Full (read only)
This bit goes high after 12 words (or 24 bytes) have been loaded into the FIFO, and low again when 13 words (or 26 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 6 - FIFO DIR (read only)
This bit goes high when a single word (or two bytes) may be written to the FIFO. There is no interrupt associated with this bit directly. Note that this bit resets to a one because when the FIFO is reset it is forced to be "empty," and hence is ready to accept data.

Bit 7 - FIFO DOR (read only)
This bit goes high when a single word (or two bytes) may be read from the FIFO. There is no interrupt associated with this bit directly.

IR9D Record FIFO IRQ Mode

Bits 7:4 - reserved

Bit 3 - FIFO IRQ Enable (RFIE)
This bit enables the various FIFO capacity thresholds to generate interrupts (as RECIRQ) when one. When zero, this bit prevents FIFO capacity IRQ generation when operating in DMA mode, which only needs RTCIRQ.

Bits 2:0 - FIFO Ready IRQ Mode Selection
This register defines FIFO utilization for both DMA and I/O mode data transfers. In I/O mode, it is used to generate interrupts (RECIRQ) when the FIFO capacity reaches a predefined point. For DMA transfers, it signals the DMA logic to request a transfer at those same predefined points. By programming the Record DMA Burst Count appropriately, the FIFO may be easily kept near the desired capacity.

The following table describes the selections available:

Bits 2:0	Source	Notes
000	DIR	Ready to take 1 word from DSP
001	EMPTY 75%	Ready to take 13 words from DSP
010	EMPTY 50%	Ready to take 9 words from DSP
011	EMPTY 25%	Ready to take 5 words from DSP
100	DOR	Ready to provide 1 word to HOST
101	FULL 25%	Ready to provide 4 words to HOST
110	FULL 50%	Ready to provide 8 words to HOST
111	FULL 75%	Ready to provide 12 words

Note that for byte transfers (RDMA16=0), the numbers listed above should be doubled.

This must be programmed before the FIFO is enabled. It may be changed while the FIFO is enabled if necessary. This register is cleared by MCR, but not by RFE low.

IR9E reserved

IR9F reserved

Miscellaneous Registers

IRA0 Digital Master Volume

Bits 7:0 - Volume
This value is used to scale all values that are output from the DSP to the DAC. It may be written while the DSP is running.

The value written is interpreted as to give a log scale output response of 0.1875dB per step. The value for nominal (0dB attenuation) is E0h. A value of FFh gives 5.8125dB of gain. Note that any value above E0h may result in digital saturation of the internal 16 bit data value.

IRA1 DAC De-glitcher Control

Bits 7:3 - Volume bits 7:3 (read only)

Bit 2 - DAC Enable Bit (read only, for test)

Bits 1:0 - DAC De-glitch Width

Code	Notes
00	De-glitcher disabled
01	Minimum de-glitch width
10	Nominal de-glitch width
11	Maximum de-glitch width

This value is determined by the clock rate at which the chip is run. ICS will provide the proper value for an application. This register is also used for test purposes.

This register is not initialized in any way and should be programmed before muting is removed.

IRA2 reserved

IRA3 reserved

ADC and Analog Control Registers

IRA4 ADC Control

Bits 7:3 - reserved

Bit 2 - ADC Test Mode

This bit is for factory testing use only, and must always be programmed to zero by an application. It is reset to zero by a zero in ADCRUN, and hence takes two writes of $05 to this register to activate for safety.

Bit 1 - reserved

Bit 0 - ADC Run

When written to a one, this bit enables the ADC hardware to run. Note that the ADC Timing Control register should be programmed appropriately first. Also note that the DSP must be running (and programmed properly) for the conversion results to be retrieved. The Sample Rate Generator determines the rate at which the conversion data is loaded into the Record FIFO.

This bit is cleared to zero by MCR.

Note that this bit, when 0, shuts down the successive approximation logic, the dynamic comparators and various logic functions. When the ADC is not being used, disabling it via this bit reduces background noise in the playback section and power consumption, and thus is recommended.

IRA5 Analog Volume/Mute

Bits 7:5 - reserved

Bits 4:1 - Analog Volume

These bits set the analog output level, in 1.5dB steps. All bits one gives 0dB attenuation of the DAC output signal, and all bits zero gives full attenuation. These bits are unaffected by any reset mechanism.

Bit 0 - Audio Enable

This bit disconnects the audio output of the output buffer amp and sets the BUFOUT pin to the nominal bias voltage when cleared to zero. When set to one, it passes the output of the output buffer amp to the BUFOUT pin.

The main function of this bit is to prevent sudden DC offset changes on the BUFOUT pin when entering and leaving power-down mode. By proper software procedure, noiseless transitions can be made.

This bit is cleared to zero by MCR.

IRA6 ADC Timing Control

This register is used to control the ADC internal operation timing.

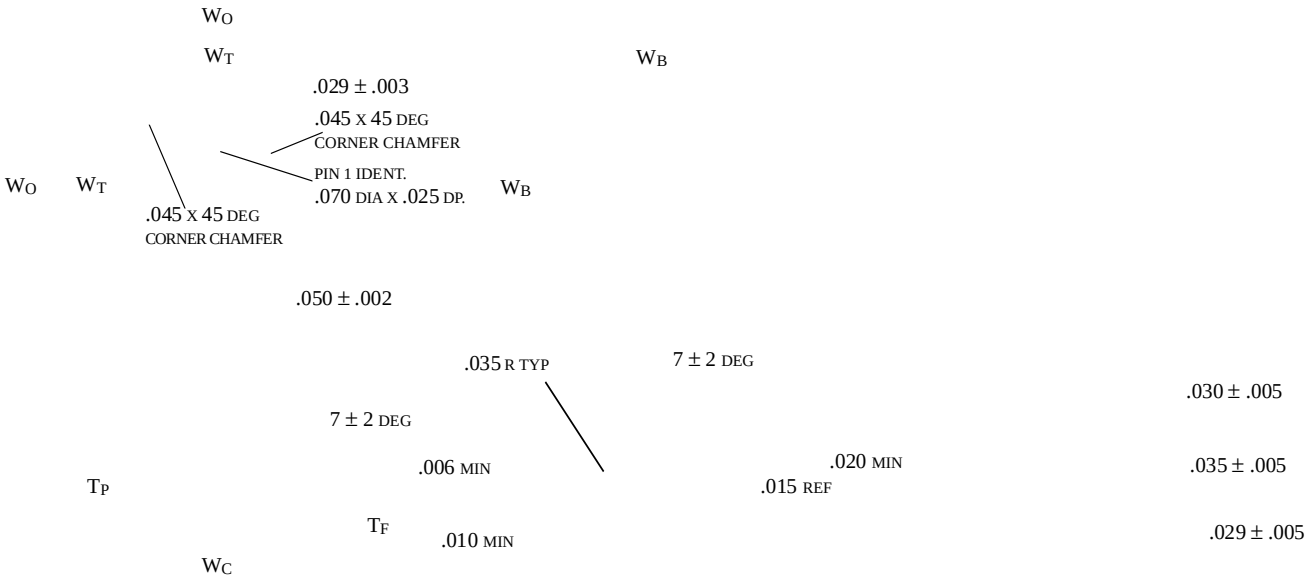
Bits 7:4 - Comparator Timing Control

These bits control the time of comparator input switching. Bits 7:5 are the count, and bit 4 is 0 for half cycle and 1 full cycle delays.

Bits 3:1 - Cycle Timing Control

These bits control the number of clocks used for each step of the successive approximation process. For the full 64 step DSP cycle, the value of these bits should be 7. For a 40 step cycle, the value should be 4.

Bit 0 - reserved



44-Pin PLCC Package

LEAD COUNT	FRAME THICKNESS TF +/-.003	PKG. THICKNESS TP +/-.004	PKG. WIDTH TOP WT +/-.004	PKG. WIDTH BOTTOM WB +/-.066	OVERALL PKG. WIDTH WO +/-.005	CONTACT WIDTH WO +.010/-.030
44L	0.010	0.152	0.650	0.623	0.690	0.620

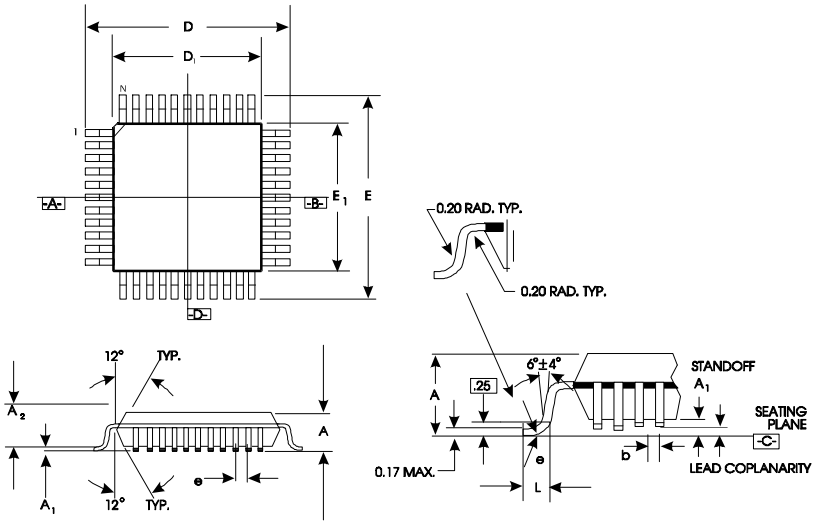
Ordering Information

ICS2002V

Example:

ICS XXXX M

Package Type
V=PLCC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device



TQFP Package

LEAD COUNT		44L
BODY THICKNESS		1.00
FOOTPRINT (BODY+)		2.00
DIMENSIONS	TOLERANCE	
A	MAX.	1.20
A_1		0.05 MIN./0.10 MAX.
A_2	±0.5	1.00
D	±0.25	12.00
D_1	±0.10	10.00
E	±0.25	12.00
E_1	±0.10	10.00
L	±0.15/-0.10	0.60
e	BASIC	0.80
b	+0.05	0.35
ccc	MAX.	0.10
ddd		0.20 MAX.
0		0° - 7°

Ordering Information

ICS2002Y

Example:

ICS XXXX M

Package Type
Y=QFP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device