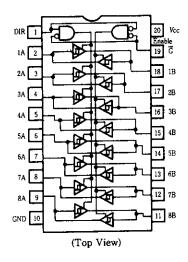
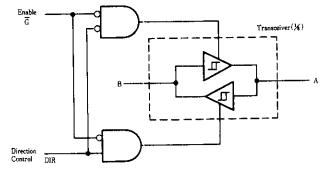
# HD74LS641-1 • Octal Bus Transceivers (non-inverted open-collector outputs)

This octal bus transceivers is designed for asynchronous two-way communication between data buses. The devices transmit data, from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input  $(\overline{G})$  can be used to disable the device so that the buses are effectively isolated.

#### PIN ARRANGEMENT



#### BLOCK DIAGRAM



## **TRECOMMENDED OPERATING CONDITIONS**

Item	Symbol	min	typ	max	Unit
Supply voltage	Vcc	4.75	5.00	5.25	V
Output voltage	Vон		_	5.5	v
Output current	Iol		-	48	mA
Operating temperature range	Topr	-20	25	75	°C

## FUNCTION TABLE

Enable		Operation		
G	DIR			
L	L	B data to A bus		
L	н	A data to B bus		
H ×		Isolation		

Notes) H; high level, L; low level, X; irrelevant

## **ELECTRICAL CHARACTERISTICS** (*Ta*=-20~+75°C)

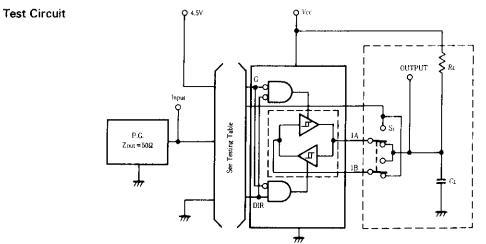
It	iem	Symbol	Test Conditions		min	typ*	max	Un
Input vol <b>tage</b>		Vin			2.0			V
		VIL		- 1	_	0.8	v	
Hysteres	is	$V_T^+ - V_T^-$	$V_{CC} = 4.75 V$		0.2			v
Output cu	urrent	Іон	$V_{CC} = 4.75 V, V_{IH} = 2V, V_{IL} = 0.8$	$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8 \text{V}, V_{OH} = 5.5 \text{V}$		··-	100	μF
				$I_{DL} = 12 \text{mA}$			0.4	v
Output vo	Output voltage	Voi	$V_{CC} = 4.75 \text{V}, V_{1H} = 2 \text{V}, V_{1L} = 0.8 \text{V}$	$Io_L = 24 \text{mA}$			0.5	v
				IoL = 48 mA		_	0.5	ν
Input current		Іін	$V_{CC} = 5.25 \text{V}, V_I = 2.7 \text{V}$				20	μ
		In	$V_{CC} = 5.25 \text{V}, V_I = 0.4 \text{V}$				400	μ
A or B DIR or $\overline{G}$	A or B	T	$V_{\rm CC} = 5.25 V$	$V_I = 5.5 V$			0.1	m
	DIR or $\overline{G}$			$V_I = 7 V$			0.1	m
Supply current		Іссн				48	70	m
		Icc1.	Vcc=5.25V, output open		62	90	m	
		Iccz			64	95	m	
Input clar	mp voltage	Vik	$V_{cc} = 4.75 \text{V}, I_{IN} = -18 \text{mA}$			····	-1.5	v

\*  $V_{CC} = 5V, Ta = 25^{\circ}C$ 

### **EXAMPLE 1** SWITCHING CHARACTERISTICS ( $V_{cc}=5V$ , $Ta=25^{\circ}C$ )

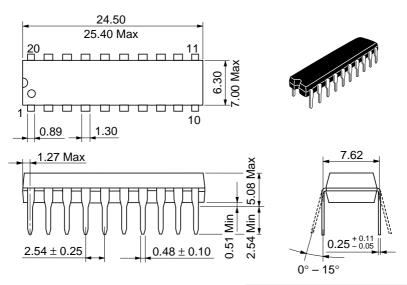
Item	Symbol	INPUT	OUTPUT	Test Conditions	min	typ	max	Unit
December 11	4	A	В			17	25	ns
	tplh	В	A		-	17	25	ns
Propagation delay time		A	В			16	25	ns
	tphl	В	A	C = 15 - D = 2600 O		16	25	ns
Output enable time		Ğ	A	$C_L = 45 \mathrm{pF}, R_L = 667 \Omega$		23	40	ns
	tplh	Ğ	В		—	25	40	ns
	4	Ē	A			34	50	ns
	tphL	Ē	В			37	50	ns

#### **TESTING METHOD**



- Notes) 1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B, are identical to above load circuit.
  - 2.  $C_L$  includes probe and jig capacitance. 3.  $S_1$  is a input-output switch.

Unit: mm



Hitachi Code	DP-20N
JEDEC	
EIAJ	Conforms
Weight (reference value)	1.26 g

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