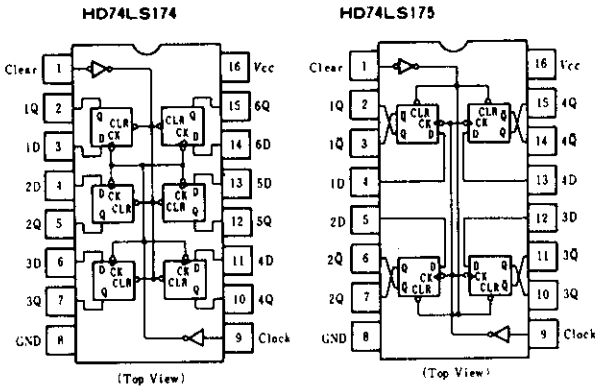


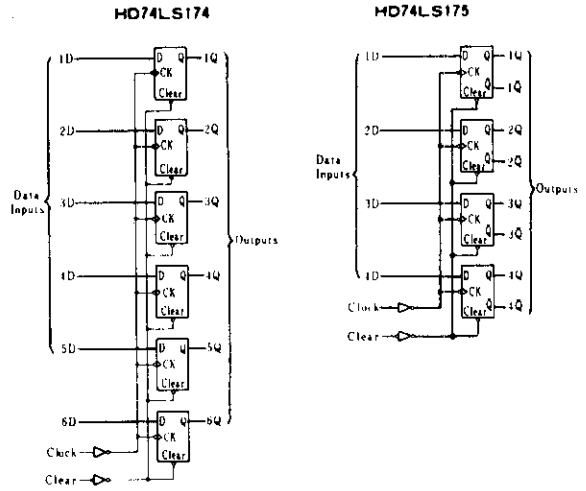
# HD74LS174/HD74LS175 ●Hex/Quadruple D-type Flip-Flops (with clear)

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the HD74LS175 features complementary outputs from each flip-flops. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the outputs.

## ■PIN ARRANGEMENT



## ■BLOCK DIAGRAM



## ■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	max	Unit
Clock frequency	$f_{clock}$	0	30	MHz
Clock pulse width	$t_w(CK)$	20	—	ns
Clear pulse width	$t_w(CLR)$	20	—	ns
Setup time	Data input	$t_{st}(data)$	20	ns
	Clear inactive-state	$t_{st}(CLR)$	25	ns
Data hold time	$t_h(data)$	5	—	ns

## ■ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	$V_{IH}$		2.0	—	—	V	
	$V_{IL}$		—	—	0.8	V	
Output voltage	$V_{OH}$	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -400\mu\text{A}$	2.7	—	—	V	
	$V_{OL}$	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}$	$I_{OL} = 8\text{mA}$	—	—	0.5	V
			$I_{OL} = 4\text{mA}$	—	—	0.4	
Input current	$I_I$	$V_{CC} = 5.25\text{V}, V_i = 7\text{V}$	—	—	0.1	mA	
	$I_{IH}$	$V_{CC} = 5.25\text{V}, V_i = 2.7\text{V}$	—	—	20	$\mu\text{A}$	
	$I_{IL}$	$V_{CC} = 5.25\text{V}, V_i = 0.4\text{V}$	—	—	-0.4	mA	
Short-circuit output current	$I_{OS}$	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA	
Supply current**	$I_{CC}$	$V_{CC} = 5.25\text{V}$	HD74LS174	—	16	26	mA
			HD74LS175	—	11	18	
Input clamp voltage	$V_{IK}$	$V_{CC} = 4.75\text{V}, I_{IN} = -18\text{mA}$	—	—	-1.5	V	

\*  $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$

\*\* With all outputs open and 4.5V applied to all data and clear inputs,  $I_{CC}$  is measured after a momentary grounded, then 4.5V, is applied to clock.

## ■FUNCTION TABLE

Inputs			Outputs	
Clear	Clock	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	$Q_0$	$\bar{Q}_0$

- Notes) 1. H; high level, L; low level, X; irrelevant  
 2. ↑; transition from low to high level  
 3.  $Q_0$ ; the level of Q before the indicated steady-state input conditions were established.  
 4.  $\bar{Q}$  is applied to HD74LS175 only.

# HD74LS174/HD74LS175

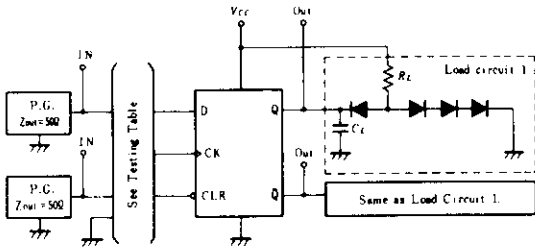
## SWITCHING CHARACTERISTICS ( $V_{CC}=5V, T_a=25^\circ C$ )

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	$f_{max}$	Clock	Q, $\bar{Q}^*$	$C_L = 15pF, R_L = 2k\Omega$	30	40	—	MHz
Propagation delay time	$t_{PLH}$	Clear	$\bar{Q}^*$		—	16	25	ns
	$t_{PHL}$		Q		—	23	35	
	$t_{PLH}$	Clock	Q, $\bar{Q}^*$		—	20	30	
	$t_{PHL}$	Clock	Q, $\bar{Q}^*$	—	21	30		

\* HD74LS175 only

## TESTING METHOD

### 1) Test Circuit



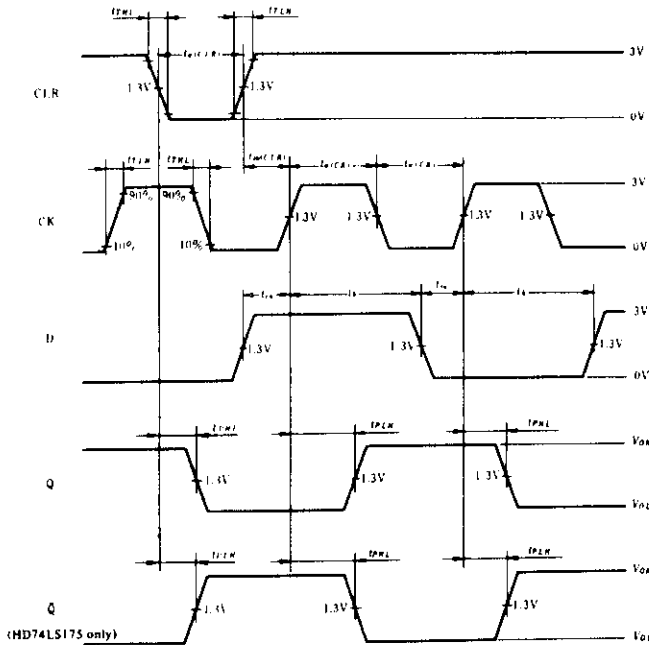
### 2) Testing Table

Item	From input to output	Inputs			Outputs	
		CLR	CK	D	Q	$\bar{Q}^*$
$f_{max}$	CK → Q, $\bar{Q}^*$	4.5V	IN	IN	OUT	OUT
$t_{PLH}$	CK → Q, $\bar{Q}^*$	4.5V	IN	IN		
$t_{PHL}$	CLR → Q, $\bar{Q}^*$	IN	IN	4.5V		

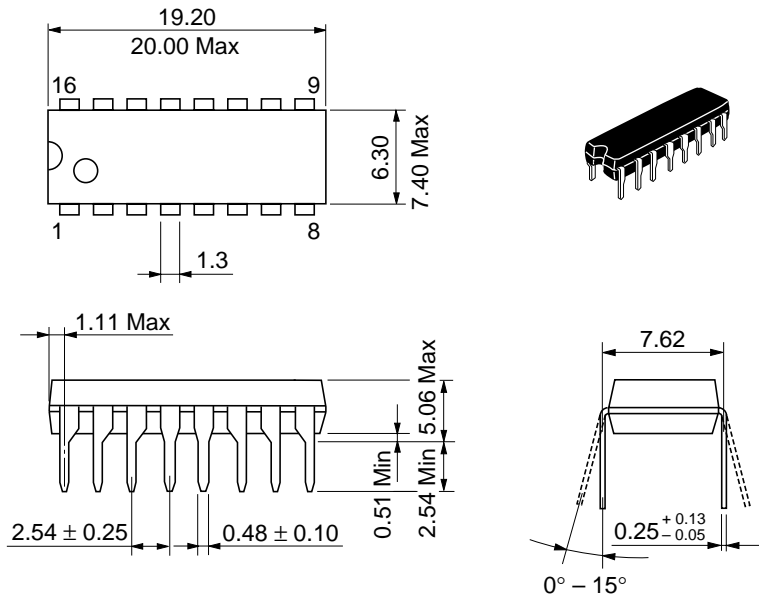
\* HD74LS175 only

- Notes) 1. Test is put into the each flip-flop  
 2. All diodes are 1S2074 (H).  
 3.  $C_L$  includes probe and jig capacitance.

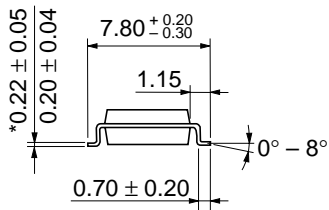
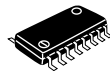
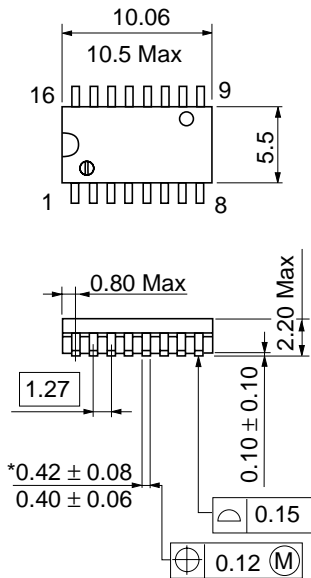
### Waveform



- Notes) 1. Input pulse;  $t_{TLH} \leq 15ns, t_{THL} \leq 6ns, PRR=1MHz$   
 and: for  $f_{max}, t_{TLH}=t_{THL} \leq 2.5ns$ .

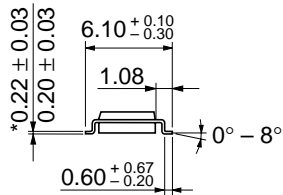
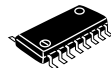
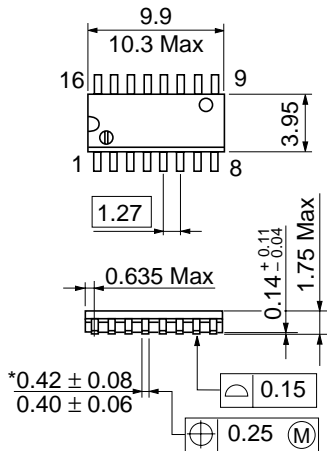


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

\*Dimension including the plating thickness  
Base material dimension

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