
HD74HC237

3-to-8-line Decoder/Demultiplexer with Address Latch

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Description

The HD74HC237 decodes a three-bit Address to one-of-eight active-high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HD74HD237 is the noninverting version of the HD74HC137.

Features

- High Speed Operation: t_{pd} (Data to Y) = 19 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

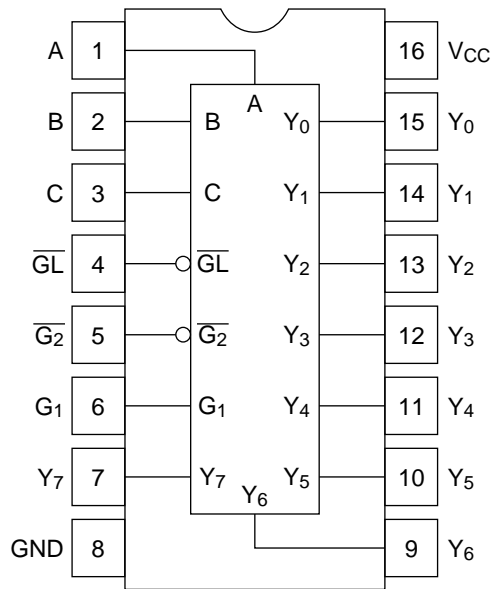
HD74HC237

Function Table

Inputs

Enable			Select			Outputs							
$\overline{G_L}$	G_1	$\overline{G_2}$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address H; all others L							

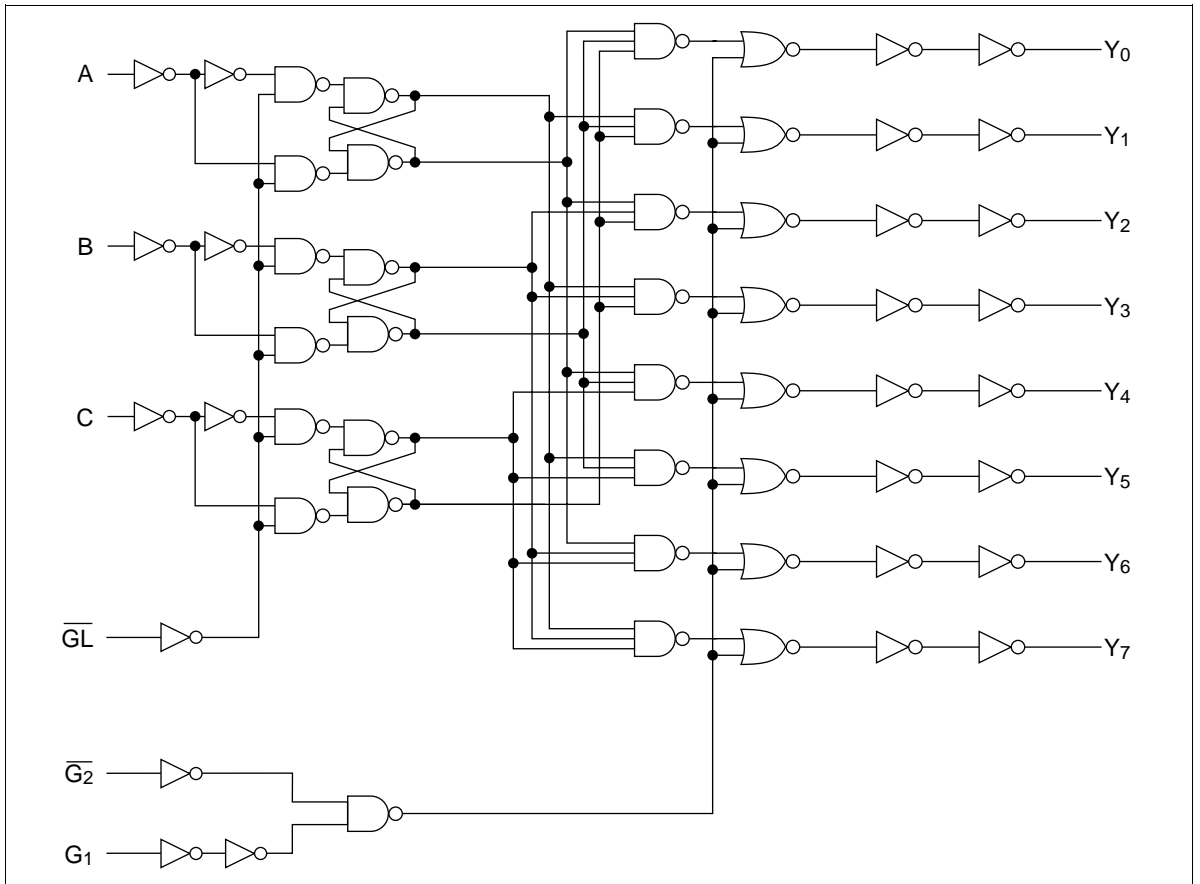
Pin Arrangement



(Top view)

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Logic Diagram

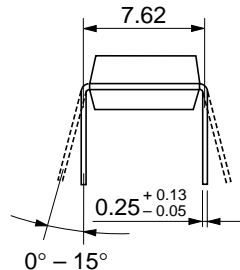
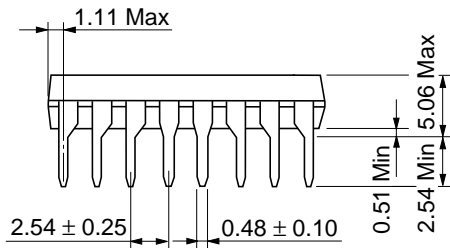
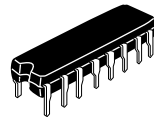
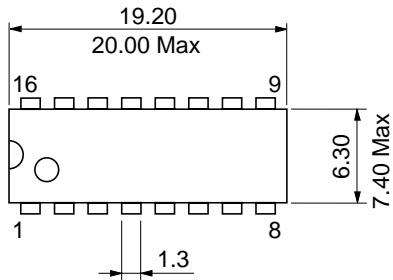


DC Characteristics

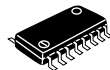
Item	Symbol	V _{CC} (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V _{IL}	2.0	—	—	0.5	—	0.5		V
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—		I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33		I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	2.0	—	—	185	—	230	ns	Data to Y		
		4.5	—	19	37	—	46				
		6.0	—	—	31	—	39				
	t_{PHL}	2.0	—	—	145	—	180	ns	\overline{G}_2 to Y		
		4.5	—	14	29	—	36				
		6.0	—	—	25	—	31				
		2.0	—	—	145	—	180			ns	G_1 to Y
		4.5	—	14	29	—	36				
		6.0	—	—	25	—	31				
	t_{PHL}	2.0	—	—	190	—	240	ns	\overline{GL} to Y		
		4.5	—	21	38	—	48				
		6.0	—	—	32	—	41				
Pulse width	t_w	2.0	80	—	—	100	—	ns			
		4.5	16	8	—	20	—				
		6.0	14	—	—	17	—				
Hold time	t_h	2.0	5	—	—	5	—	ns			
		4.5	5	-4	—	5	—				
		6.0	5	—	—	5	—				
Setup time	t_{su}	2.0	75	—	—	95	—	ns			
		4.5	15	4	—	19	—				
		6.0	13	—	—	16	—				
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns			
	t_{THL}	4.5	—	5	15	—	19				
	t_{THL}	6.0	—	—	13	—	16				
Input capacitance	C_{in}	—	—	5	10	—	10	pF			

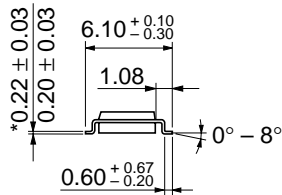


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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