

# HD74HCT74A

Dual D-type Positive Edge-triggered Flip Flops  
with Clear and Preset

# HITACHI

ADE-205-290 (Z)

1st. Edition

June 1999

## Description

The HD74HCT74A has independent data, preset, clear, and clock inputs Q and  $\bar{Q}$  outputs in a 14 pin package. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

## Features

- $V_{CC} = 4.5$  to  $5.5$  V operation
- Input terminal has protection diode

## Function Table

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>1</sup>	H <sup>1</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

H : High level

L : Low level

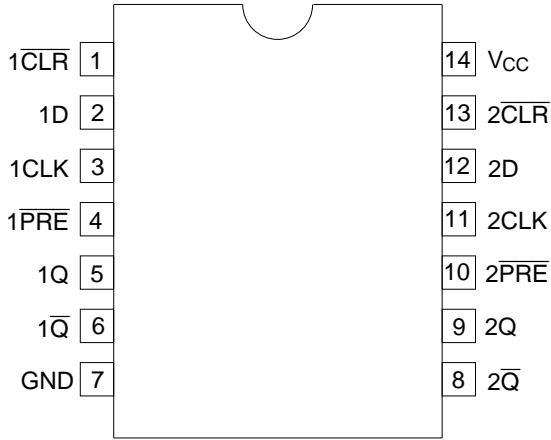
X : Immaterial

↑ : Low to high transition

Q<sub>0</sub> : Level to Q before the indicated steady state input conditions were established.

Note : 1. Q and  $\bar{Q}$  will remain high as long as preset and clear are low, but Q and  $\bar{Q}$  are unpredictable, if preset and clear go high simultaneously.

## Pin Arrangement



(Top view)

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	-0.5 to 7.0	V
Input diode peak current	$I_{IK}$	±20	mA
Output diode peak current	$I_{OK}$	±20	mA
Output current	$I_o$	±25	mA
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	±50	mA
Storage temperature	Tstg	-65 to 150	°C

**Recommended Operating Conditions**

<b>Item</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage	$V_{IH}$	2.0	—	—	V
	$V_{IL}$	0	—	0.8	
	$V_I$	0	—	$V_{CC}$	
Output voltage	$V_O$	0	—	$V_{CC}$	V
Output current	$I_{OH}$	—	-4	—	mA
	$I_{OL}$	—	4	—	
Input rise / fall time	$t_r, t_f$	—	—	500	ns
Operating temperature	$T_a$	-40	—	85	°C

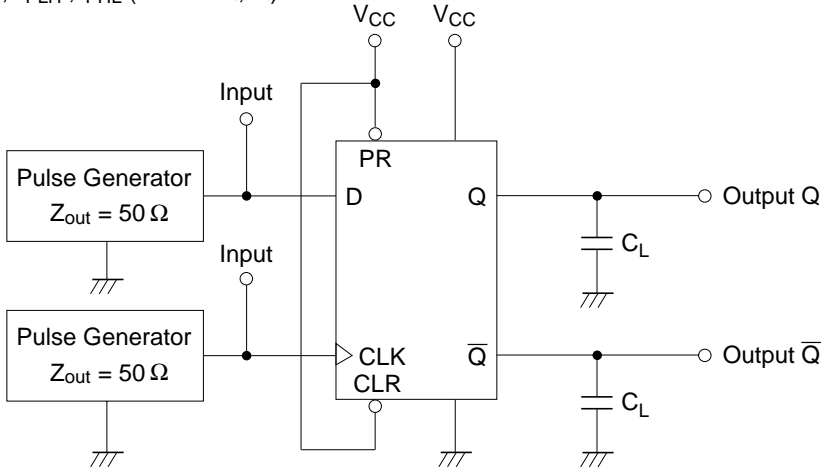


**Switching Characteristics** ( $C_L = 50$  pF)

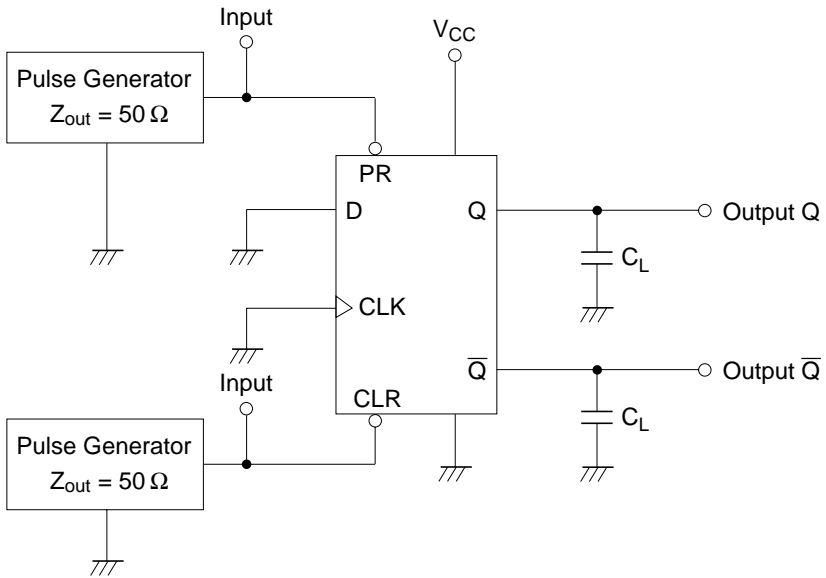
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$		Unit	Input FROM	Output TO	
			Min	Typ	Max	Min	Max				
Maximum clock frequency	$f_{max}$	4.5	27	78	—	22	—	MHz			
		5.5	30	92	—	24	—				
Propagation delay time	$t_{PLH}$	4.5	—	14	28	—	35	ns	$\overline{\text{PRE}}$ ,	Q, $\overline{\text{Q}}$	
	$t_{PHL}$	5.5	—	12	25	—	32		$\overline{\text{CLR}}$		
		4.5	—	14	22	—	28	ns	CLK	Q, $\overline{\text{Q}}$	
		5.5	—	13	20	—	25				
Output rise / fall time	$t_r / t_f$	4.5	—	7	15	—	19	ns		Each output	
		5.5	—	6	13	—	16				
Setup time	$t_{su}$	4.5	10	—	—	13	—	ns	D		
		5.5	9	—	—	12	—				
			4.5	5	—	—	5	—	ns	$\overline{\text{PRE}}$ , $\overline{\text{CLR}}$	
			5.5	5	—	—	5	—		inactive	
Hold time	$t_h$	4.5	0	—	—	0	—	ns			
		5.5	0	—	—	0	—				
Pulse width	$t_w$	4.5	15	—	—	19	—	ns			
		5.5	14	—	—	17	—				
Input capacitance	$C_I$	—	—	3	10	—	10	pF			
Power dissipation capacitance	$C_{PD}$	—	—	35	—	—	—	pF			

## Test Circuit

1)  $f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$  (CLK  $\rightarrow$  Q,  $\bar{Q}$ )

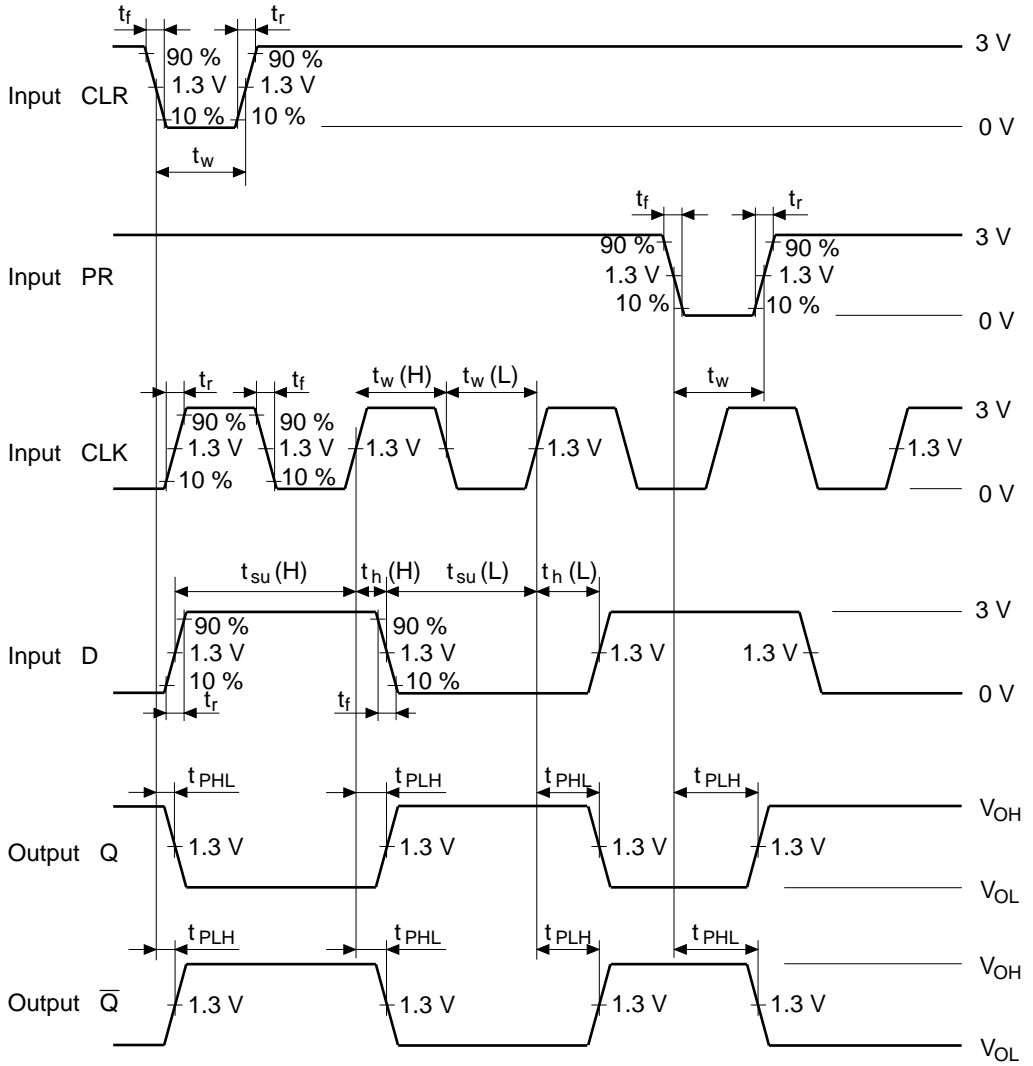


2)  $t_{PLH}$ ,  $t_{PHL}$  (CLR or PR  $\rightarrow$  Q,  $\bar{Q}$ )



Notes: 1. C<sub>L</sub> includes probe and jig capacitance.  
2. Test is put into the each flip flops.

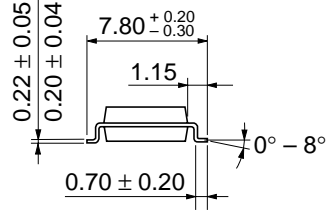
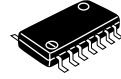
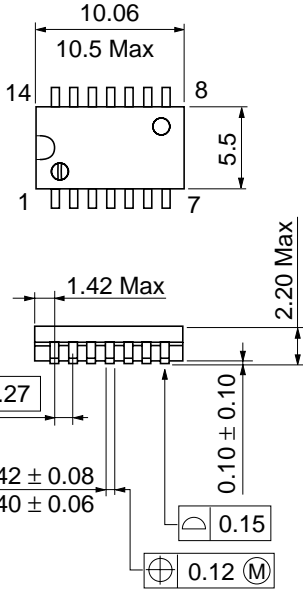
• Waveform



Note: 1. Input waveform : PRR = 1 MHz, duty cycle 50%,  $t_r = 6$  ns,  $t_f = 6$  ns

## Package Dimensions

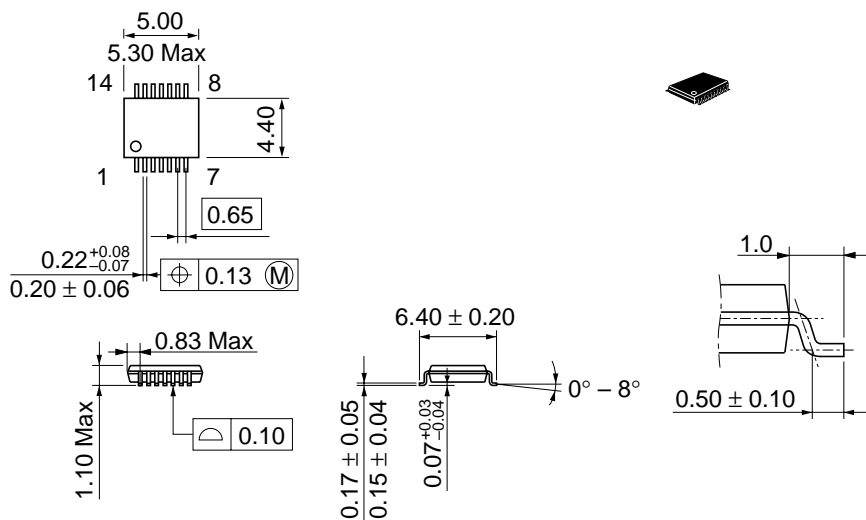
Unit : mm



Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g





Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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