512K x 8 MoBL Static RAM

Features

- **Low voltage range:**
  - **— 2.7V–3.6V**
- **Ultra low active power**
- **Low standby power**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The CY62148V is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling.

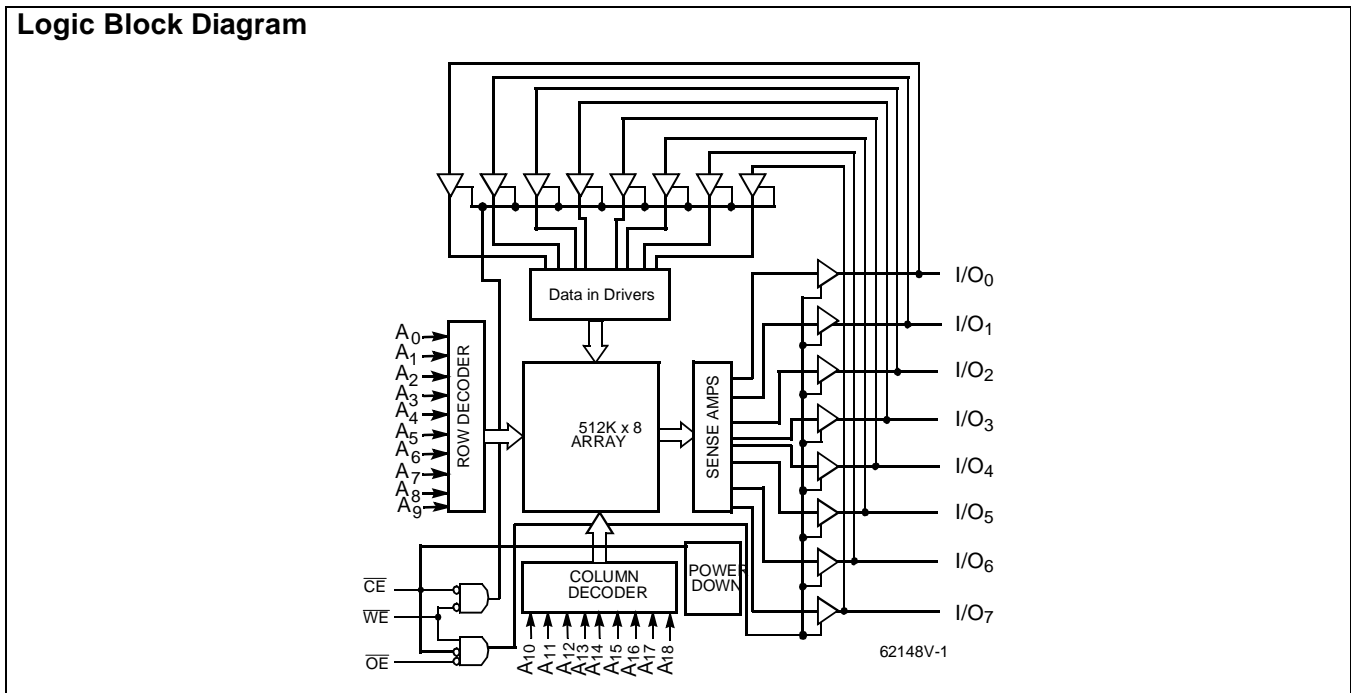The device can be put into standby mode when deselected ($\overline{CE}$ HIGH).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O$_0$ through I/O$_7$) is then written into the location specified on the address pins (A$_0$ through A$_{18}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.
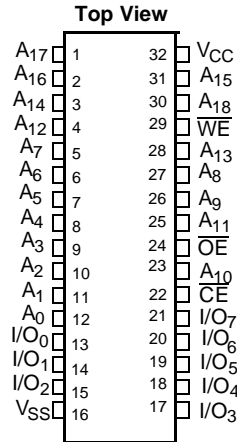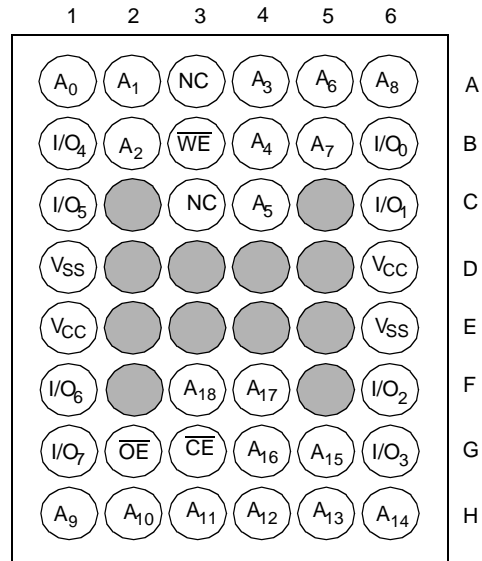
The eight input/output pins (I/O$_0$ through I/O$_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

The CY62148V is available in a 36-ball FBGA, 32 pin TSOPII, and a 32-pin SOIC package.

Logic Block Diagram

62148V-1

Pin Configurations

TSOPII/SOIC

Top View

A_{17}	1	32	V_{CC}
A_{16}	2	31	A_{15}
A_{14}	3	30	A_{18}
A_{12}	4	29	$\overline{WE}$
A_7	5	28	A_{13}
A_6	6	27	A_8
A_5	7	26	A_9
A_4	8	25	A_{11}
A_3	9	24	$\overline{OE}$
A_2	10	23	A_{10}
A_1	11	22	$\overline{CE}$
A_0	12	21	I/O_7
I/O_0	13	20	I/O_6
I/O_1	14	19	I/O_5
I/O_2	15	18	I/O_4
V_{SS}	16	17	I/O_3

FBGA
Top View

	1	2	3	4	5	6	
A	A_0	A_1	NC	A_3	A_6	A_8	A
B	I/O_4	A_2	$\overline{WE}$	A_4	A_7	I/O_0	B
C	I/O_5		NC	A_5		I/O_1	C
D	V_{SS}					V_{CC}	D
E	V_{CC}					V_{SS}	E
F	I/O_6		A_{18}	A_{17}		I/O_2	F
G	I/O_7	$\overline{OE}$	$\overline{CE}$	A_{16}	A_{15}	I/O_3	G
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	H

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Maximum Ratings

(Above which the useful life may be impaired. For user guide-
lines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied .... 55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +4.6V

DC Voltage Applied to Outputs
in High Z State[1] ....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1] .... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Industrial)			
	Min.	Typ.[2]	Max.		Operating (I_{CC})		Standby (I_{SB2})	
					Typ.[2]	Maximum	Ty.p[2]	Maximum
CY62148V	2.7V	3.0V	3.6V	70 ns	7	15 mA	2 μA	20 μA

Notes:
1. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62148V Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0$ mA	$V_{CC} = 2.7V$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA	$V_{CC} = 2.7V$			0.4	V
V_{IH}	Input HIGH Voltage		$V_{CC} = 3.6V$	2.2		$V_{CC} + 0.5V$	V
V_{IL}	Input LOW Voltage		$V_{CC} = 2.7V$	−0.5		0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−1	±1	+1	µA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		−1	±1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	$I_{OUT} = 0$ mA, (f = $f_{MAX} = 1/t_{RC}$) CMOS Levels	$V_{CC} = 3.6V$		7	15	mA
		$I_{OUT} = 0$ mA, f = 1 MHz CMOS Levels			1	2	mA
I_{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f = f_{MAX}				100	µA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f = 0	$V_{CC} = 3.6V$ L		1	50	µA
			LL		2	20	µA

Capacitance[3]

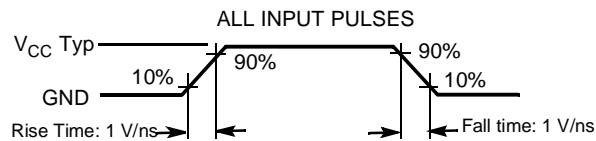| Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 3.0V$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Description	Test Conditions	Symbol	Others	BGA	Units
Thermal Resistance[3] (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ_{JA}	TBD	TBD	°C/W
Thermal Resistance[3] (Junction to Case)		Θ_{JC}	TBD	TBD	°C/W

Note:
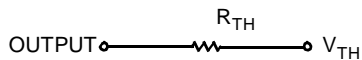3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms
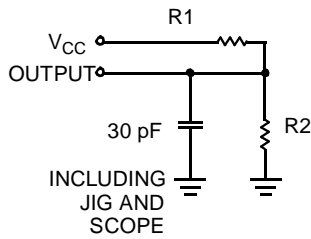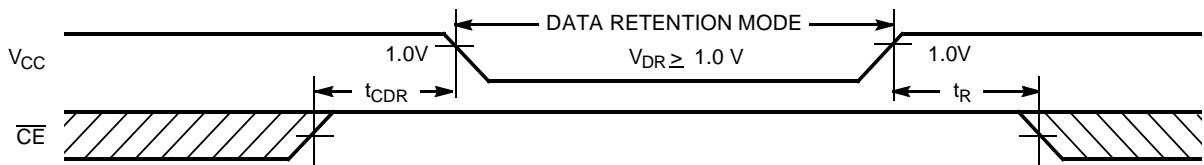

62148V–3

62148V–4

Equivalent to: THÉVENIN EQUIVALENT

Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75V	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.0		3.6	V
I_{CCDR}	Data Retention Current	V_{CC} = 1.0V $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed V_{CC}+0.3V	L/ LL		0.2	5.5	µA
							µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0			ns
t_R[4]	Operation Recovery Time			t_{RC}			ns

Note:
4. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 10\,\mu s$ or stable at $V_{CC(min.)} \geq 10\,\mu s$.

Data Retention Waveform

62148V–5

Switching Characteristics Over the Operating Range[5]

| Parameter	Description	(2.7V–3.6V Operation) Min.	Max.	Unit
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		70	ns
WRITE CYCLE[8, 9]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Set-Up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	10		ns

Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Read Cycle No. 1 [10, 11]
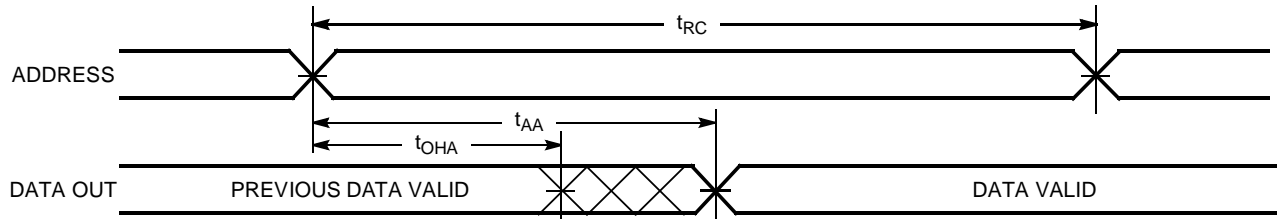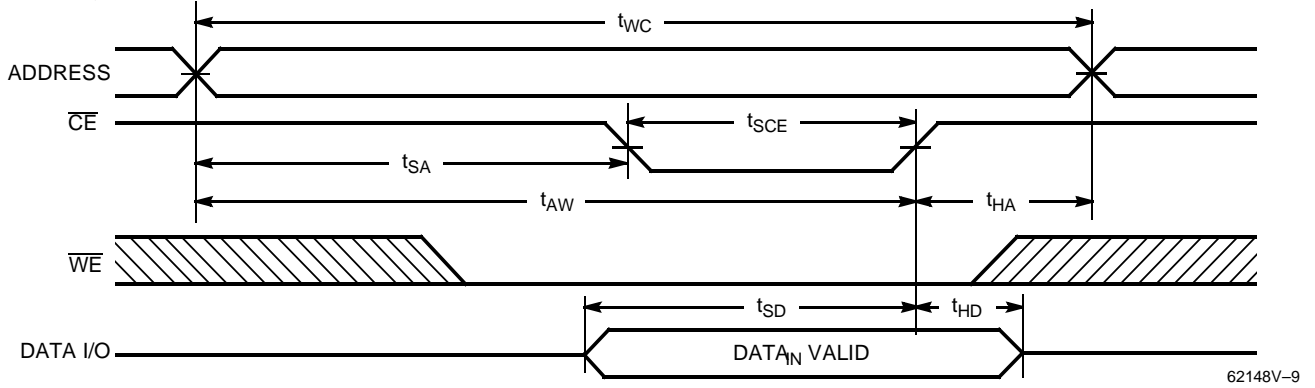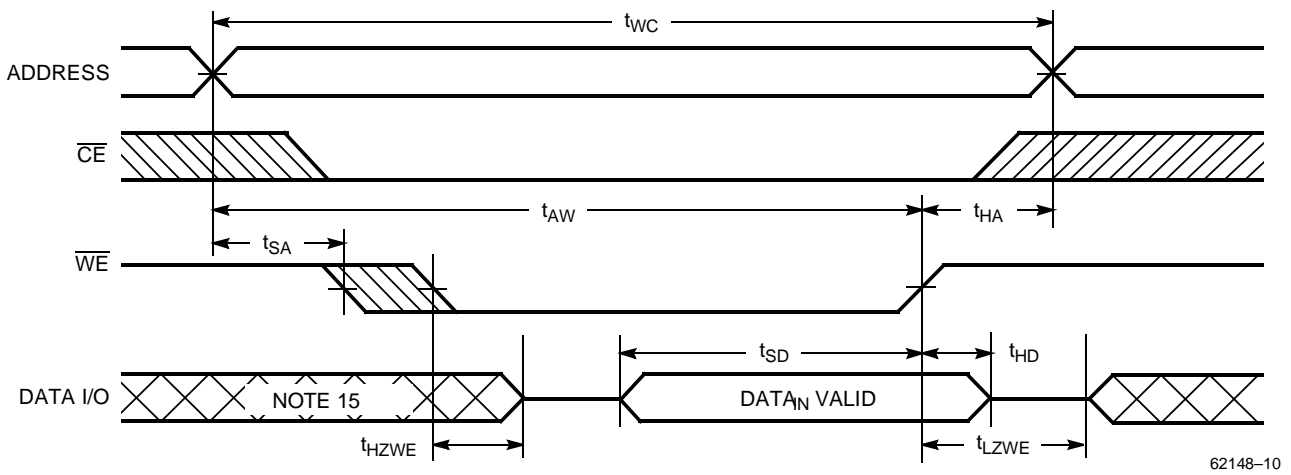

62148V–6

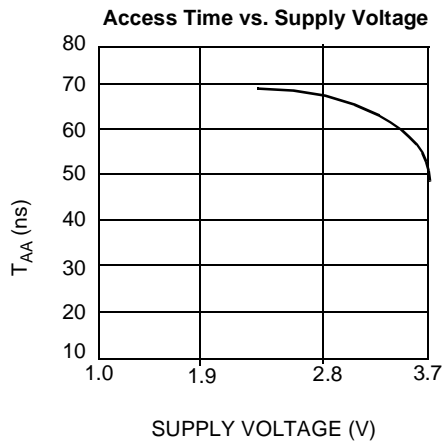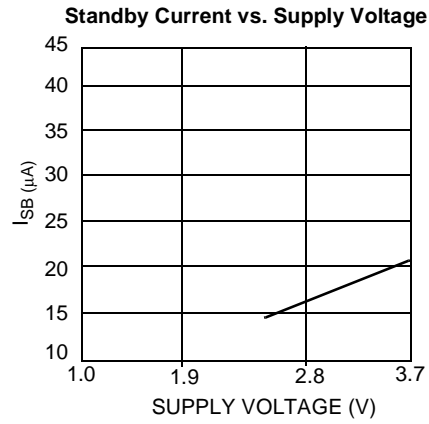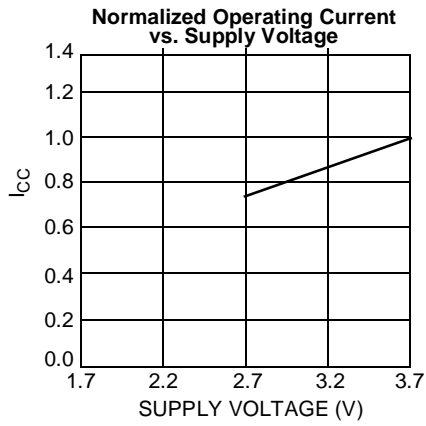### Read Cycle No. 2 [11, 12]
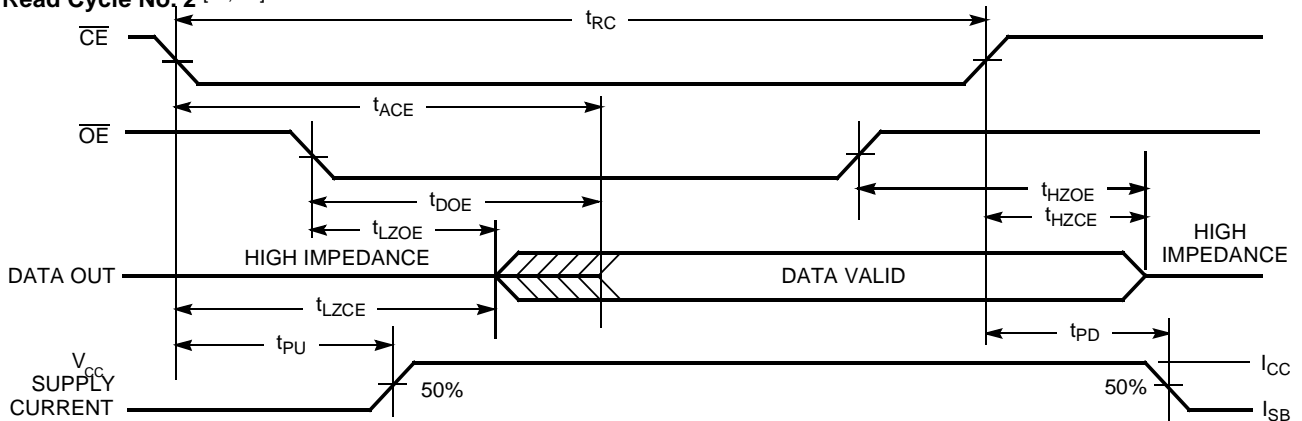
62148V–7

Write Cycle No. 1 ($\overline{WE}$ Controlled) [8, 13, 14]
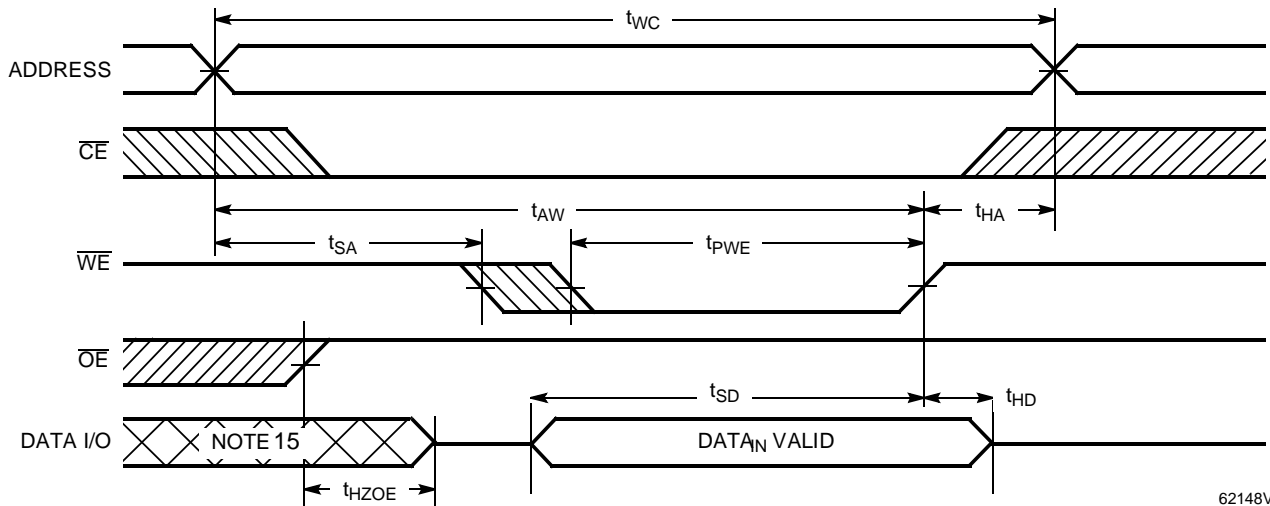
62148V–8

Notes:
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled) [8, 13, 14]

62148V–9

Write Cycle No. 3 (WE Controlled, OE LOW) [9, 14]

62148–10

Typical DC and AC Characteristics

**Normalized Operating Current
vs. Supply Voltage**

Standby Current vs. Supply Voltage

Access Time vs. Supply Voltage

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Output Disabled	Active (I_{CC})

Ordering Information

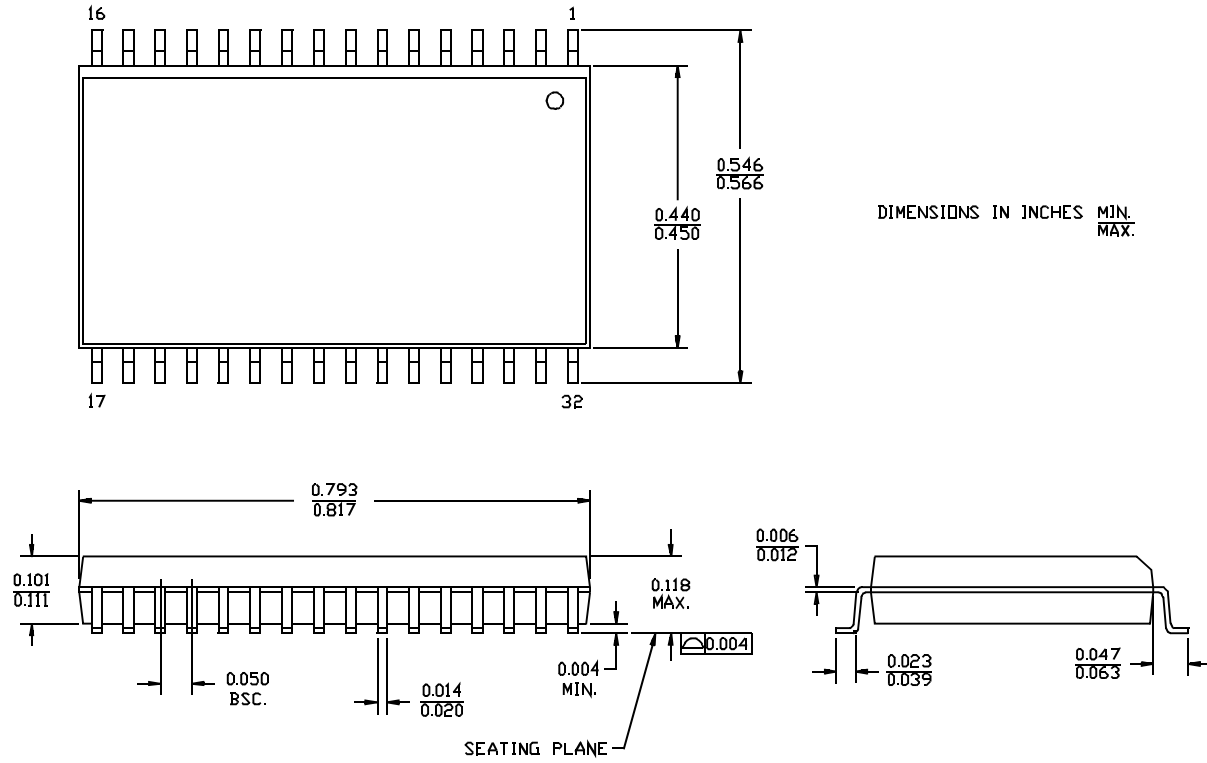| Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148VLL-70BAI	BA37	36-Ball Fine Pitch BGA	Industrial
	CY62148VLL-70ZI	ZS32	32-Lead TSOPII	
	CY62148VLL-70SI	S34	32-Lead 450 mil. molded SOIC	

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Package Diagrams

36-Ball (7.00 mm x 8.5 mm x 1.5 mm) Thin BGA BA37
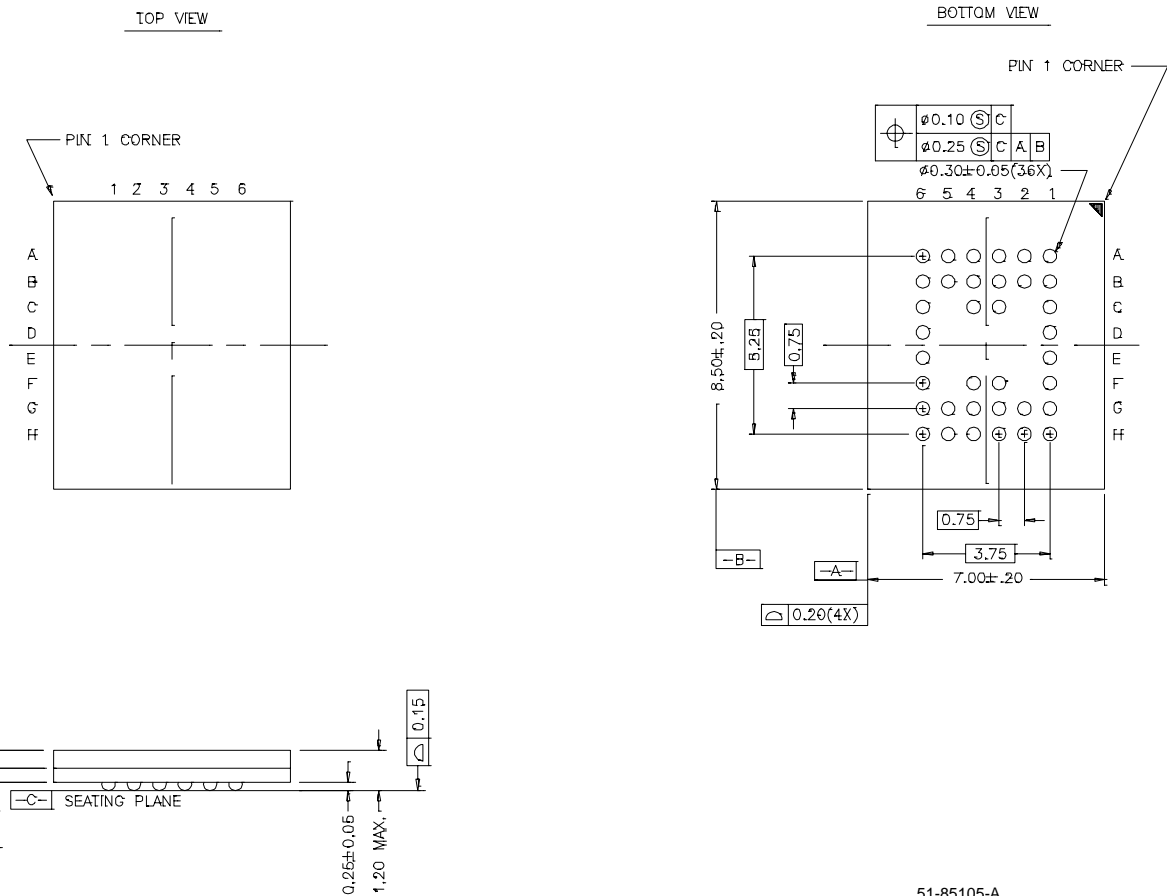
51-85105-A

* THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS
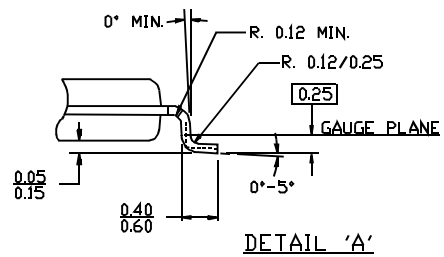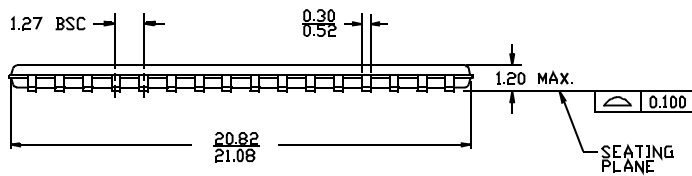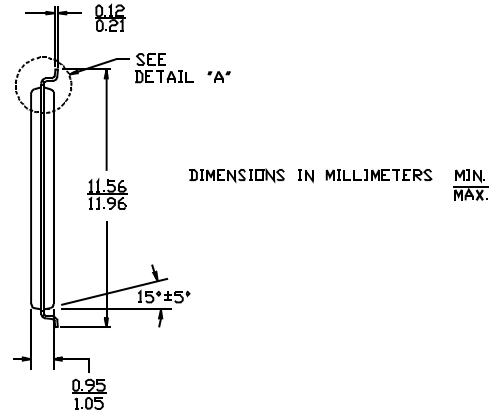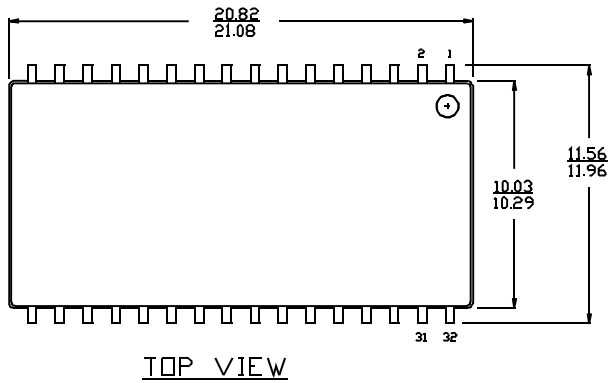ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

Package Diagrams (continued)

32-Lead (450 MIL) Molded SOIC S34

DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

Package Diagrams (continued)

32-Lead TSOP II ZS32

TOP VIEW

DIMENSIONS IN MILLIMETERS $\frac{MIN.}{MAX.}$

SEE DETAIL 'A'

SEATING PLANE

DETAIL 'A'

GAUGE PLANE

51-85095