SmartHSF™ Mobile Modem

Host-Processed, V.90/K56flex™ Modem Device Set with Host Side Device (11242), SmartDAA™ (20463), and Optional Voice Codec (20437) for PCI Bus/MiniPCI/ CardBus-Based Mobile Applications

The Conexant™ SmartHSF Host-Processed (SoftK56™) V.90/K56flex Modem Device Family with SmartDAA technology supports analog data up to 56 kbps, analog fax to 14.4 kbps, PDC high speed data, telephone answering machine (TAM), voice/speakerphone (optional), and PCI Bus/MiniPCI/CardBus host interface operation. These modem devices meet the size and power requirements of the mobile environment. Table 1 lists the available models.

The modem operates with PSTN telephone lines in the U.S./Japan/Canada and optionally world-wide, and with Japanese PDC (Personal Digital Cellular) phones. Modem and cellular data protocol software is provided.

Conexant's SmartDAA technology (patent pending) eliminates the need for a costly line transformer, relays, and opto-isolators typically used in discrete DAA (Data Access Arrangement) implementations. The SmartDAA architecture also simplifies product implementation by eliminating the need for country-specific board configurations enabling world-wide homologation of a single modem board design.

The SmartDAA system-powered DAA operates reliably without drawing power from the line, unlike line-powered DAAs which operate poorly when line current is insufficient due to long lines or poor line conditions. Enhanced features, such as monitoring of local extension status without going off-hook, are also supported.

Incorporating Conexant's proprietary Digital Isolation Barrier (DIB) design (patent pending) and other innovative DAA features, such as Digital PBX line protection and reporting, the SmartDAA architecture simplifies application design, minimizes layout area, and reduces component cost.

For over a decade, Conexant has assisted customers with DAA technology and homologation. This expertise and system level approach has been leveraged in this product.

The SmartHSF device set, consisting of a Host Side Device (HSD) in a 100-pin TQFP and a Line Side Device (LSD) (SmartDAA device) in a 32-pin TQFP, supports data/fax/TAM operation with host software-based digital signal processing and cell phone/DAA/telephone line interface functions (Figure 1). The optional Voice Codec (VC), in a 32-pin TQFP, supports voice/full-duplex speakerphone (FDSP) operation with interfaces to a microphone, speaker, and telephone handset/headset. Figure 2 identifies the major hardware signal interfaces.

Distinguishing Features

- V.90 data/V.17 fax modem
- Cellular data hardware interface and software (C models)
  - Protocol stacks for PDC high speed
  - API for customer-provided cellular data protocol stack
- SmartDAA technology
  - Digital PBX line protection
  - Caller ID detection
  - Line-in-use detection
  - Remote hang-up detection
  - Extension off-hook detection
  - Call waiting detection
- Data/Fax/Voice call discrimination
- Host software/MMX digital signal processing
- Voice/full-duplex speakerphone mode (S models)
- World-wide operation (W models)
- Industry standard communication commands
- PCI Bus/Mini-PCI or CardBus host interface
  - 32-bit PCI Local Bus compliant
  - Supports PCI Bus Power Management
- System compatibilities
  - Windows 95, Windows 95 OSR2, Windows 98, Windows NT 4.0, Windows 2000
  - Microsoft PC 98 and PC 99 compliant
- V.80 synchronous access mode
- Thin packages support low profile designs
- +3.3V operation with +5V tolerant digital inputs

Applications

- Laptop, notebook, and handheld computers
- PCI Bus/Mini-PCI embedded system boards
- PCI Bus/Mini-PCI/CardBus plug-in cards

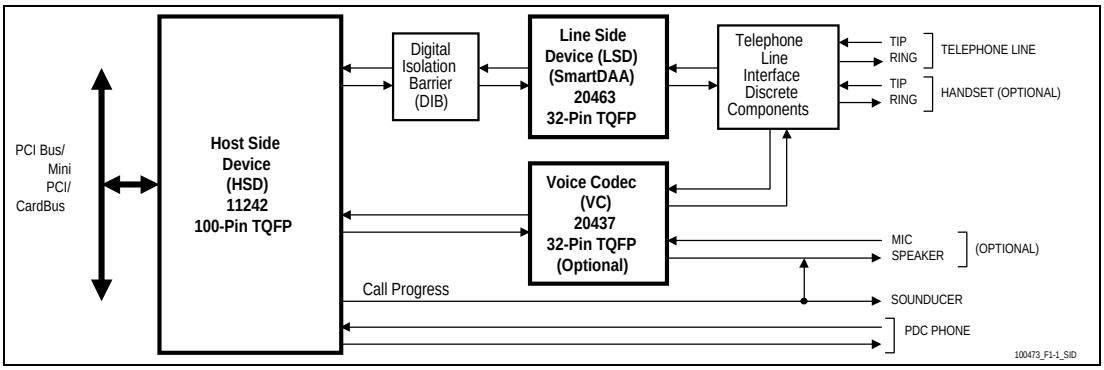

Figure 1. SmartHSF Modem Simplified Interface Diagram

Table 1. SmartHSF Modem Models and Functions

Model/Order/Part Numbers					Supported Hardware Functions (See Note 3)					
Marketing Name	Device Set Order No.	Host Side Device (HSD) [100-Pin TQFP] Part No.	Line Side Device (LSD) [32-Pin TQFP] Part No.	Voice Codec (VC) [32-Pin TQFP] Part No.	Host Bus	DAA Type	PDC	V.90/K56flex Data, V.17 Fax, TAM	World-wide	Voice/ FDSP
SmartHSF/M-PCI	DS56-L155-001	11242-11	20463-12	—	PCI	US/J/C	—	Y	—	—
SmartHSF/MS-PCI	DS56-L155-011	11242-11	20463-12	20437-11	PCI	US/J/C	—	Y	—	Y
SmartHSF/MW-PCI	DS56-L155-021	11242-11	20463-11	—	PCI	WW	—	Y	Y	—
SmartHSF/MWS-PCI	DS56-L155-031	11242-11	20463-11	20437-11	PCI	WW	—	Y	Y	Y
SmartHSF/MC-CB	DS56-L155-041	11242-21	20463-12	—	CardBus	US/J/C	Y	Y	—	—
SmartHSF/MCS-CB	DS56-L155-051	11242-21	20463-12	20437-11	CardBus	US/J/C	Y	Y	—	Y
SmartHSF/MCW-CB	DS56-L155-061	11242-21	20463-11	—	CardBus	WW	Y	Y	Y	—
SmartHSF/MCWS-CB	DS56-L155-071	11242-21	20463-11	20437-11	CardBus	WW	Y	Y	Y	Y
SmartHSF/MC-PCI	DS56-L155-081	11242-31	20463-12	—	PCI	US/J/C	Y	Y	—	—
SmartHSF/MCS-PCI	DS56-L155-091	11242-31	20463-12	20437-11	PCI	US/J/C	Y	Y	—	Y
SmartHSF/MCW-PCI	DS56-L155-100	11242-31	20463-11	—	PCI	WW	Y	Y	Y	—
SmartHSF/MCWS-PCI	DS56-L155-101	11242-31	20463-11	20437-11	PCI	WW	Y	Y	Y	Y

Notes:

1. Model options:
   - C Cellular
   - M Mobile
   - S Voice/full-duplex speakerphone (FDSP)
   - W World-wide support
   - -CB CardBus Interface
   - -PCI PCI Bus/MiniPCI interface
2. Supported functions (Y = Supported; – = Not supported):
   - TAM Telephone answering machine (Voice playback and record through telephone line)
   - FDSP Full-duplex speakerphone and voice playback and record through telephone line, handset, and mic/speaker
   - PDC Personal Digital Cellular data
3. Software configuration/functions determined by Device ID loaded into EEPROM. See SmartHSF Designer's Guide (Doc. No. 100473).

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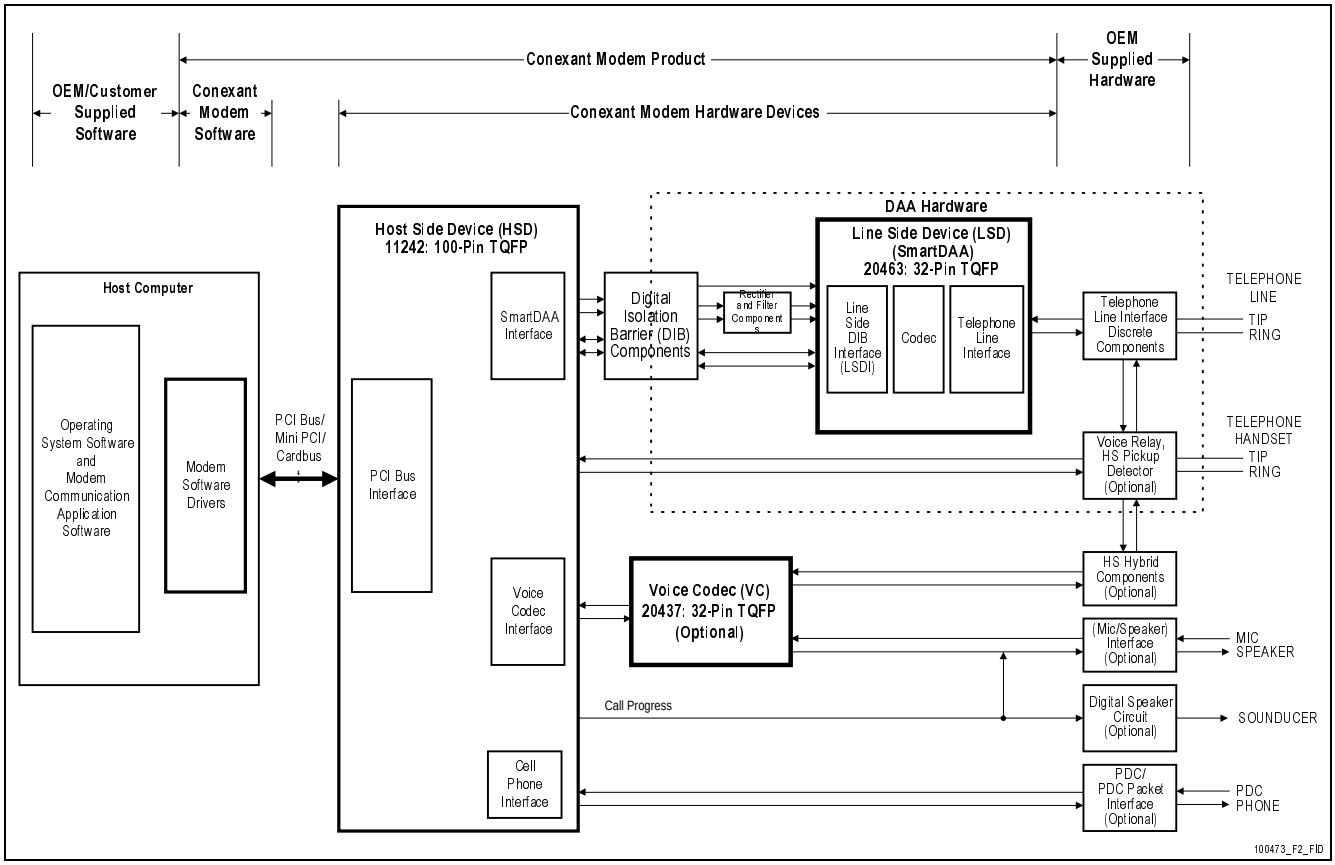


Figure 2. SmartHSF Modem Major Interfaces

Detailed Features

General Modem Features

- V.90 data modem with receive rates up to 56k bps and send rates up to V.34 rates
  - ITU-T V.90, K56flex, V.34 (33.6 kbps), V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21; Bell 212A and 103
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - V.250 (ex V.25 ter) and V.251 (ex V.25 ter Annex A) commands
- V.17 fax modem with send and receive rates up to 14.4 kbps
  - V.17, V.29, V.27 ter, and V.21 ch 2
  - EIA/TIA 578 Class 1 and T.31 Class 1.0 commands
- Cellular data hardware interface and software support (C models)
  - Protocol stacks for PDC high speed
  - API for customer-provided cellular data protocol stack
- Telephony/TAM
  - V.253 commands
  - 8-bit μ-Law/A-Law coding (G.711)
  - 8-bit/16-bit linear coding
  - 8 kHz sample rate
  - Concurrent DTMF, ring, and Caller ID detection
- V.80 synchronous access mode supports host-controlled communication protocols with H.324 interface support
- V.8/V.8bis and V.251 (ex V.25 ter Annex A) commands
- Data/Fax/Voice call discrimination
- Full-duplex Speakerphone (FDSP) Mode (S models)
  - Microphone and speaker interface
  - Telephone handset/headset interface
- Host software/MMX-based digital signal processing
- Single configuration profile stored in host
- Operates in US/Japan/Canada
- World-wide operation (W models)
  - Complies to TBR21 and other country requirements
  - Caller ID detection
- System compatibilities
  - Windows 95, Windows 95 OSR2, Windows 98, Windows NT 4.0, Windows 2000 operating systems
  - Microsoft's PC 98 and PC 99 Design Initiative compliant
  - Advanced Configuration and Power Interface (ACPI)
  - Unimodem/V compliant
  - Pentium 166 MHz MMX-compatible PC or greater
  - 16 Mbyte RAM or more
- Thin packages support low profile designs
  - HSD (11242): 100-pin TQFP (1.2 mm max. height)
  - LSD (20463): 32-pin TQFP (1.6 mm max. height)
  - VC (20437): 32-pin TQFP (1.6 mm max. height)
- +3.3V operation with +5V tolerant digital inputs

PCI Bus Host Interface Features

- 32-bit PCI Bus host interface
  - Meets PCI Local Bus Specification Rev. 2.2
  - PCI Bus Mastering interface
  - 33 MHz PCI clock support
- Supports Power Management
  - Meets PCI Bus Power Management Spec. Rev. 1.1
  - ACPI Power Management Registers
  - APM support
  - PME# support
  - Vaux/Vpci power switching support (-PCI model option)
  - VauxDET support

SmartDAA Features

- Digital PBX line protection
- System side powered DAA operates under poor line current supply conditions
- Wake-on-ring
- Ring detection
- Line polarity reversal detection
- Line current loss detection
- Caller ID (CID) detection
- Pulse dialing
- Line-in-use detection – detects even while on-hook
- Remote hang-up detect – for efficient call termination
- Extension pickup detect
- Call waiting detection
- Meets world-wide DC VI Masks requirements (W models)

Description

General

Modem operation, including dialing, call progress, telephone line interface, telephone handset interface, PDC High Speed interface, voice/speakerphone interface, and host interface functions are supported and controlled through the V.250, V.251, and V.253-compatible command set.

The modem hardware connects to the host processor via a PCI/MiniPCI/CardBus bus interface. The OEM adds a crystal circuit, EEPROM, DIB and LSD power rectifier and filter components, telephone line interface, optional telephone handset interface, optional PDC high speed interface, optional voice/speakerphone interface, and other supporting discrete components as required by the modem model (Table 1) and the application to complete the system.

Host Modem Software

The host modem software performs the following tasks:

1. General modem control, which includes command sets, fax Class 1, TAM, voice/speakerphone, error correction, data compression, PDC high speed data protocol stacks and phone drivers, and operating system interface functions.

2. Modem data pump signal processing, which includes data and facsimile modulation and demodulation, as well as voice sample formatting, is performed by the host processor using Conexant SoftK56 technology.
3. SmartDAA control, which includes HSD SmartDAA Interface control, LSD configuration and control, telephone line interface parameter control, and telephone line impedance control.

Configurations of the modem software are provided to support modem models listed in Table 1.

Data/Fax Modes

In V.90/K56flex data modem mode, the modem can receive data from a digital source using a V.90- or K56flex-compatible central site modem at line speeds up to 56 kbps. Asymmetrical data transmission supports sending data at line speeds up to V.34 rates. This mode can fallback to full-duplex V.34 mode, and to lower rates, as dictated by line conditions.

In V.34 data modem mode, the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33.6 kbps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps down to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported.

In V.32 bis data modem mode, the modem can operate at line speeds up to 14.4 kbps.

In fax modem mode, the modem can operate in 2-wire, half-duplex, synchronous modes and can support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax data transmission and reception performed by the modem are controlled and monitored through the EIA/TIA-578 Class 1 or T.31 Class 1.0 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

Synchronous Access Mode (SAM) - Video Conferencing

V.80 Synchronous Access Mode between the modem and the host/DTE is provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

TAM Mode

TAM Mode features include 8-bit μ-Law, A-Law, and linear coding at 8 kHz sample rate. Full-duplex voice supports concurrent voice receive and transmit. Tone detection/generation, call discrimination, and concurrent DTMF detection are also supported. This mode supports applications such as digital TAM, voice annotation, and recording from and playback to the telephone line. ADPCM (4-bit IMA) coding is also supported to meet Microsoft WHQL logo requirements.

TAM Mode is supported by three submodes:

1. Online Voice Command Mode supports connection to the telephone line or, for S models, a microphone/speaker/handset/headset.
2. Voice Receive Mode supports recording voice or audio data input from the telephone line or, for S models, a microphone/handset/headset.
3. Voice Transmit Mode supports playback of voice or audio data to the telephone line or, for S models, a speaker/handset/headset.

Voice/Speakerphone Mode (S Models)

The S models include additional telephone handset, external microphone, and external speaker interfaces which support voice and full-duplex speakerphone (FDSP) operation.

Hands-free full-duplex telephone operation is supported in Speakerphone Mode under host control. Speakerphone Mode features an advanced proprietary speakerphone algorithm which supports full-duplex voice conversation with acoustic, line, and handset echo cancellation. Parameters are constantly adjusted to maintain stability with automatic fallback from full-duplex to pseudo-duplex operation. The speakerphone algorithm allows position independent placement of microphone and speaker. The host can separately control volume, muting, and AGC in microphone and speaker channels.

Personal Digital Cellular (PDC) High Speed Mode (C Models)

PDC High Speed Mode, implemented in host software, includes V.42 bis data compression and ARQ framing. A pass-through mode is also available to allow a phone book to be transferred to and from the PC at speeds up to 9600 bps (e.g., for editing on the PC). PDC High Speed Mode is enabled by +WS46=20 and disabled by +WS46=1.

Reference Design

A MiniPCI Type IIIB data/fax/TAM reference design board is available to minimize application design time and costs.

The board is pretested to pass FCC Part 15, Part 68, and CTR 21 for immediate manufacturing.

A design package for the board is available in electronic form. The design package includes schematics, bill of materials (BOM), vendor parts list (VPL), board layout files in Gerber format, and complete documentation.

The design can also be used for the basis of a custom design by the OEM to accelerate design completion for rapid market entry.

Additional Information

Additional information is described in the SmartHSF Modem Device Family for Mobile Applications Designer's Guide (Doc. No. 100473, formerly identified as Doc. No. 1221) and the Command Reference Manual (Doc. No. 100498, formerly identified as Doc. No. 1118).

Hardware Description

SmartDAA™ technology (patent pending) eliminates the need for a costly analog transformer, relays, and opto-isolators that are typically used in discrete DAA implementations. The programmable SmartDAA architecture simplifies product implementation in world-wide markets by eliminating the need for country-specific components.

Host Side Device (HSD)

The HSD, packaged in a 100-pin TQFP, includes a PCI/MiniPCI/CardBus Interface and a SmartDAA Interface.

The PCI/MiniPCI/CardBus interface connects directly to an embedded or external PCI/MiniPCI/CardBus interface eliminating the need for additional external logic components.

The SmartDAA Interface communicates with, and supplies power and clock to, the LSD through the DIB.

Digital Isolation Barrier (DIB) (OEM Supplied)

The DIB electrically DC isolates the HSD from the LSD and telephone line. The HSD is connected to a fixed digital ground and operates with standard CMOS logic levels. The LSD is connected to a floating ground and can tolerate high voltage input (compatible with telephone line and typical surge requirements).

The DIB power and clock transformer (PCXFMR) couples power and clock from the HSD to the LSD.

The DIB data channel supports bidirectional half-duplex serial transfer of data, control, and status information between the HSD and the LSD.

SmartDAA Line Side Device (LSD)

The LSD includes a Line Side DIB Interface (LSDI), a coder/decoder (codec), and a Telephone Line Interface (TLI).

The LSDI communicates with, and receives power and clock from, the SmartDAA interface in the HSD through the DIB.

LSD power is received from the DIB PCXFMR secondary winding through a half-wave rectifying diode and capacitive power filter circuit. The CLK input is also accepted from the PCXFMR secondary winding through a capacitor and a resistor in series.

Information is transferred between the LSD and the HSD through the DIB_P and DIB_N pins. These pins connect to the HSD DIB_DATAP and DIB_DATAN pins, respectively, through the DIB.

The TLI integrates DAA and direct telephone line interface functions and connects directly to the line TIP and RING pins, as well as to external line protection components.

Direct LSD connection to TIP and RING allows real-time measurement of telephone line parameters, such as the telephone central office (CO) battery voltage, individual telephone line (copper wire) resistance, and allows dynamic regulation of the off-hook TIP and RING voltage and total current drawn from the central office (CO). This allows the modem to maintain compliance with U.S. and world-wide regulations and to actively control the DAA power dissipation.

Voice Codec (VC) (S Models)

The optional VC, packaged in a 32-pin TQFP, supports voice/full-duplex speakerphone (FDSP) operation with interfaces to a microphone and speaker and to a telephone handset/headset.

HSD (11242) Hardware Pins and Signals

General

PCI Bus/MiniPCI/CardBus Host Interface

The Host Side Device conforms to the PCI Local Bus Specification Version 2.2, MiniPCI Specification Draft 1.0, and PC Card Standard for CardBus. It is a memory slave and a bus master for PC host memory accesses (burst transactions). Configuration is by PCI configuration protocol.

The PCI Bus/MiniPCI/CardBus interface signals are:

- Address and data
  - 32 bidirectional Address/Data (AD[31-0]); bidirectional
  - 4 Bus Command and Byte Enable (CBE [3:0]); bidirectional
  - Bidirectional Parity (PAR); bidirectional
- Interface control
  - Cycle Frame (FRAME#); bidirectional
  - Initiator Ready (IRDY#); bidirectional
  - Target Ready (TRDY#); bidirectional
  - Stop (STOP#); bidirectional
  - Initialization Device Select (IDSEL); input
  - Device Select (DEVSEL#); bidirectional
- Arbitration
  - Request (REQ#); output
  - Grant (GRANT#); input
- Error reporting
  - Parity Error (PERR#); bidirectional
  - System Error (SERR#); bidirectional
- Interrupt
  - Interrupt A (INTA#); output
- System
  - Clock (PCICLK); input
  - Reset (PCIRST#); input
  - Clock Running (CLKRUN#); input
  - Power Management Event (PME#), output (-PCI model)
  - Status Change (STSCHG#), output (-CB model)

Power Detection and Switching

- Vaux Enable (VauxEN#); output (-PCI model)
- Vpci Enable (VpciEN#); output (-PCI model)
- Vpci Detect (VpciDET); input
- Vaux Detect (VauxDET); input

Serial EEPROM Interface

A serial EEPROM is required to store the Device ID, Vendor ID, Subsystem ID, Subsystem Vendor ID, and Power Management parameters for the PCI Configuration Space Header. The EEPROM is also required to store the CIS table for CardBus designs.

The EEPROM must be 2048 (128 x 16) bits or larger for PCI Bus/MiniPCI applications or 4096 (256 x 16) bits or larger for CardBus applications, and be rated at 1MHz (SROMCLK is 537.6 kHz). For example, the following EEPROMs or equivalent may be used: Microchip 93LC66B (256 x 16), 93LC56B (128 x 16), Atmel AT93C66 (256 x 16), AT93C56 (128 x 16). The EEPROM is programmable by the PC via the modem.

The EEPROM interface signals are:

- Serial Data Input (SROMIN); input
- Serial Data Output (SROMOUT); output
- Clock (SROMCLK); output
- Chip Select (SROMCS); output

LSD Interface (Through DIB)

The DIB interface signals are:

- Clock and Power Positive (PWRCLKP); output
- Clock and Power Negative (PWRCLKN); output
- Data Positive (DIB_DATAP); input/output
- Data Negative (DIB_DATAN); input/output

VC Interface (S Models)

The VC interface signals are:

- Modem Sleep (IASLEEP); output
- Master Clock (M_CLK); output
- Voice Serial Clock (V_SCLK); input
- Voice Serial Control (V_CTRL); output
- Voice Serial Frame Sync (V_STROBE); input
- Voice Serial Transmit Data (V_TXSIN); output
- Voice Serial Receive Data (V_RXOUT); input

Telephone Handset Interface (S Models)

The telephone handset interface signals are:

- Voice Relay Control (VOICE#); output
- Handset Pickup Detect (H_PICKUP); input

Call Progress Speaker Interface

The call progress speaker interface signal is:

- Digital speaker output (DSPKOUT); output

DSPKOUT is a square wave output in Data/Fax mode used for call progress or carrier monitoring. This output can be optionally connected to a low-cost on-board speaker, e.g., a sounducer, or to an analog speaker circuit.

PDC Interface

Seven lines are available to support the PDC cellular phone interface. Specific signal assignments depend upon the installed cell phone driver.

HSD Interface Signals and Pin Assignments

The HSD (11242) 100-pin TQFP hardware interface signals are shown by major interface in Figure 3, are shown by pin number in Figure 4, and are listed by pin number in Table 2.

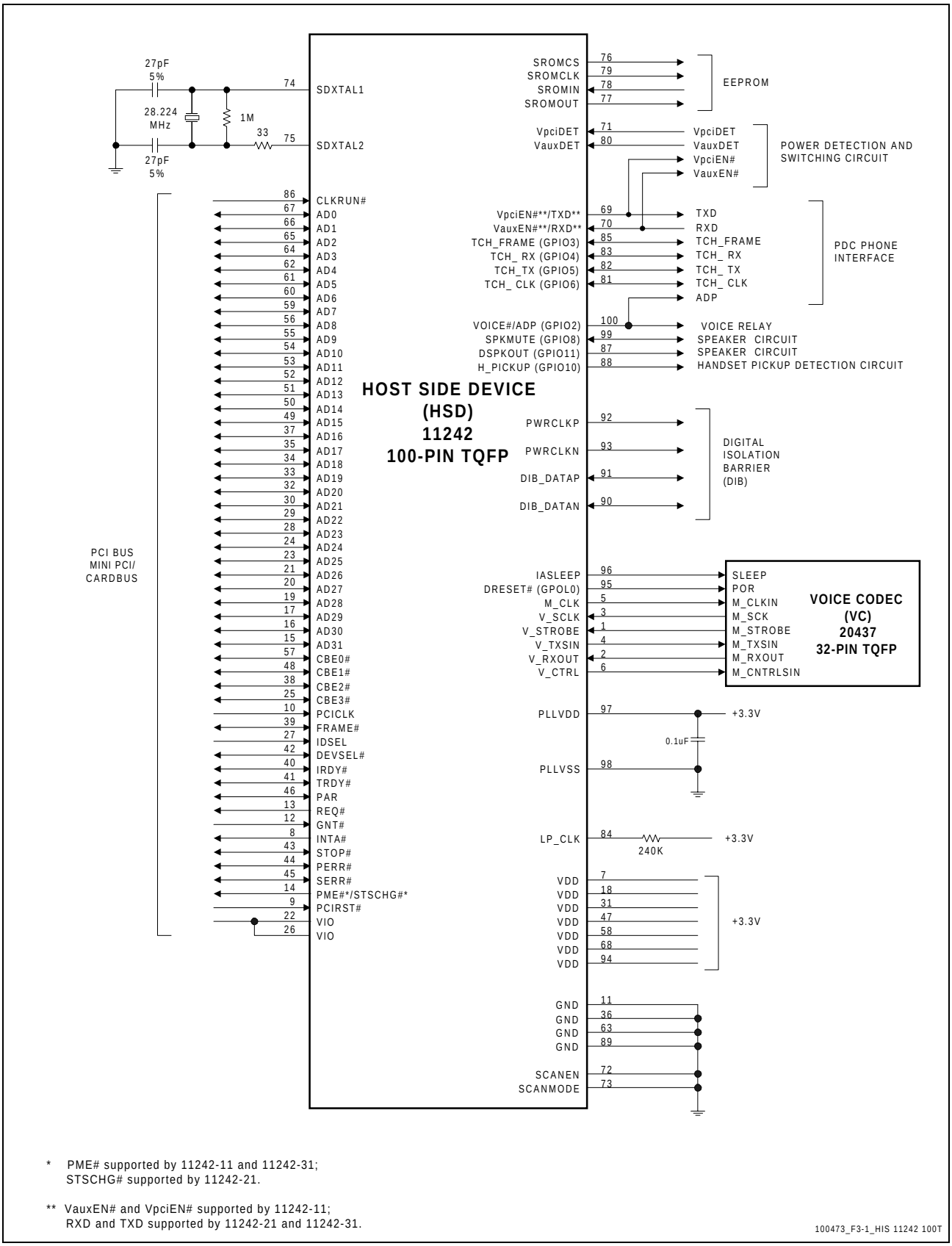


Figure 3. HSD (11242) 100-Pin TQFP Hardware Interface Signals

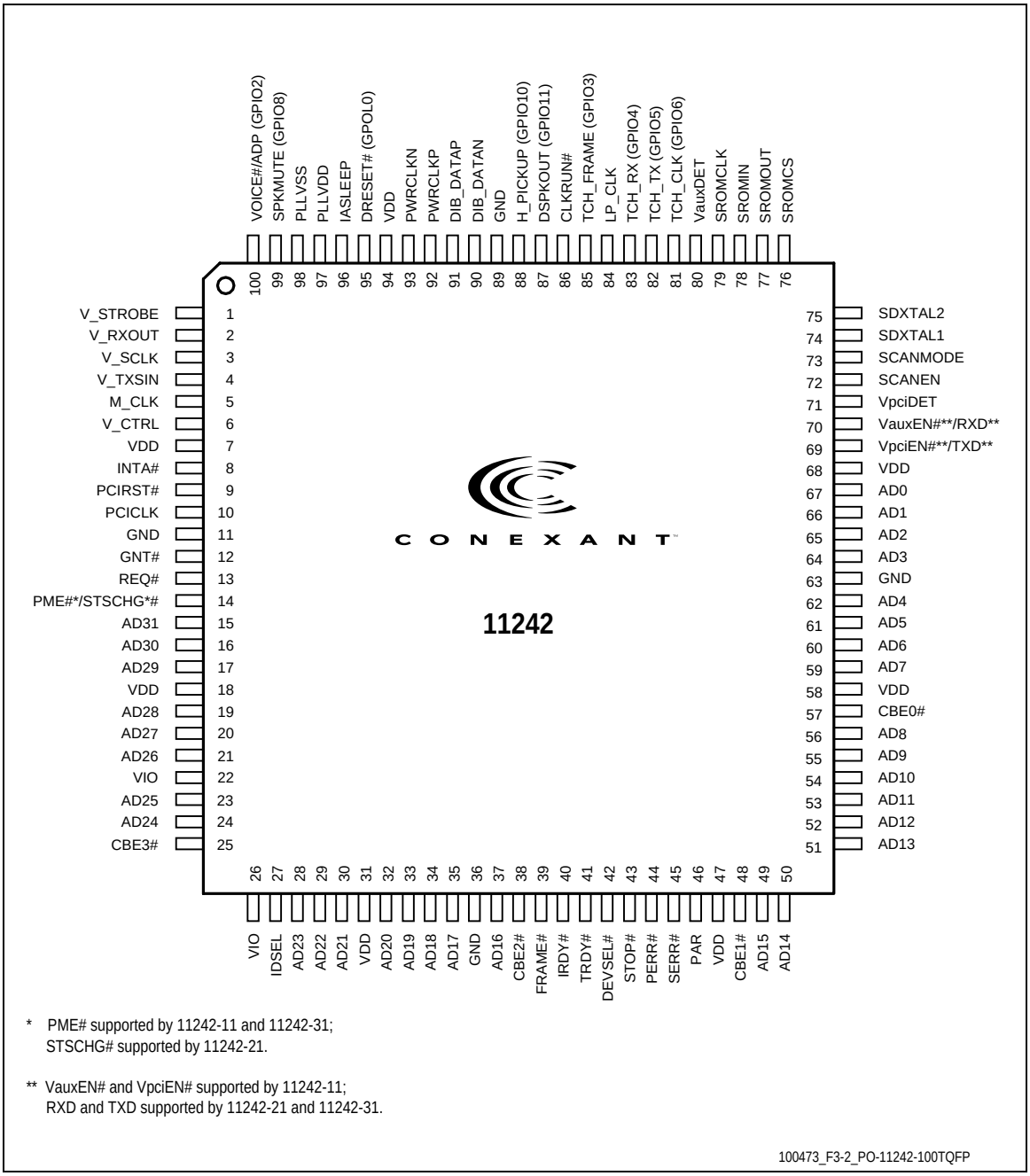


Figure 4. HSD (11242) 100-Pin TQFP Pin Signals

Table 2. HSD (11242) 100-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	V_STROBE	Itpd	VC: M_STROBE	51	AD13	I/Opts	PCI Bus: AD13
2	V_RXOUT	Itk	VC: M_RXOUT	52	AD12	I/Opts	PCI Bus: AD12
3	V_SCLK	Itpd	VC: M_SCK	53	AD11	I/Opts	PCI Bus: AD11
4	V_TXSIN	Ot2	VC: M_TXSIN	54	AD10	I/Opts	PCI Bus: AD10
5	M_CLK	Ot2	VC: M_CLKIN	55	AD9	I/Opts	PCI Bus: AD9
6	V_CTRL	Ot2	VC: M_CNTRLSIN	56	AD8	I/Opts	PCI Bus: AD8
7	VDD	PWR	+3.3V	57	CBE0#	I/Opts	PCI Bus: CBE0#
8	INTA#	Opod	PCI Bus: INTA#	58	VDD	PWR	+3.3V
9	PCIRST#	Ip	PCI Bus: PCIRST#	59	AD7	I/Opts	PCI Bus: AD7
10	PCICLK	Ip	PCI Bus: PCICLK	60	AD6	I/Opts	PCI Bus: AD6
11	GND	GND	GND	61	AD5	I/Opts	PCI Bus: AD5
12	GNT#	Ipts	PCI Bus: GNT#	62	AD4	I/Opts	PCI Bus: AD4
13	REQ#	Opts	PCI Bus: REQ#	63	GND	GND	GND
14	PME#/STSCHG#	Opod	PCI Bus: PME# CardBus: STSCHG# (See Note 3)	64	AD3	I/Opts	PCI Bus: AD3
15	AD31	I/Opts	PCI Bus: AD31	65	AD2	I/Opts	PCI Bus: AD2
16	AD30	I/Opts	PCI Bus: AD30	66	AD1	I/Opts	PCI Bus: AD1
17	AD29	I/Opts	PCI Bus: AD29	67	AD0	I/Opts	PCI Bus: AD0
18	VDD	PWR	+3.3V	68	VDD	PWR	+3.3V
19	AD28	I/Opts	PCI Bus: AD28	69	VpciEN#/TXD	Ot2	PCI Bus: Pwr Detection/Switching Ckt Cell Phone: TXD (See Note 4)
20	AD27	I/Opts	PCI Bus: AD27	70	VauxEN#/RXD	Ot2	PCI Bus: Pwr Detection/Switching Ckt Cell Phone: RXD (See Note 4)
21	AD26	I/Opts	PCI Bus: AD26	71	VpciDET	Itpd	Pwr Detection/Switching Ckt
22	VIO	PWR	PCI Bus: VI/O	72	SCANEN	Itpd	GND
23	AD25	I/Opts	PCI Bus: AD25	73	SCANMODE	Itpd	GND
24	AD24	I/Opts	PCI Bus: AD24	74	SDXTAL1	Ix	Crystal or Clock Circuit
25	CBE3#	I/Opts	PCI Bus: CBE3#	75	SDXTAL2	Ox	Crystal or NC (if SDXTAL1 connected to Clock Circuit)
26	VIO	PWR	PCI Bus: VI/O	76	SROMCS	Ot2	SROM: Chip Select (CS)
27	IDSEL	Ip	PCI Bus: IDSEL	77	SROMOUT	Ot2	SROM: Data In (DI)
28	AD23	I/Opts	PCI Bus: AD23	78	SROMIN	Itpu	SROM: Data Out (DO)
29	AD22	I/Opts	PCI Bus: AD22	79	SROMCLK	Ot2	SROM: Clock (SK)
30	AD21	I/Opts	PCI Bus: AD21	80	VauxDET	Itpd	Pwr Detection/Switching Ckt
31	VDD	PWR	+3.3V	81	TCH_CLK (GPIO6)	Itpu/Ot12	Cell Phone: TCH_CLK/CEL_CLK
32	AD20	I/Opts	PCI Bus: AD20	82	TCH_TX (GPIO5)	Itpu/Ot12	Cell Phone: TCH_TX/CEL_DATA
33	AD19	I/Opts	PCI Bus: AD19	83	TCH_RX (GPIO4)	Itpu/Ot12	Cell Phone: TCH_RX/CEL_BSY_IN
34	AD18	I/Opts	PCI Bus: AD18	84	LP_CLK	RC	+3.3V through 240 KΩ
35	AD17	I/Opts	PCI Bus: AD17	85	TCH_FRAME (GPIO3)	Itpu/Ot12	Cell Phone: TCH_FRAME/CEL_BSY_OUT
36	GND	GND	GND	86	CLKRUN#	I/Opod	PCI Bus: CLKRUN#
37	AD16	I/Opts	PCI Bus: AD16	87	DSPKOUT (GPIO11)	Ot12	AI: Digital/analog speaker circuit for call progress.
38	CBE2#	I/Opts	PCI Bus: CBE2#	88	H_PICKUP (GPIO10)	Itpu	Line Interface: Handset Pickup Detection Circuit
39	FRAME#	I/Opsts	PCI Bus: FRAME#	89	GND	GND	GND
40	IRDY#	I/Opsts	PCI Bus: IRDY#	90	DIB_DATAN	Idd/Odd	DIB: Data Negative Channel
41	TRDY#	I/Opsts	PCI Bus: TRDY#	91	DIB_DATAP	Idd/Odd	DIB: Data Positive Channel
42	DEVSEL#	I/Opsts	PCI Bus: DEVSEL#	92	PWRCLKP	Odpc	DIB: PCXFMR primary winding top
43	STOP#	I/Opsts	PCI Bus: STOP#	93	PWRCLKN	Odpc	DIB: PCXFMR primary winding bottom
44	PERR#	I/Opsts	PCI Bus: PERR#	94	VDD	PWR	+3.3V
45	SERR#	I/Opod	PCI Bus: SERR#	95	DRESET# (GPOL0)	Ot2	VC: POR
46	PAR	I/Opts	PCI Bus: PAR	96	IASLEEP	Ot2	VC: SLEEP
47	VDD	PWR	+3.3V	97	PLLVDD	PWR	+3.3V and to GND through 0.1 µF
48	CBE1#	I/Opts	PCI Bus: CBE1#	98	PLLVSS	GND	GND
49	AD15	I/Opts	PCI Bus: AD15	99	SPKMUTE (GPIO8)	It/Ot12	Audio Circuit: Spkr Control (output); Vaux Mode Power Select (input)
50	AD14	I/Opts	PCI Bus: AD14	100	VOICE# (GPIO2)	Ot12	Line Interface: Voice Relay Control

Table 2. HSD (11242) 100-Pin TQFP Pin Signals (Cont'd)

Notes:

1. I/O Types

I/Opod	Digital input/output, PCI, open drain (PCI type = o/d)
I/Opsts	Digital input/output, PCI, sustained tristate (PCI type = s/t/s)
I/Opts	Digital input/output, PCI, tristate (PCI type = t/s)
Idd	input, DIB, data channel
Ip	Digital input, PCI, totem pole (PCI type = in)
Ipts	Digital input, PCI, (PCI type = t/s)
It	Digital input, TTL-compatible
Itk	Digital input, TTL-compatible, internal keeper
Itpd	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-up
It/Ot2	Digital input, TTL-compatible/digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
It/Ot12	Digital input, TTL-compatible/digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Ix	Crystal/clock input
Odpc	Output, DIB power and clock channel
Odd	Output, DIB data channel
Ood	Digital output, open drain
Opod	Digital output, PCI, open drain (PCI type =o/d)
Opts	Digital output, PCI, tristate (PCI type = t/s)
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Ox	Crystal output

2. Interface Legend:
   - NC No internal pin connection
   - DIB Digital Isolation Barrier
   - VC Voice Codec
3. PME#/STSCHG# pin:
   - PME# supported by 11242-11 and 11242-31;
   - STSCHG# supported by 11242-21.
4. VauxEN#/RXD and VpciEN#/TXD pins:
   - VauxEN# and VpciEN# supported by 11242-11;
   - RXD and TXD supported by 11242-21 and 11242-31.
5. All references to PCI Bus also apply to MiniPCI and CardBus unless otherwise specified.

SmartDAA LSD (20463) Hardware Pins and Signals

General

HSD Interface (Through DIB)

The DIB interface signals are:

- Clock (CLK); input
- Digital Power (PWR+); input power
- Digital Ground (DGND); digital ground
- Data Positive (DIB_P); input
- Data Negative (DIB_N); input

Telephone Line Interface

The telephone line interface signals are:

- RING AC Coupled (RAC1); input
- TIP AC Coupled (TAC1); input
- Electronic Inductor Resistor (EIR); output
- TIP and RING DC Measurement (TRDC); input
- DAC Output Voltage (DAC); output
- Electronic Inductor Capacitor (EIC)
- Electronic Inductor Output (EIO)
- Electronic Inductor Feedback (EIF)
- Resistive Divider Midpoint (DCF)
- Transmit Analog Output (TXA); output
- Receive Analog Input (RXI); input
- Receiver Gain (RXG); output
- MOV Enable (MOVEN); output
- World-wide Impedance 0 (ZW0); input
- US Impedance 0 (ZUS0); input
- Transmit Feedback (TXF); input
- Transmit Output (TXO); output

LSD Interface Signals and Pin Assignments

The LSD (20463) 32-pin TQFP hardware interface signals are shown by major interface in Figure 5, are shown by pin number in Figure 6, and are listed by pin number in Table 3.

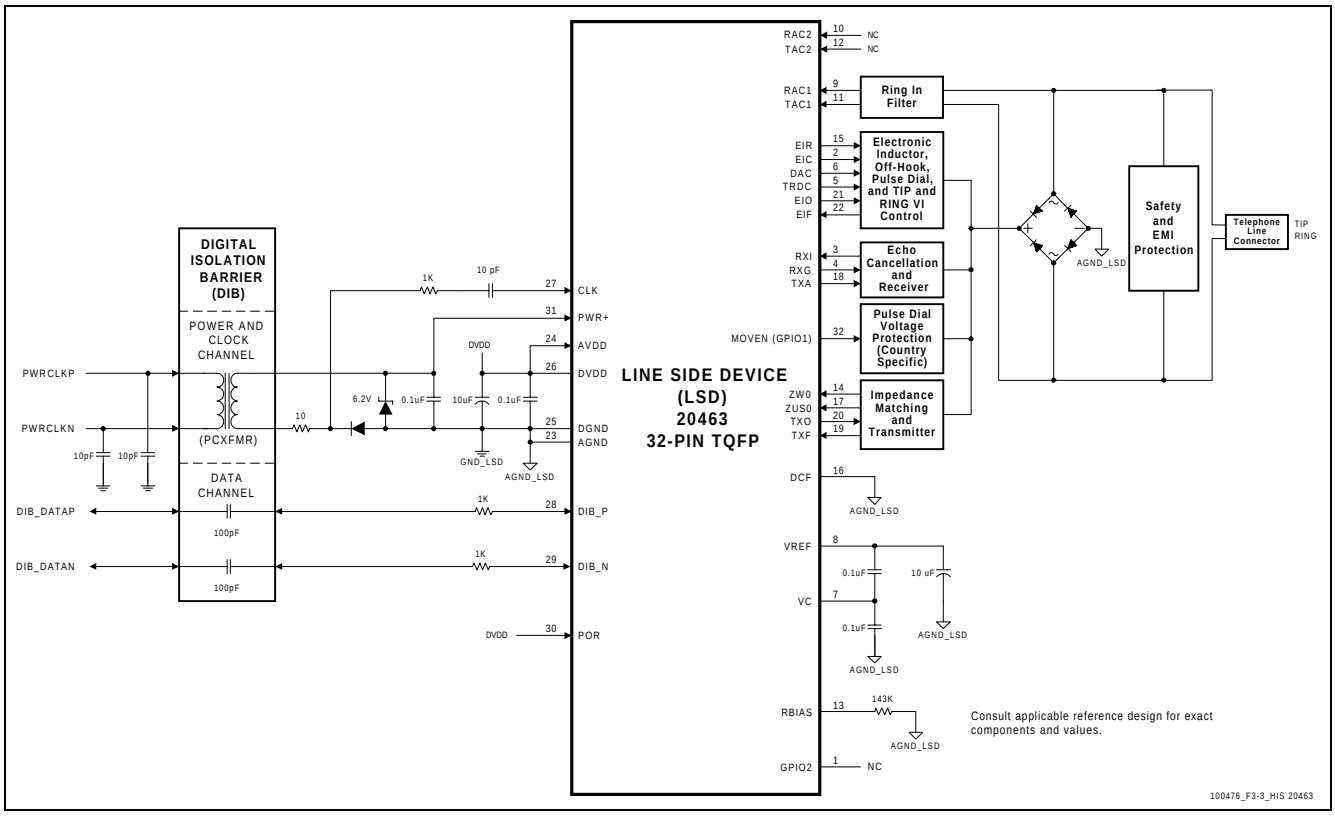


Figure 5. LSD (20463) 32-Pin TQFP Hardware Interface Signals

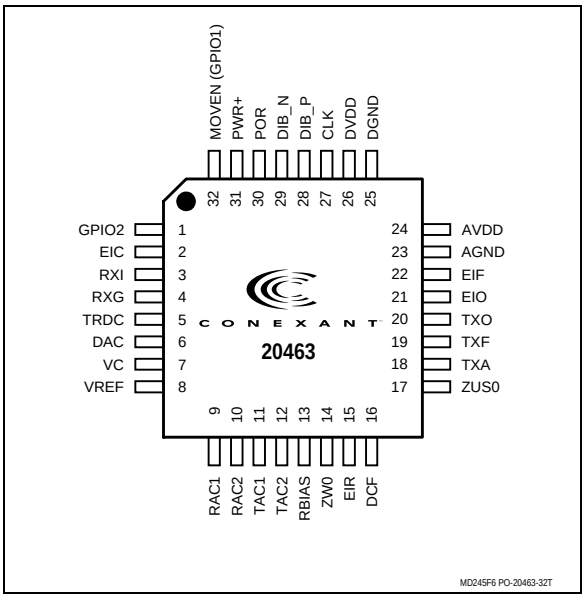


Figure 6. LSD (20463) 32-Pin TQFP Pin Signals

Table 3. LSD (20463) 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface
1	GPIO2	It/Ot12	NC
2	EIC	Oa	Telephone Line Interface Components
3	RXI	Ia	Telephone Line Interface Components
4	RXG	Oa	Telephone Line Interface Components
5	TRDC	Oa	Telephone Line Interface Components
6	DAC	Oa	Telephone Line Interface Components
7	VC	REF	VREF through 0.1 µF and to AGND_LSD through 0.1 µF
8	VREF	REF	VC through 0.1 µF and to AGND_LSD through 10 µF
9	RAC1	Ia	RING through 1 MΩ and 0.033 µF
10	RAC2	Ia	NC
11	TAC1	Ia	TIP through 1 MΩ and 0.033 µF
12	TAC2	Ia	NC
13	RBIAS	Ia	AGND_LSD through 143 KΩ
14	ZW0	Ia	Telephone Line Interface Components
15	EIR	Ot12	Telephone Line Interface Components
16	DCF	Ia	AGND_LSD
17	ZUS0	Ia	Telephone Line Interface Components
18	TXA	Oa	Telephone Line Interface Components
19	TXF	Ia	Telephone Line Interface Components
20	TXO	Oa	Telephone Line Interface Components
21	EIO	Oa	Telephone Line Interface Components
22	EIF	Ia	Telephone Line Interface Components
23	AGND	AGND_LSD	AGND_LSD
24	AVDD	PWR	LSD DVDD pin
25	DGND	GND_LSD	DIB PCXFMR secondary winding bottom through diode and 10 Ω in series and to GND_LSD
26	DVDD	PWR	LSD AVDD pin and to GND_LSD through 10 µF and 0.1 µF in parallel
27	CLK	I	DIB PCXFMR secondary winding bottom through 10 pF and 1 KΩ in series and through 10 Ω shared with LSD DGND pin through diode
28	DIB_P	I/O	DIB line side Data Positive capacitor through 1 KΩ
29	DIB_N	I/O	DIB line side Data Negative capacitor through 1 KΩ
30	POR	It	LSD DVDD pin
31	PWR+	PWR	DIB PCXFMR secondary winding top and to GND_LSD through 6.2 V zener diode and 0.1 µF in parallel
32	MOVEN (GPIO1)	Ot12	Telephone Line Interface Components

Notes:

1. I/O type:
   - Ia — Analog input
   - It — Digital input, TTL-compatible
   - Oa — Analog output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
   - AGND_LSD — Isolated LSD Analog Ground
   - GND_LSD — Isolated LSD Digital Ground
2. Interface Legend:
   - HSD — Host Side Device
3. Interface components may vary (see reference design for exact components and values).

VC (20437) Hardware Pins and Signals (S Models)

General

Microphone and analog speaker interface signals, as well as telephone handset/headset interface signals are provided to support functions such as speakerphone mode, telephone emulation, microphone voice record, speaker voice playback, and call progress monitor.

Speakerphone Interface

The following signals are supported:

- Speaker Out (M_SPKR_OUT); analog output - Should be used in speakerphone designs where sound quality is important
- Microphone (M_MIC_IN); analog input

Telephone Handset/Headset Interface

The following interface signals are supported:

- Telephone Input (M_LINE_IN), input (TELIN) –Optional connection to a telephone handset interface circuit
- Telephone output (M_LINE_OUTP); output (TELOUT) - Optional connection to a telephone handset interface circuit
- Center Voltage (VC); output reference voltage

HSD Interface

The following interface signals are supported:

- Reset (POR); input
- Sleep (SLEEP); input
- Master Clock (M_CLKIN); input
- Serial Clock (M_SCK); output
- Control (M_CNTRLSIN); input
- Serial Frame Sync (M_STROBE); output
- Serial Transmit Data (M_TXSIN); input
- Serial Receive Data (M_RXOUT); output

VC Interface Signals and Pin Assignments

The VC (20437) 32-pin TQFP hardware interface signals are shown by major interface in Figure 7, are shown by pin number in Figure 8, and are listed by pin number in Table 4.

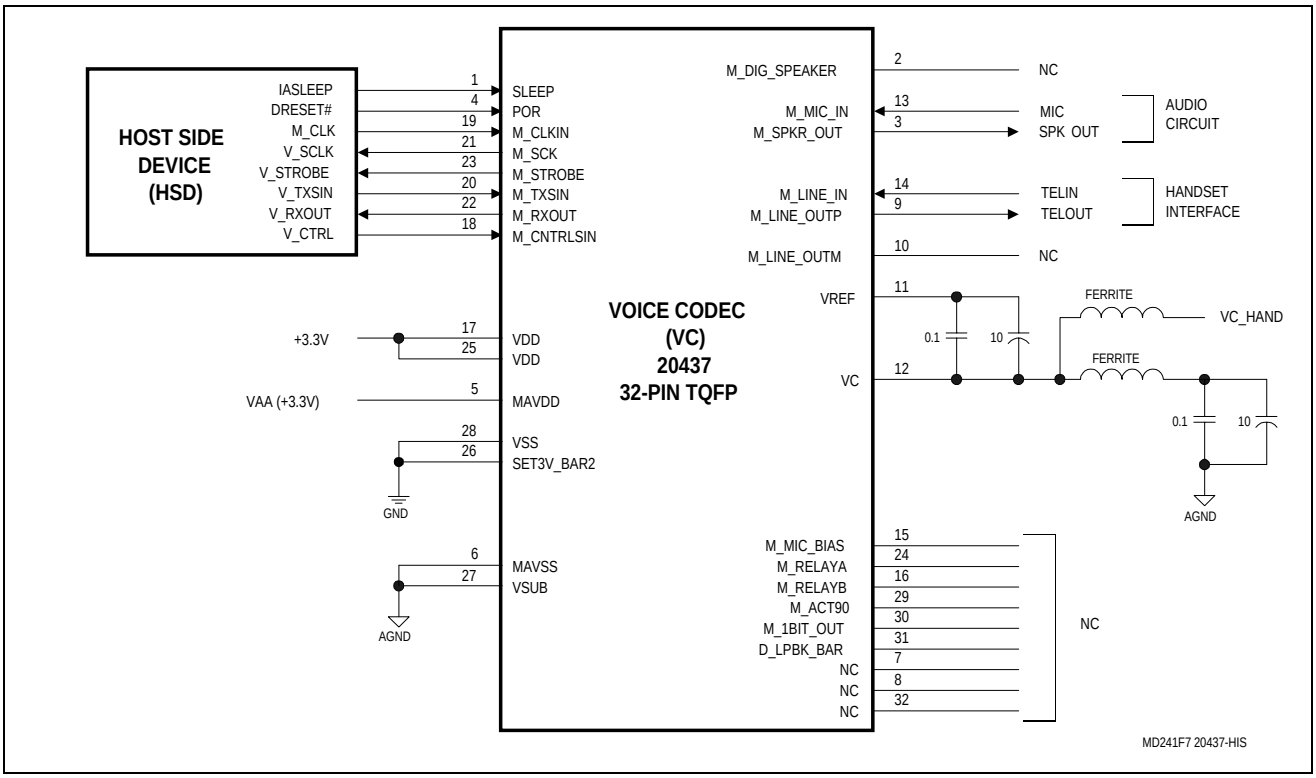


Figure 7. VC (20437) 32-Pin TQFP Hardware Interface Signals

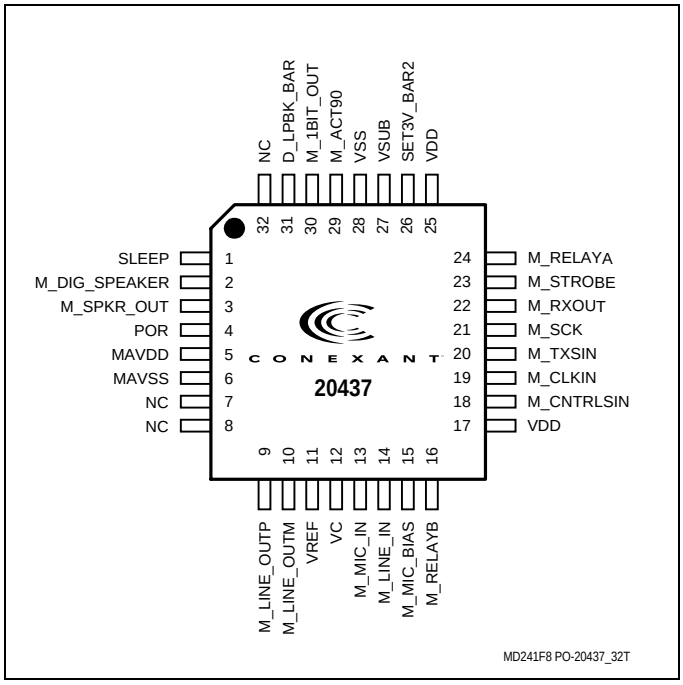


Figure 8. VC (20437) 32-Pin TQFP Pin Signals

Table 4. VC (20437) 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O	I/O Type	Interface
1	SLEEP	I	Itpd	HSD: IASLEEP
2	M_DIG_SPEAKER	O	Ot2	NC
3	M_SPKR_OUT	O	Oa	Speaker interface circuit
4	POR	I	Itpu	HSD: DRESET#
5	MAVDD		PWR	VAA (+3.3V)
6	MAVSS		AGND	AGND
7	NC			NC
8	NC			NC
9	M_LINE_OUTP (TELOUT)	O	Oa	Handset interface circuit
10	M_LINE_OUTM	O	Oa	NC
11	VREF		REF	VC through capacitors
12	VC		REF	AGND through ferrite bead and capacitors and to and to handset interface circuit (VC_HAND) through ferrite bead
13	M_MIC_IN	I	Ia	Microphone interface circuit
14	M_LINE_IN (TELIN)	I	Ia	Handset interface circuit
15	M_MIC_BIAS			NC
16	M_RELAYB			NC
17	VDD		PWR	+3.3V
18	M_CNTRLSIN	I	Itpd	HSD: V_CTRL
19	M_CLKIN	I	Itpd	HSD: M_CLK
20	M_TXSIN	I	Itpd	HSD: V_TXSIN
21	M_SCK	O	Ot2	HSD: V_SCLK
22	M_RXOUT	O	Ot2	HSD: V_RXOUT
23	M_STROBE	O	Ot2	HSD: V_STROBE
24	M_RELAYA	O	Ot2od	NC
25	VDD		PWR	+3.3V
26	M_SET3V_BAR2	I	Itpu	GND
27	VSUB		AGND	AGND
28	VSS		GND	GND
29	M_ACT90	I	Itpu	NC
30	M_1BIT_OUT	O	Ot2	NC
31	D_LPBK_BAR	I	Itpu	NC
32	NC			NC

Notes:

1. I/O types:

Ia	Analog input
It	Digital input, TTL-compatible
Itpd	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-up
It/Ot2	Digital input, TTL-compatible/digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
It/Ot12	Digital input, TTL-compatible/digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Oa	Analog output
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
AGND	Analog Ground
GND	Digital Ground

2. Interface Legend:

HSD	Host Side Device

Electrical and Environmental Specifications

The operating conditions are specified in Table 5.

The absolute maximum ratings are listed in Table 6.

The current and power requirements are listed in Table 7.

Table 5. Operating Conditions

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	+3.0 to +3.6	VDC
Operating Temperature Range	T_A	0 to +70	°C

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +4.0	VDC
Input Voltage	V_{IN}	-0.5 to (VIO +0.5)*	VDC
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (MAVDD + 0.5)	VDC
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VIO +0.5)*	VDC
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	VDC
Latch-up Current (25°C)	I_{TRIG}	±400	mA
* VIO = +3.3V ± 0.3V or +5V ± 5%.			

Table 7. Current and Power Requirements

	Conditions			Current		Power	
HSD (11242) + LSD (20463)							
Device State (Dx) and Bus State (Bx)	**PCI Bus Power**	**PCI Clock (PCICLK)**	**Line Connection**	**Typical Current (mA)**	**Maximum Current (mA)**	**Typical Power (mW)**	**Maximum Power (mW)**
D0, B0	On	Running	Yes	45.4	50.0	150	180
D0, B0	On	Running	No	11.8	13.0	39.0	46.7
D3, B0	On	Running	No	11.8	13.0	39.0	46.7
D3, B1	On	Running	No	11.8	13.0	39.0	46.7
D3, B2, B3 (D3hot)	On	Stopped	No	11.8	13.0	39.0	46.7
D3, B3 (D3cold)	Off	Stopped	No	1.9	2.1	6.3	7.6

Notes:

Operating voltage: VDD = +3.3V ± 0.3V.

Test conditions: VDD = +3.3 VDC for typical values; VDD = +3.6 VDC for maximum values.

Definitions:

PCI Bus Power — On: PCI Bus +5V and +3.3V on (modem normally powered by +3.3V from PCI Bus +3.3V or regulated down from PCI Bus +5V); PCIRST# not asserted.
Off: PCI Bus +5V and +3.3V off (modem normally powered by +3.3V from Vaux or Vpci); PCIRST# asserted.

MiniPCI Bus Power — On: PCI Bus +3.3V on (modem normally powered by +3.3V from PCI Bus +3.3V; PCIRST# not asserted.
Off: PCI Bus +3.3V off (modem normally powered by +3.3V from Vaux or Vpci); PCIRST# asserted.

CardBus Power — On: CardBus +3.3V on (modem normally powered by CardBus +3.3V).
Off: CardBus +3.3V off (modem normally powered by CardBus +3.3V).

PCI Clock (PCICLK) — Running: PCI Bus signal PCICLK running (PCI Bus and MiniPCI Bus only).
Stopped: PCI Bus signal PCICLK stopped (off) (PCI Bus and MiniPCI Bus only).

Line connection: — Yes: Off-hook, IA powered.
No: On-hook, IA powered down.

Device States: — D3: Low power state. Suspend state can change the system power state; the resulting power state depends on the system architecture (OS, BIOS, hardware) and system configuration (i.e., other PCI installed cards).
D0: Full power state.

Device and Bus States:
- D0, B0: Any PCI transaction, PCICLK running, VCC present.
- D3, B1: No PCI Bus transactions, PCICLK running, VCC present.
- D3, B2, B3: No PCI transactions, PCICLK stopped, VCC may be present.
- D3, B3: No PCI transactions, PCICLK stopped, no VCC.

Refer to the PCI Bus Power Management Interface Specification for additional information.

Package Dimensions

The package dimensions are shown in Figure 9 (100-pin TQFP) and Figure 10 (32-pin TQFP).

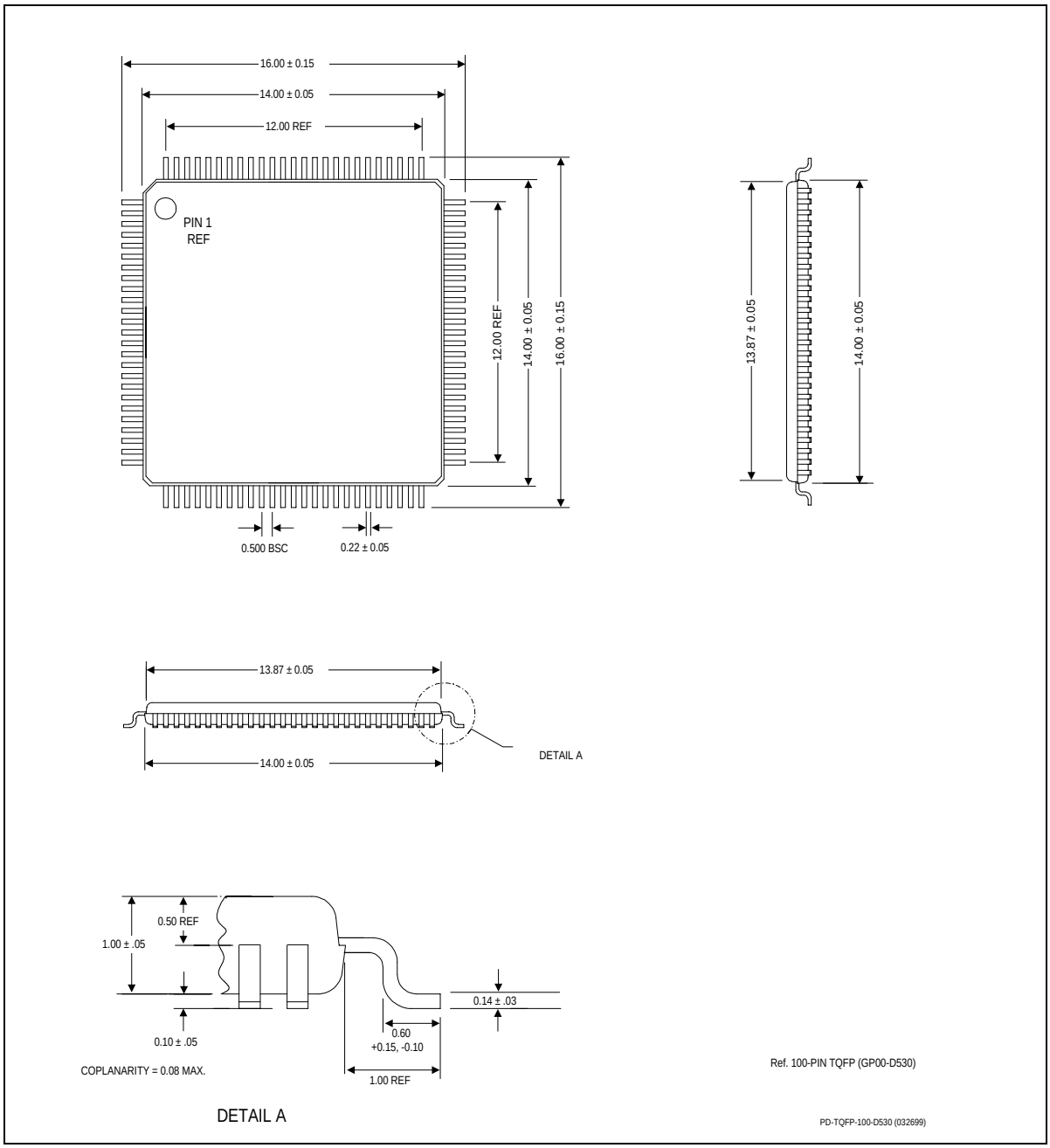
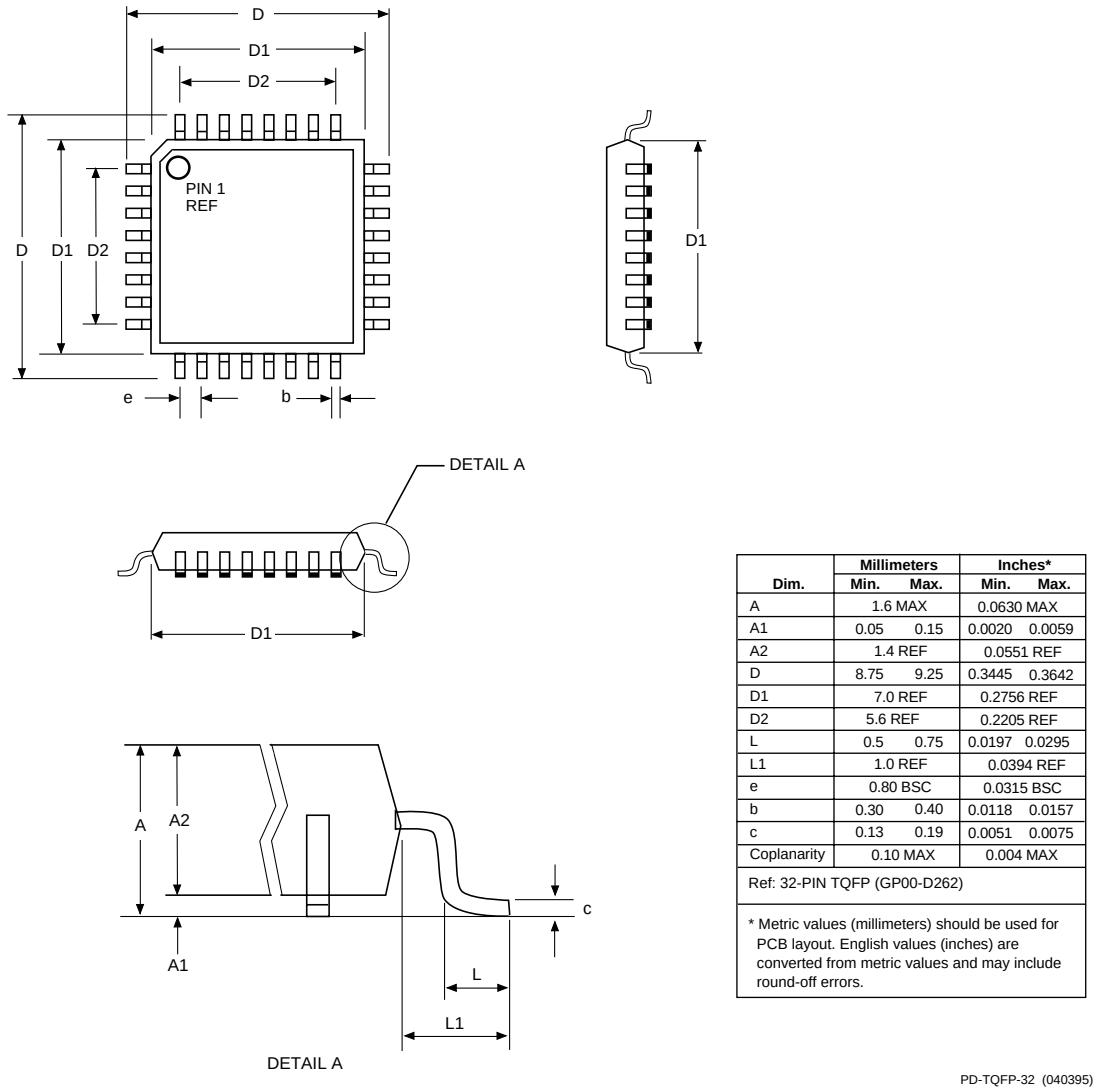


Figure 9. Package Dimensions - 100-Pin TQFP



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	8.75	9.25	0.3445	0.3642
D1	7.0 REF		0.2756 REF	
D2	5.6 REF		0.2205 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX		0.004 MAX	

Ref: 32-PIN TQFP (GP00-D262)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-32 (040395)

Figure 10. Package Dimensions - 32-Pin TQFP

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