

## Features

- Permanent Software Write Protection for the First-Half of the Array
  - Software Procedure to Verify Write Protect Status
- Hardware Write Protection for the Entire Array
- Low Voltage and Standard Voltage Operation
  - 5.0 ( $V_{CC} = 4.5V$  to  $5.5V$ )
  - 2.7 ( $V_{CC} = 2.7V$  to  $5.5V$ )
  - 1.8 ( $V_{CC} = 1.8V$  to  $5.5V$ )
- Internally Organized 256 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 KHz (1.8V and 2.7V) and 400 KHz (5.0V) Compatibility
- 16-Byte Page Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3,000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP, 8-Pin JEDEC SOIC and 8-Pin TSSOP Packages

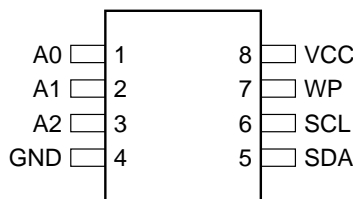
## Description

The AT34C02 provides 2048 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 256 words of 8 bits each. The first-half of the device incorporates a software write protection feature while hardware write protection for the entire array is available via an external pin as well. Once the software write protection is enabled, by sending a special command to the device, it cannot be reversed. The hardware write protection is controlled with the WP pin and can be used to protect the entire array, whether or not the software write protection has been enabled. This allows the user to protect none, first-half, or all of the array depending on the application. The device is optimized for use in many industrial and commercial applications where low power and low voltage operations are essential. The AT34C02 is available in space saving 8-pin PDIP, 8-pin JEDEC SOIC, and 8-pin TSSOP packages and is accessed via a 2-wire serial interface. In addition, it is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), and 1.8V (1.8V to 5.5V) versions.

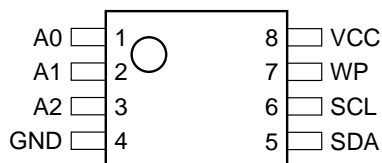
## Pin Configurations

Pin Name	Function
A0 to A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

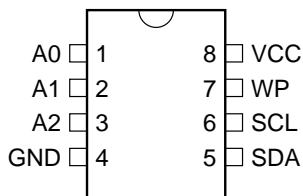
8-Pin SOIC



8-Pin TSSOP



8-Pin PDIP



## 2-Wire Serial EEPROM with Permanent Software Write Protect

2K (256 x 8)

## AT34C02

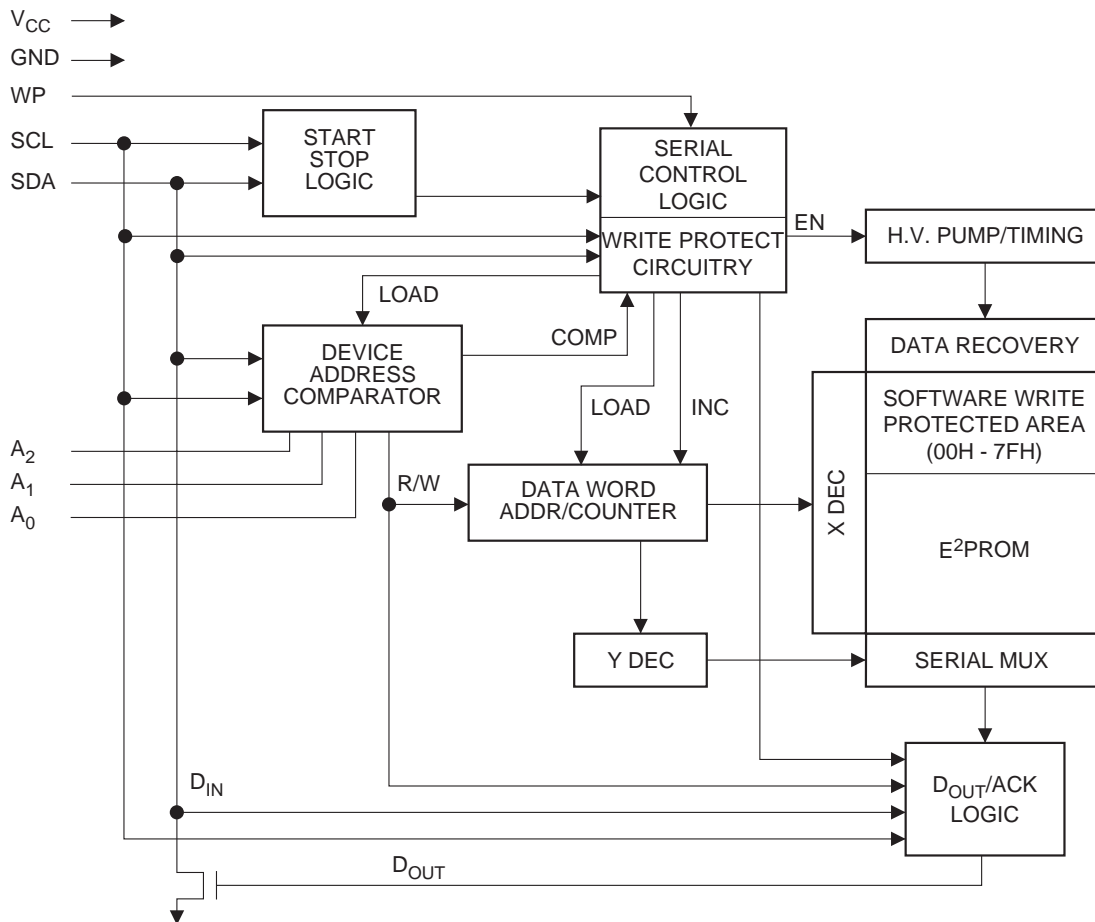


## Absolute Maximum Ratings\*

Operating Temperature .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-1.0V to +7.0V
Maximum Operating Voltage.....	6.25V
DC Output Current.....	5.0 mA

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Block Diagram



## Pin Description

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**SERIAL DATA (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

**DEVICE/PAGE ADDRESSES (A2, A1, A0):** The A2, A1 and A0 pins are device address inputs that are hard wired for the AT34C02. As many as eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

**WRITE PROTECT (WP):** The AT34C02 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when con-

nected to ground (GND) or when left floating. When the Write Protect pin is connected to  $V_{CC}$ , the write protection feature is enabled for the entire array. The write protection modes are shown in the following table.

## AT34C02 Write Protection Modes

WP Pin Status	Write Protect Register	Part of the Array Write Protected
$V_{CC}$	—	Full Array (2K)
GND or Floating	Not Programmed	Normal Read/Write
GND or Floating	Programmed	First-Half of Array (1K: 00H - 7FH)

## Pin Capacitance<sup>(1)</sup>

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = +1.8\text{V}$

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
$C_{IN}$	Input Capacitance ( $A_0$ , $A_1$ , $A_2$ , SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested

## DC Characteristics

Applicable over recommended operating range from:  $T_{AI} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  $T_{AC} = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$  (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{CC1}$	Supply Voltage		1.8		5.5	V
$V_{CC2}$	Supply Voltage		2.7		5.5	V
$V_{CC3}$	Supply Voltage		4.5		5.5	V
$I_{CC}$	Supply Current $V_{CC} = 5.0\text{V}$	READ at 100 KHz		0.4	1.0	mA
$I_{CC}$	Supply Current $V_{CC} = 5.0\text{V}$	WRITE at 100 KHz		2.0	3.0	mA
$I_{SB1}$	Standby Current $V_{CC} = 1.8\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$		0.6	3.0	$\mu\text{A}$
$I_{SB2}$	Standby Current $V_{CC} = 2.7\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$		1.6	4.0	$\mu\text{A}$
$I_{SB3}$	Standby Current $V_{CC} = 5.0\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$		8.0	18.0	$\mu\text{A}$
$I_{LI}$	Input Leakage Current	$V_{IN} = V_{CC}$ or $V_{SS}$		0.10	3.0	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$V_{OUT} = V_{CC}$ or $V_{SS}$		0.05	3.0	$\mu\text{A}$
$V_{IL}$	Input Low Level <sup>(1)</sup>		-0.6		$V_{CC} \times 0.3$	V
$V_{IH}$	Input High Level <sup>(1)</sup>		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
$V_{OL2}$	Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V
$V_{OL1}$	Output Low Level $V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.



## AC Characteristics

Applicable over recommended operating range from  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  $C_L = 1$  TTL Gate and  $100\text{ pF}$  (unless otherwise noted).

Symbol	Parameter	1.8V, 2.7V		5.0V		Units
		Min	Max	Min	Max	
$f_{\text{SCL}}$	Clock Frequency, SCL		100		400	kHz
$t_{\text{LOW}}$	Clock Pulse Width Low	4.7		1.2		$\mu\text{s}$
$t_{\text{HIGH}}$	Clock Pulse Width High	4.0		0.6		$\mu\text{s}$
$t_i$	Noise Suppression Time <sup>(1)</sup>		100		50	ns
$t_{\text{AA}}$	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	$\mu\text{s}$
$t_{\text{BUF}}$	Time the bus must be free before a new transmission can start <sup>(1)</sup>	4.7		1.2		$\mu\text{s}$
$t_{\text{HD,STA}}$	Start Hold Time	4.0		0.6		$\mu\text{s}$
$t_{\text{SU,STA}}$	Start Set-up Time	4.7		0.6		$\mu\text{s}$
$t_{\text{HD,DAT}}$	Data In Hold Time	0		0		$\mu\text{s}$
$t_{\text{SU,DAT}}$	Data In Set-up Time	200		100		ns
$t_{\text{R}}$	Inputs Rise Time <sup>(1)</sup>		1.0		0.3	$\mu\text{s}$
$t_{\text{F}}$	Inputs Fall Time <sup>(1)</sup>		300		300	ns
$t_{\text{SU,STO}}$	Stop Set-up Time	4.7		0.6		$\mu\text{s}$
$t_{\text{DH}}$	Data Out Hold Time	100		50		ns
$t_{\text{WR}}$	Write Cycle Time		10		10	ms
Endurance <sup>(1)</sup>	5.0V, 25°C, Page Mode	1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

## Memory Organization

**AT34C02, 2K Serial EEPROM:** The 2K is internally organized with 256 pages of 1 byte each. Random word addressing requires a 8-bit data word address.

## Device Operation

**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the

stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

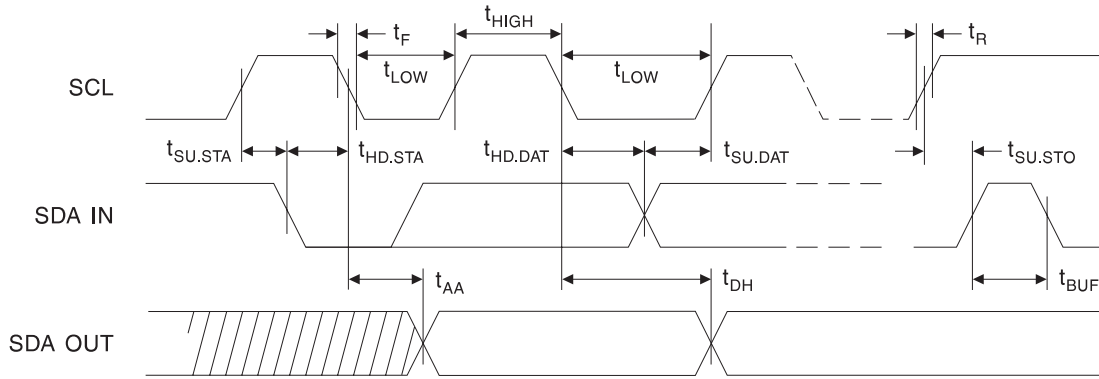
**ACKNOWLEDGE:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

**STANDBY MODE:** The AT34C02 features a low power standby mode which is enabled: (a) upon power-up or (b) after the receipt of the STOP bit and the completion of any internal operations.

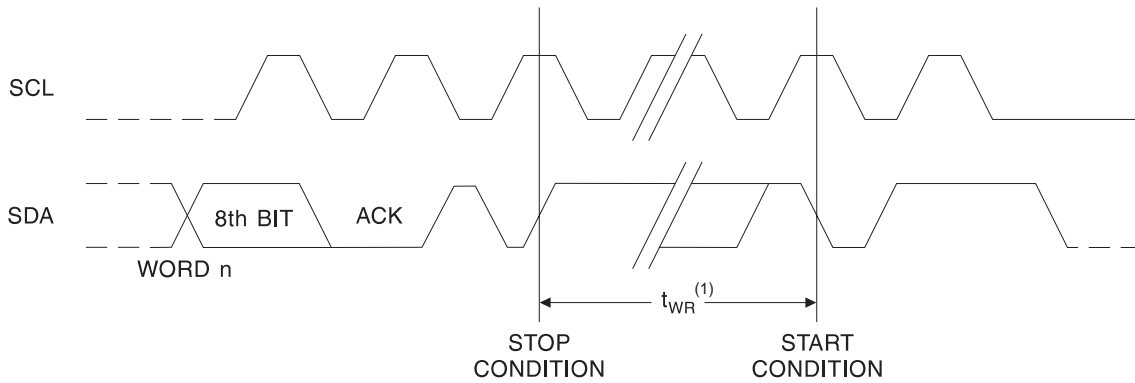
**MEMORY RESET:** After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

**Bus Timing SCL: Serial Clock SDA: Serial Data I/O**

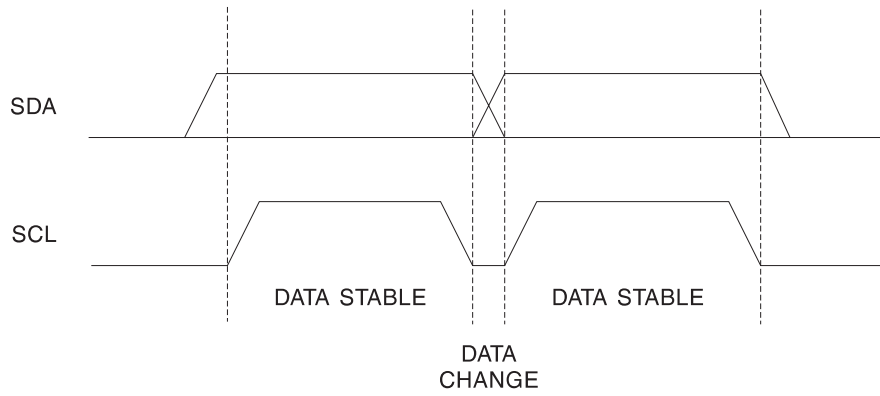


**Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O**

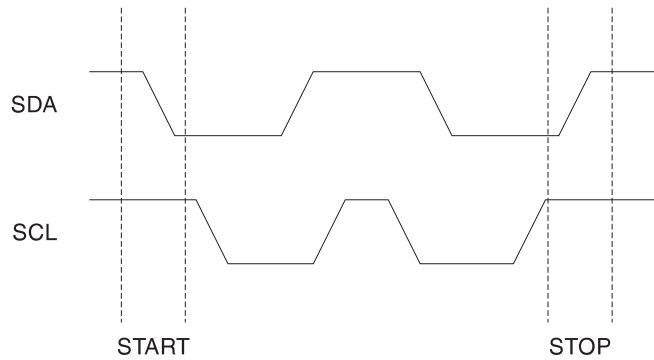


Note: 1. The write cycle time  $t_{WR}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

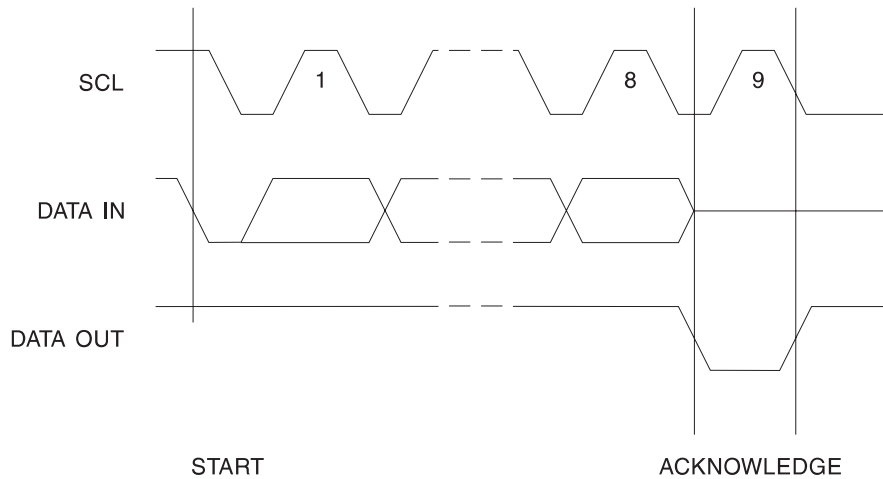
## Data Validity



## Start and Stop Condition



## Output Acknowledge



## Device Addressing

The 2K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 2).

The device address word consists of a mandatory one-zero sequence for the first four most-significant bits (1010) for normal read and write operations and 0110 for writing to the write protect register.

The next 3 bits are the A2, A1 and A0 device address bits for the AT34C02 EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state. The device will not acknowledge if the write protect register has been programmed and the control code is 0110.

## Write Operations

**BYTE WRITE:** A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 3).

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

**PAGE WRITE:** The 2K device is capable of 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 4).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

**ACKNOWLEDGE POLLING:** Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

## Write Protection

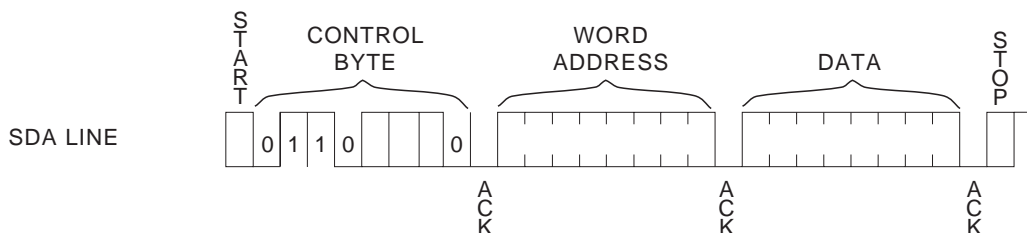
The software write protection, once enabled, permanently write protects only the first-half of the array (00H - 7FH) while the hardware write protection, via the WP pin, is used to protect the entire array.

**SOFTWARE WRITE PROTECTION:** The software write protection is enabled by sending a command, similar to a normal write command, to the device which programs the write protect register. This must be done with the WP pin low. The write protect register is programmed by sending a write command with the device address of 0110 instead of 1010 with the address and data bit being don't cares (refer to Figure 1). Once the software write protection has been enabled, the device will no longer acknowledge the 0110 control byte. The software write protection cannot be reversed even if the device is powered down. The write cycle time must be observed.

**HARDWARE WRITE PROTECTION:** The WP pin can be connected to  $V_{CC}$ , GND, or left floating. Connecting the WP pin to  $V_{CC}$  will write protect the entire array, regardless of whether or not the software write protection has been enabled. The software write protection register cannot be programmed when the WP pin is connected to  $V_{CC}$ . If the WP pin is connected to GND or left floating, the write protection mode is determined by the status of the software write protect register.

WP Connected to GND or Floating				
Start	R/W Bit	Write Protect Register	Acknowledgment from Device	Action from Device
1010	R	X	ACK	Read Array
1010	W	Programmed	ACK	Can Write to First Half Only
1010	W	Not Programmed	ACK	Can Write to Full Array
0110	R	Programmed	No ACK	Stop - Indicates Write Protect Register is Programmed
0110	R	Not Programmed	ACK	Read Out Data Don't Care. Indicates WP Register is Not Prog
0110	W	Programmed	No ACK	Stop - Indicates Write Protect Register is Programmed
0110	W	Not Programmed	ACK	Program Write Protect Register (irreversible)
WP Connected to V <sub>CC</sub>				
1010	R	X	ACK	Read Array
1010	W	Programmed	ACK	Device Write Protect
1010	W	Not Programmed	ACK	Device Write Protect
0110	R	Programmed	No ACK	Stop - Indicates Write Protect Register is Programmed
0110	R	Not Programmed	ACK	Read Out Data Don't Care. Indicates WP Register is Not Prog
0110	W	Programmed	No ACK	Stop - Indicates Write Protect Register is Programmed
0110	W	Not Programmed	ACK	Cannot Program Write Protect Register

**Figure 1.** Setting Write Protect Register



## Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

**CURRENT ADDRESS READ:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. To end

the command, the microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 5).

**RANDOM READ:** A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. To end the command, the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

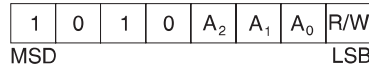


**SEQUENTIAL READ:** Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when

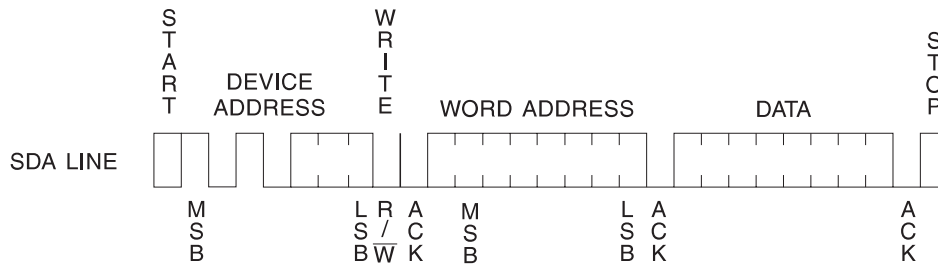
the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 7).

**WRITE PROTECT REGISTER STATUS:** To find out if the register has been programmed, the same procedure is used as to program the register except that the R/W bit is set to 1. If the device acknowledges, then the write protect register has not been programmed. Otherwise, it has been programmed and the device is permanently write protected at the first half of the array.

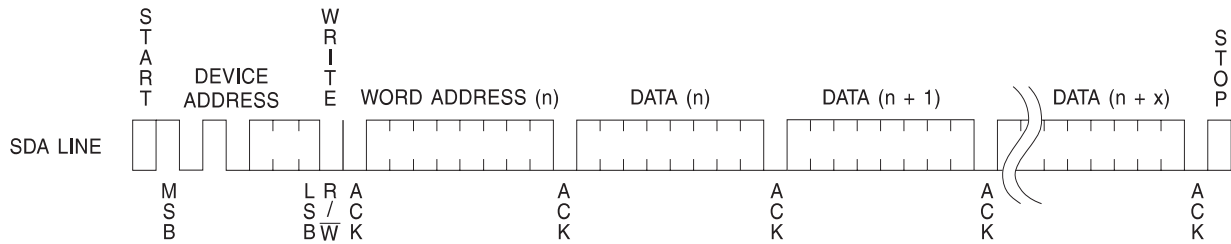
**Figure 2.** Device Address



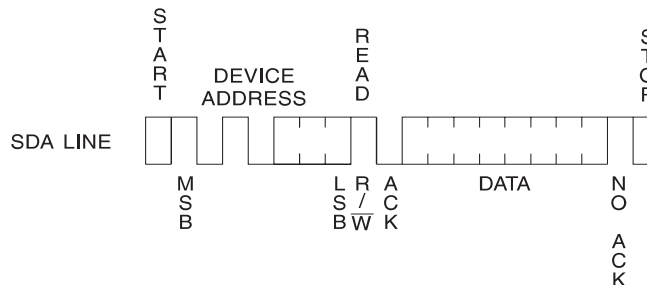
**Figure 3.** Byte Write



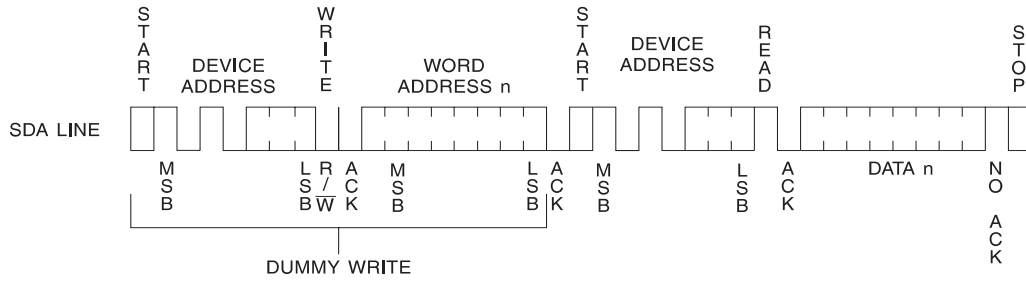
**Figure 4.** Page Write



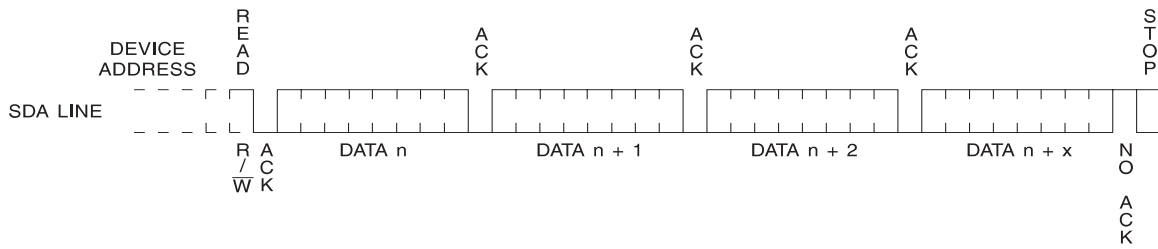
**Figure 5.** Current Address Read



**Figure 6. Random Read**



**Figure 7. Sequential Read**



## Ordering Information

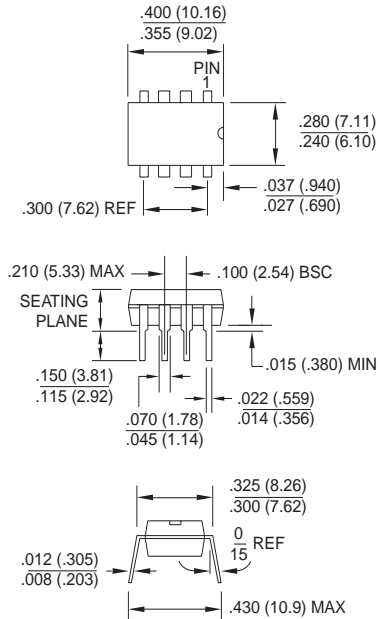
$t_{WR}$ (max) (ms)	$I_{CC}$ (max) ( $\mu$ A)	$I_{SB}$ (max) ( $\mu$ A)	$f_{MAX}$ (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT34C02-10PC AT34C02N-10SC AT34C02-10TC	8P3 8S1 8T	Commercial (0°C to 70°C)
	3000	18	400	AT34C02-10PI AT34C02N-10SI AT34C02-10TI	8P3 8S1 8T	Industrial (-40°C to 85°C)
10	1500	4	100	AT34C02-10PC-2.7 AT34C02N-10SC-2.7 AT34C02-10TC-2.7	8P3 8S1 8T	Commercial (0°C to 70°C)
	1500	4	100	AT34C02-10PI-2.7 AT34C02N-10SI-2.7 AT34C02-10TI-2.7	8P3 8S1 8T	Industrial (-40°C to 85°C)
10	800	3	100	AT34C02-10PC-1.8 AT34C02N-10SC-1.8 AT34C02-10TC-1.8	8P3 8S1 8T	Commercial (0°C to 70°C)
	800	3	100	AT34C02-10PI-1.8 AT34C02N-10SI-1.8 AT34C02-10TI-1.8	8P3 8S1 8T	Industrial (-40°C to 85°C)

Package Type	
<b>8P3</b>	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>8S1</b>	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
<b>8T</b>	8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
<b>Blank</b>	Standard Operation (4.5V to 5.5V)
<b>-2.7</b>	Low Voltage (2.7V to 5.5V)
<b>-1.8</b>	Low Voltage (1.8V to 5.5V)

## Packaging Information

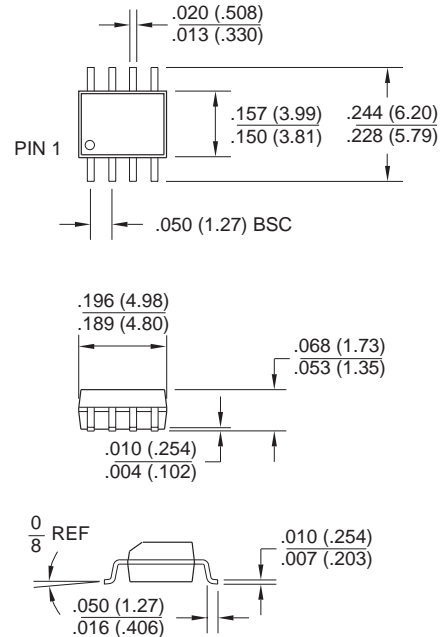
### 8P3, 8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

Dimensions in Inches and (Millimeters)



### 8S1, 8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Dimensions in Inches and (Millimeters)



### 8T, 8-Lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)

Dimensions in Millimeters and (Inches)

