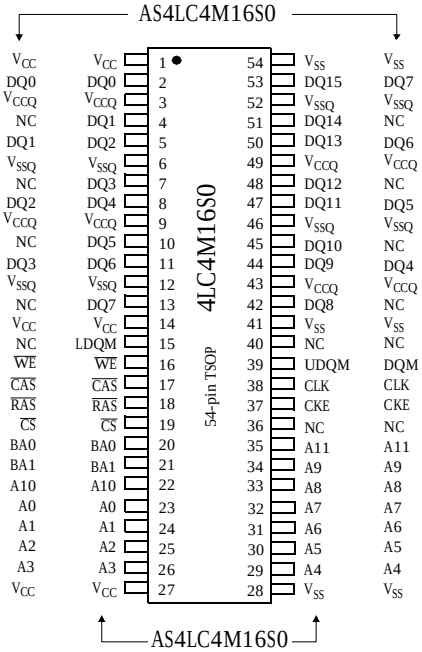
3.3V 4Mx16 and 8Mx8 CMOS synchronous DRAM

Features

- PC100/133 compliant
- Organization
  - 2,097,152 words × 8 bits × 4 banks (8M×8)
  - 1,048,576 words × 16 bits × 4 banks (4M×16)
- Fully synchronous
  - All signals referenced to positive edge of clock
- Four internal banks controlled by BA0/BA1 (bank select)
- High speed
  - 133/125/100 MHz
  - 5.4 ns (133 MHz)/6 ns (125/100 MHz) clock access time
- Low power consumption
  - Standby: 7.2 mW max, CMOS I/O
- 4096 refresh cycles, 64 ms refresh interval
- Auto refresh and self refresh
- Automatic and direct precharge
- Burst read, single write operation
- Can assert random column address in every cycle
- LVTTL compatible I/O
- 3.3V power supply
- JEDEC standard package, pinout and function
  - 400 mil, 54-pin TSOP II
- Read/write data masking
- Programmable burst length (1/2/4/8/full page)
- Programmable burst sequence (sequential/interleaved)
- Programmable $\overline{CAS}$ latency (2/3)

Pin arrangement



Pin designation

Pin(s)	Description
DQM (8M×8) UDQM/LDQM (4M×16)	Output disable/write mask
A0 to A11	Address inputs
BA0, BA1	Bank select inputs
DQ0 to DQ7 (8M×8) DQ0 to DQ15 (4M×16)	Input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}, V_{CCQ}	Power (3.3V ± 0.3V)
V_{SS}, V_{SSQ}	Ground
CLK	Clock input
CKE	Clock enable

Selection guide

		Symbol	-75 (PC133)	-8	-10F (PC100)	-10 (PC100)	Unit
Bus frequency		f_{max}	133	125	100	100	MHz
Minimum clock access time	CL = 2	t_{AC}	–	–	6	–	ns
	CL = 3	t_{AC}	5.4	6	–	6	ns
Minimum setup time		t_S	1.5	2	2	2	ns
Minimum hold time		t_H	0.8	1.0	1.0	1.0	ns
Minimum $\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}	3	3	2	3	cycles
Minimum $\overline{RAS}$ precharge time		t_{RP}	3	3	2	3	cycles
Remarks: ($CL/t_{RCD}/t_{RP}$)			3/3/3	3/3/3	2/2/2	3/3/3	

Functional description

The AS4LC8M8S0 and AS4LC4M16S0 are high-performance 64-megabit CMOS Synchronous Dynamic Random Access Memory (SDRAM) devices organized as 2,097,152 words × 8 bits × 4 banks, and 1,048,576 words × 16 bits × 4 banks, respectively. Very high bandwidth is achieved using a pipelined architecture where all inputs and outputs are referenced to the rising edge of a common clock. Programmable burst mode can be used to read up to a full page of data without selecting a new column address.

The four internal banks can be alternately accessed (read or write) at the maximum clock frequency for seamless interleaving operations. This provides a significant advantage over asynchronous EDO and fast page mode devices.

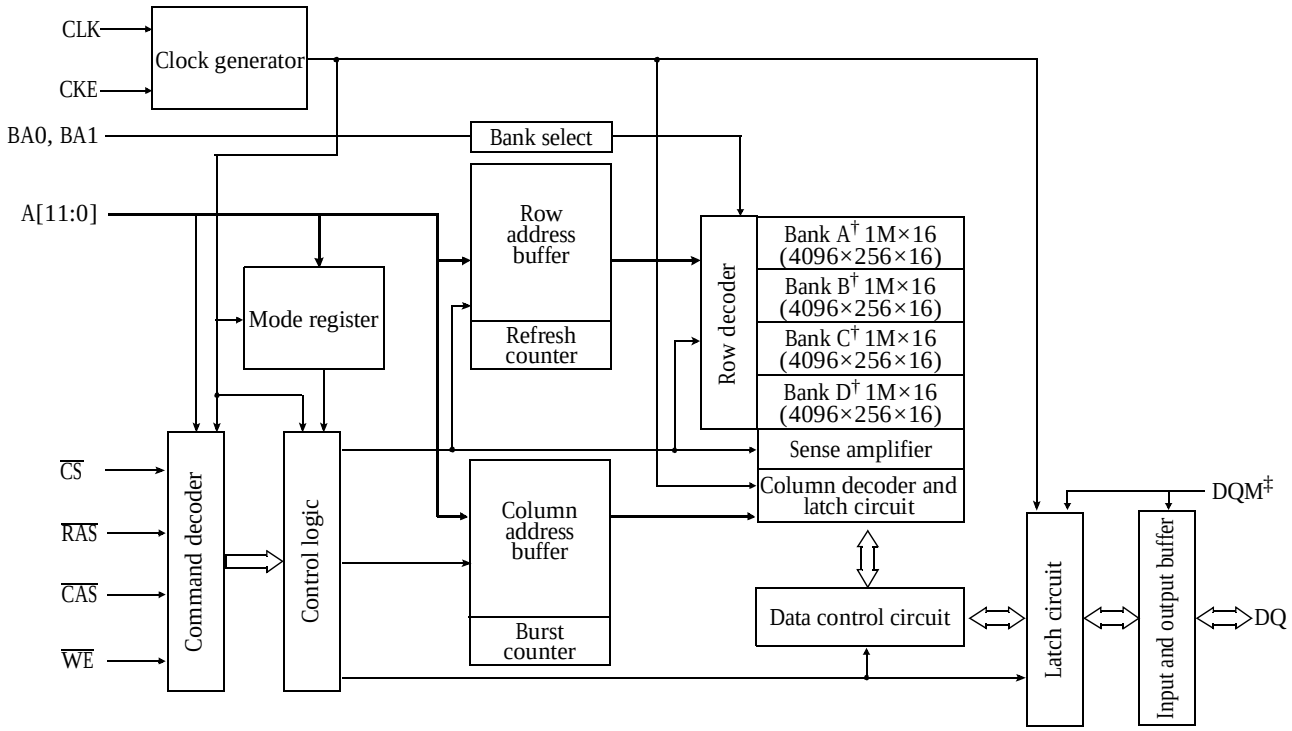
This SDRAM product also features a programmable mode register, allowing users to select read latency as well as burst length and type (sequential or interleaved). Lower latency improves first data access in terms of CLK cycles, while higher latency improves maximum frequency of operation. This feature enables flexible performance optimization for a variety of applications.

DRAM commands and functions are decoded from control inputs. Basic commands are as follows:

- Mode register set
- Deactivate bank
- Deactivate all banks
- Select row; activate bank
- Select column; write
- Select column; read
- Deselect; power down
- CBR refresh
- Auto precharge with read/write
- Self-refresh

The 64 Mb DRAM devices are available in 400-mil plastic TSOP II packages and have 54 pins in each configuration. Both devices operate with a power supply of 3.3V ± 0.3V. Multiple power and ground pins are provided for low switching noise and EMI. Inputs and outputs are LVTTL-compatible.

Logic block diagram



† For AS4LC8M8S0, Banks A-D will read 8M×8 (4096×512×8).
‡ For AS4LC4M16S0, DQM will be UDQM and LDQM.

Pin descriptions

Pin	Name	Description
CLK	System clock	All operations synchronized to rising edge of CLK. It also increments the burst counters.
CKE	Clock enable	Controls CLK input. If CKE is high, the next CLK rising edge is valid. If CKE is low, the internal clock is suspended from the next clock cycle and the burst address and output states are frozen. Pulling CKE low has the following effects: all banks idle: Precharge power down and Self refresh. row active in any bank: Active power down. burst/access in progress: Clock suspend. When in Power down or Self refresh mode, CKE becomes asynchronous until exiting the mode.
$\overline{CS}$	Chip select	Enables or disables device operation by masking or enabling all inputs except CLK, CKE, UDQM/LDQM (×16), DQM (×8).
A0~A11	Address	Row and column addresses are multiplexed. Row address: A0~A11. Column address (8M×8): A0~A8. Column address (4M×16): A0~A7.
BA0, BA1	Bank select	Memory cell array is organized in 4 banks. BA0 and BA1 select which internal bank will be active during activate, read, write, and precharge operations.
$\overline{RAS}$	Row address strobe	Enables row access and precharge operation. When $\overline{RAS}$ is low, row address is latched at the rising edge of CLK.
$\overline{CAS}$	Column address strobe	Enables column access. When $\overline{CAS}$ is low, starting column address for the burst access operation is latched at the rising edge of the CLK.
$\overline{WE}$	Write enable	Enables write operation and row precharge operation.
×8: DQM ×16: UDQM/LDQM	Output disable/ write mask	Controls I/O buffers. When DQM is high, output buffers are disabled during a read operation and input data is masked during a write operation. DQM latency is 2 clocks for Read and 0 clocks for Write. For ×16, LDQM controls lower byte (DQ0–7) and UDQM controls upper byte (DQ8–15). For ×8, only one DQM controls the 8 DQs. UDQM and LDQM are considered same state when referenced as DQM.
DQ0~DQ15	Data input/output	Data inputs/outputs are multiplexed. Data bus for 8M×8 is DQ0~DQ7 only.
V_{DD}/V_{SS}	Power supply/ground	Power and ground for core logic and input buffers.
V_{DDQ}/V_{SSQ}	Data output power/ ground	Power and ground for data output buffers.

Commands

Command			CKE_{n-1}	CKE_n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0/BA1	A10	A9–A0	DQ	Note
Register	Mode register set		H*	H	L	L	L	L	X		Op code		X	1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	–		–		3
	Self refresh	Entry	H	L	L	L	L	H	X	–	X	–	X	3
		Exit	L	H	L	H	H	H	X	–		–		3
					H	X	X	X	X	–		–		3
Bank activate			H	H	L	L	H	H	X	V	row address		X	
Read	Auto precharge disable		H	H	L	H	L	H	X	V	L	column address	X	4
	Auto precharge enable										H			4,5
Write	Auto precharge disable		H	H	L	H	L	L	X	V	L	column address	Valid	4
	Auto precharge enable										H			4,5
Burst stop			H	H	L	H	H	L	X		X		Active	6
Precharge	Selected bank		H	H	L	L	H	L	X	V	L	X	X	4
	All banks									X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X	X	X	X	
					L	V	V	V						
		Exit	L	H	X	X	X	X						
Precharge power down mode		Entry	H	L	H	X	X	X	X	X	X	X	X	
					L	H	H	H						
		Exit	L	H	H	X	X	X						
					L	V	V	V						
DQM	Write enable/output enable		H	H	X	X	X	X	H	X	X	X	X	7
	Write inhibit/Output High-Z													
No operation command			H	X	H	X	X	X	X	X	X	X	X	
					L	H	H	H	X					

1 OP = operation code.
A0~A11 and BA0~BA1 program keys.

2 MRS can be issued only when all banks are precharged. A new command can be issued 1 clock cycle after MRS.

3 Auto refresh functions similarly to CBR DRAM refresh. However, precharge is automatic.
Auto/self refresh can only be issued after all banks are precharged.

4 BA0~BA1: bank select addresses.
If A10/AP is High at row precharge, BA0 and BA1 are ignored and all banks are selected.
During read, write, row active, and prechage:
If BA0 and BA1 are Low, Bank A is selected.
If BA0 = Low and BA1 = High, Bank B is selected.
If BA0 = High and BA1 = Low, Bank C is selected.
If BA0 and BA1 are High, Bank D is selected.

5 A new read/write command to the same bank cannot be issued during a burst read/write with auto precharge.
A new row active command can be issued after t(t_{RP}/t_{CK} + BL +) cycles.

6 Burst stop command valid at every burst length.

7 DQM sampled at positive edge of CLK. Data-in may be masked at every CLK (Write DQM latency is 0).
Data-out mask is active 2 CLK cycles after issuance. (Read DQM latency is 2).

Mode register fields

Register programmed with MRS											
Address	A11~A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU†	WBL	TM		CAS latency			BT	Burst length		

† RFU = 0 during MRS cycle.

Write burst length	
A9	Length
0	Programmed burst length
1	Single burst

Burst type	
A3	Type
0	Sequential
1	Interleaved

Test mode		
A8	A7	Type
0	0	Mode register set
0	1	Reserved
1	0	Reserved
1	1	Reserved

CAS latency			
A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	X	X	Reserved

Burst length				
A2	A1	A0	BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full page	Reserved

Recommended operating conditions

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC},V_{CCQ}	3.0	3.6	V
	GND	0.0	0.0	V
Input voltage	V_{IH}	2.0	V_{CC} + 0.3	V
	V_{IL}	–0.3†	0.8	V
Output voltage‡	V_{OH}	2.4	–	V
	V_{OL}	–	0.4	V
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{CC}	I_L	–5	+5	uA
Output leakage current DQs are disabled 0V ≤ V_{OUT} ≤ V_{CCQ}	I_{OZ}	–5	+5	uA
Ambient operating temperature	T_A	0	70	°C

† V_{IL} min = –1.5V for pulse widths less than 5 ns.
‡ I_{OH} = –2mA, and I_{OL} = 2mA.
Recommended operating conditions apply throughout this document unless otherwise specified.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{IN},V_{OUT}	–1.0	+4.6	V
Power supply voltage	V_{CC},V_{CCQ}	–1.0	+4.6	V
Storage temperature (plastic)	T_{STG}	–55	+150	°C
Power dissipation	P_D	–	1	W
Short circuit output current	I_{OUT}	–	50	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specificati on is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance: CLK	C_{i1}	2.5	4	pF	1, 2, 3
Input capacitance: All other input-only pins	C_{i2}	2.5	5	pF	1, 2, 4
Input/output capacitance	$C_{I/O}$	4.0	6.5	pF	1, 2, 5

Notes
1 This parameter is sampled. V_{CC} = V_{CCQ} = 3.3V; f = 1MHz; T_A = 23° C; pin under test biased at 1.4V.
2 Max value is specified for –10, –10F, and –8.
3 For –75 part, Max = 3.5 pF.
4 For –75 part, Max = 3.8 pF.
5 For –75 part, Max = 6.0 pF.

I_{DD} specifications and conditions
(0° C ≤ T_A ≤ 70° C, V_{DD}, V_{DDQ} = +3.3V ± 0.3V)

Parameter		Symbol	Max –75	Max –8	Max –10F/10	Units	Notes
Operating current: active mode; burst = 2; READ or WRITE; t_{RC} = t_{RC}(min); CAS latency = 3		I_{DD1}	115	95	95	mA	4, 5
Standby current: power-down mode; all banks idle; CKE = low		I_{DD2}	2	2	2	mA	4,5
Standby current: active mode; CKE = high; CS# = high; all banks active after t_{RCD} met; no accesses in progress		I_{DD3}	45	35	35	mA	4, 5
Operating current: burst mode; continuous burst; READ or WRITE; all banks active; CAS latency = 3		I_{DD4}	140	130	120	mA	4,5
Auto refresh current: CKE = high; CS# = high	t_{RFC} = t_{RFC}(min); CL = 3	I_{DD5}	210	210	190	mA	4, 5
	t_{RFC} = 15.625ms; CL = 3	I_{DD6}	50	50	40	mA	4,5
Self-refresh current: CKE ≤ 0.2V		I_{DD7}	1	1	1	mA	4,5

Notes

1 I_{DD} specifications are tested after proper initialization of the device.
2 I_{DD} is dependent on output loading and clock cycle time. Values are specified with minimum cycle time and outputs open.
3 I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V.
4 I_{DD} current will decrease at lower CAS latencies. This is because the lower the latency, the lower the clock cycle time.
5 Address transitions average one transition every two clock cycles.

AC parameters common to all waveforms

Sym	Parameter	$\overline{CAS}$ latency	-75		-8		-10F		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{RRD}	Row active to row active delay		15	–	20	–	20	–	20	–	ns	1
t_{RCD}	RAS to CAS delay time		20	–	20	–	20	–	30	–	ns	1
t_{RP}	Row precharge		20	–	20	–	20	–	30	–	ns	1
t_{RAS}	Row active		44	–	50	–	50	–	60	–	ns	1
tRC	Row cycle time		66	–	70	–	70	–	90	–	ns	1
t_{CDL}	Last data in to new column address delay		1	–	1	–	1	–	1	–	CLK	2
t_{RDL}	Last data in to row precharge		2	–	2	–	2	–	2	–	CLK	2
t_{BDL}	Last data in to burst stop		1	–	1	–	1	–	1	–	CLK	2
t_{CCD}	Column address to column address delay		1	–	1	–	1	–	1	–	CLK	3
t_{CK}	CLK cycle time	3	7.5	–	8	–	10	–	10	–	ns	4
		2	10	–	10	–	15	–	15	–		4
t_{AC}	CLK to valid output delay @ 50pF	3	5.4	–	6	–	6	–	6	–	ns	4,5,7
		2	6	–	6	–	6	–	6	–		4,5,7
t_{OH}	Output data hold time @ 50 pF	3	2.7	–	3	–	3	–	3	–	ns	4,5,7
		2	3	–	3	–	3	–	3	–		4,5,7
t_{CH}	CLK high pulse width		2.5	–	3	–	3	–	3	–	ns	6
t_{CL}	CLK low pulse width		2.5	–	3	–	3	–	3	–	ns	6
t_{AS}	Add setup time		1.5	–	2	–	2	–	2	–	ns	6
t_{AH}	Add hold time		0.8	–	1	–	1	–	1	–	ns	6
t_{SLZ}	CLK to output in low Z		1	–	1	–	1	–	1	–	ns	5
t_{SHZ}	CLK to output in high Z	3	–	6	–	7	–	7	–	7	ns	
		2	–	6	–	7	–	7	–	7		
t_{CKH}	CKE hold time		0.8	–	1	–	1	–	1	–	ns	
t_{CKS}	CKE setup time		1.5	–	2	–	2	–	2	–	ns	
t_{CMH}	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM hold time		0.8	–	1	–	1	–	1	–	ns	
t_{CMS}	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM setup time		1.5	–	2	–	2	–	2	–	ns	
t_{DH}	Data in hold time		0.8	–	1	–	1	–	1	–	ns	
t_{DS}	Data in setup time		1.5	–	2	–	2	–	2	–	ns	

AC parameters common to all waveforms (continued)

Sym	Parameter	CAS latency	-75		-8		-10 F		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{DQD}	DQM to input data delay		1	–	1	–	1	–	1	–	CLK	
t_{DQM}	DQM to data mast during writes		0	–	0	–	0	–	0	–	CLK	
t_{DQZ}	DQM to data high Z during reads		2	–	2	–	2	–	2	–	CLK	
t_{DWD}	Write command to input data delay		0	–	0	–	0	–	0	–	CLK	
t_{DAL}	Data-in to active command		5	–	5	–	5	–	5	–	CLK	
t_{MRD}	Load mode register to active/ refresh command		1	–	1	–	1	–	1	–	CLK	
t_{ROH}	Data-out high Z from precharge/burst stop command	3	3	–	3	–	3	–	3	–	CLK	4
		2	2	–	2	–	2	–	2	–	CLK	4
t_{CKED}	CKE to CLOCK disable or power-down entry mode		1	–	1	–	1	–	1	–	CLK	
t_{PED}	CKE to clock enable or power-down exit mode		1	–	1	–	1	–	1	–	CLK	

Notes

1 Minimum clock cycles = (Minimum time / clock cycle time) rounded up.
2 Minimum delay required to complete write.
3 Column address change allowed every cycle.
4 Parameters dependent on CAS latency.
5 If clock rising time > 1ns, (tr/2-0.5)ns should be added to parameter.
6 If (tr and tf) > 1ns, [(tr+tf)/2-1]ns should be added to parameter.
7 Outputs measured at 1.5V with 50pF load only without resistive termination.

Burst sequence (BL = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Burst sequence (BL = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

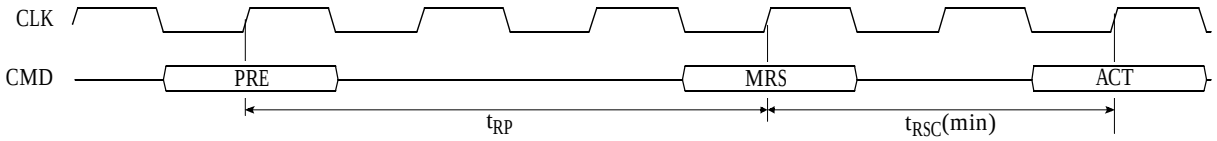
Device operation

Command	Pin settings	Description
Power up		The following sequence must be performed prior to normal operation. 1. Apply power, start clock, and assert CKE and DQM high. All other signals are NOP. 2. After power-up, pause for a minimum of 200µs. CKE/DQM = high; all others NOP. 3. Precharge both banks. 4. Perform Mode Register Set command to initialize mode register. 5. Perform a minimum of 8 auto refresh cycles to stabilize internal circuitry. (Steps 4 and 5 may be interchanged.)
Mode register set	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = low; A0~A11 = opcode	The mode register stores the user selected opcode for the SDRAM operating modes. The $\overline{CAS}$ latency, burst length, burst type, test mode and other vendor specific functions are selected/programmed during the Mode Register Set command cycle. The default setting of the mode register is not defined after power-up. The power-up and mode register set cycle must be executed prior to normal SDRAM operation. Refer to the Mode Register Set table and timing for details.
Device deselect and no operation	$\overline{CS}$ = high	The SDRAM performs a "no operation" (NOP) when $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ = high. Since the NOP performs no operation, it may be used as a wait state in performing normal SDRAM functions. The SDRAM is deselected when CS is high. CS high disables the command decoder such that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address inputs are ignored. Device deselection is also considered a NOP.
Bank activation	$\overline{CS}$ = $\overline{RAS}$ = low; $\overline{CAS}$ = $\overline{WE}$ = high; A0~A10 = row address; BA0~BA1 = bank select	The SDRAM is configured with four internal banks. Use the Bank Activate command to select a row in one of the idle banks. Initiate a read or write operation after t_{RCD}(min) from the time of bank activation.
Burst read	$\overline{CS}$ = $\overline{CAS}$ = A10 = low; $\overline{RAS}$ = $\overline{WE}$ = high; BA0~BA1 = bank select, A0~A8 = column address; (A9 = don't care for 8M×8; A8,A9 = don't care for 4M×16)	Use the Burst Read command to access a consecutive burst of data from an active row in an active bank. Burst read can be initiated on any column address of an active row. The burst length, sequence and latency are determined by the mode register setting. The first output data appears after the $\overline{CAS}$ latency from the read command. The output goes into a high impedance state at the end of the burst (BL = 1,2,4,8) unless a new burst read is initiated to form a gapless output data stream. Terminate the burst with a burst stop command, precharge command to the same bank or another burst read/write.
Burst write	$\overline{CS}$ = $\overline{CAS}$ = $\overline{WE}$ = A10 = low; RAS = high; A0~A9 = column address; (A9 = don't care for 8M×8; A8,A9 = don't care for 4M×16)	Use the Burst Write command to write data into the SDRAM on consecutive clock cycles to adjacent column addresses. The burst length and addressing mode is determined by the mode register opcode. Input the initial write address in the same clock cycle as the Burst Write command. Terminate the burst with a burst stop command, precharge command to the same bank or another burst read/write.
UDQM/LDQM (×16), DQM (×8) operation		Use DQM to mask input and output data on a cycle-by-cycle basis. It disables the output buffers in a read operation and masks input data in a write operation. The output data is invalid 2 clocks after DQM assertion (2 clock latency). Input data is masked on the same clock as DQM assertion (0 clock latency).

Device operation (continued)

Command	Pin Settings	Description
Burst stop	$\overline{CS}$ = $\overline{WE}$ = low; $\overline{RAS}$ = $\overline{CAS}$ = high	Use burst stop to terminate burst operation. This command may be used to terminate all legal burst lengths.
Bank precharge	$\overline{CS}$ = A10 = $\overline{RAS}$ = $\overline{WE}$ = low; $\overline{CAS}$ = high; A11 = bank select; A0~A9 = don't care	The Bank Precharge command precharges the bank specified by BA0 and BA1. The precharged bank is switched from active to idle state and is ready to be activated again. Assert the precharge command after t_{RAS}(min) of the bank activate command in the specified bank. The precharge operation requires a time of t_{RP}(min) to complete.
Precharge all	$\overline{CS}$ = $\overline{RAS}$ = $\overline{WE}$ = low; $\overline{CAS}$ = A10 = high; BA0~BA1 = bank select; A0~A9 = don't care	The Precharge All command precharges all four banks simultaneously. All four banks are switched to the idle state on precharge completion.
Auto precharge	$\overline{CS}$ = $\overline{CAS}$ = $\overline{WE}$ (write) = low; $\overline{RAS}$ = $\overline{WE}$ (read) = A10 = high; BA0~BA1 = bank select; A0~A9 = column address; (A9 = don't care for 2M×8; A8,A9 = don't care for 1M×16)	During auto precharge, the SDRAM adjusts internal timing to satisfy t_{RAS}(min) and t_{RP} for the programmed CAS latency and burst length. Couple the auto precharge with a burst read/write operation by asserting A10 to a high state at the same time the burst read/write commands are issued. At auto precharge completion, the specified bank is switched from active to idle state. Note that no new commands to the bank can be issued until the specified bank achieves the idle state. Auto precharge doesn't work with full-page burst.
Clock suspend/power down mode entry	CKE = low	When CKE is low, the internal clock is frozen or suspended from the next clock cycle and the state of the output and burst address are frozen. If all banks are idle and CKE goes low, the SDRAM enters power down mode at the next clock cycle. When in power down mode, no input commands are acknowledged as long as CKE remains low. To exit power down mode, raise CKE high before the rising edge of CLK.
Clock suspend/power down mode exit	CKE = high	Resume internal clock operation by asserting CKE high before the rising edge of CLK. Subsequent commands can be issued one clock cycle after the end of the Exit command.
Auto refresh	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = low; $\overline{WE}$ = CKE = high; A0~A11 = don't care	SDRAM storage cells must be refreshed every 64ms to maintain data integrity. Use the Auto Refresh command to refresh all rows in all banks of the SDRAM. The row address is provided by an internal counter which increments automatically. Auto refresh can only be asserted when all four banks are idle and the device is not in the power down mode. The time required to complete the auto refresh operation is t_{RC}(min). Use NOPs in the interim until the auto refresh operation is complete. This is the most common refresh mode. It is typically performed once every 15.6us or in a burst of 4096 auto refresh cycles every 64ms. All four banks will be in the idle state after this operation.
Self refresh	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = CKE = low; WE = high; A0~A11 = don't care	Self refresh is another mode for refreshing SDRAM cells. In this mode, refresh address and timing are provided internally. Self refresh entry is allowed only when all four banks are idle. The internal clock and all input buffers with the exception of CKE are disabled in this mode. Exit self refresh by restarting the external clock and then asserting CKE high. NOP's must follow for a time of t_{RC}(min) for the SDRAM to reach the idle state where normal operation is allowed. If burst auto refresh is used in normal operation, burst 4096 auto refresh cycles immediately after exiting self refresh.

Mode register set command waveform

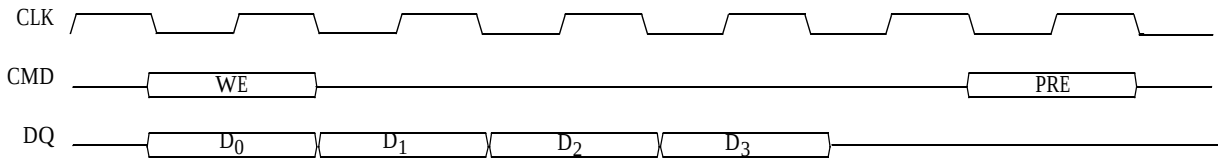


MRS can be issued only when both banks are idle.

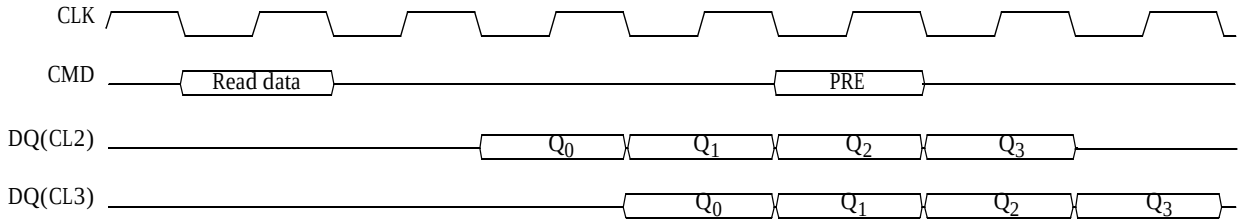
Precharge waveforms

Precharge can be asserted after t_{RAS} (min). The selected bank will enter the idle state after t_{RP}. The earliest assertion of the precharge command without losing any burst data is show below.

(normal write; BL = 4)



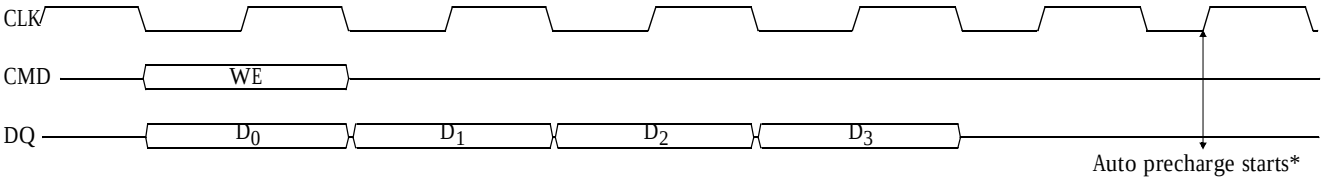
(normal read; BL = 4)



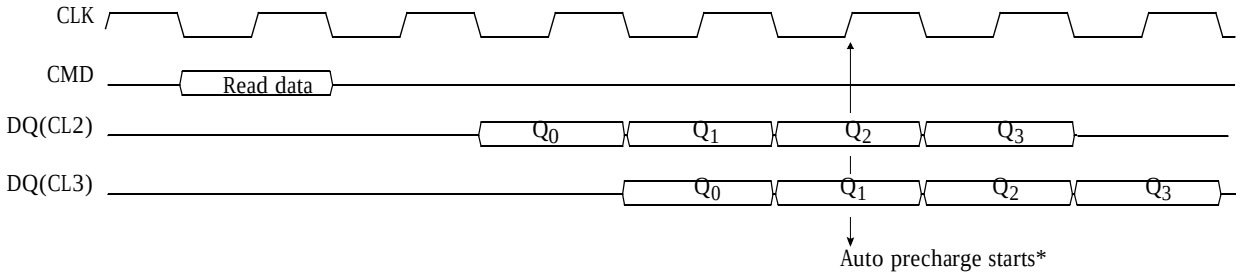
Auto precharge waveforms

A10 controls the selection of auto precharge during the read or write command cycle.

(write with auto precharge; BL = 4)



(read with auto precharge; BL = 4)

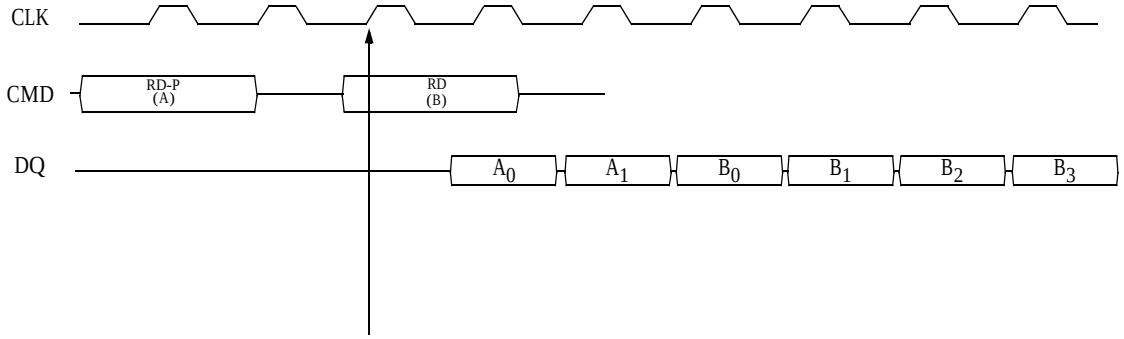


* The row active command of the precharge bank can be issued after t_{RP} from this point. At burst read/write with auto precharge, CAS interrupt of the same bank is illegal; other bank is described below.

Concurrent Auto-P Waveforms

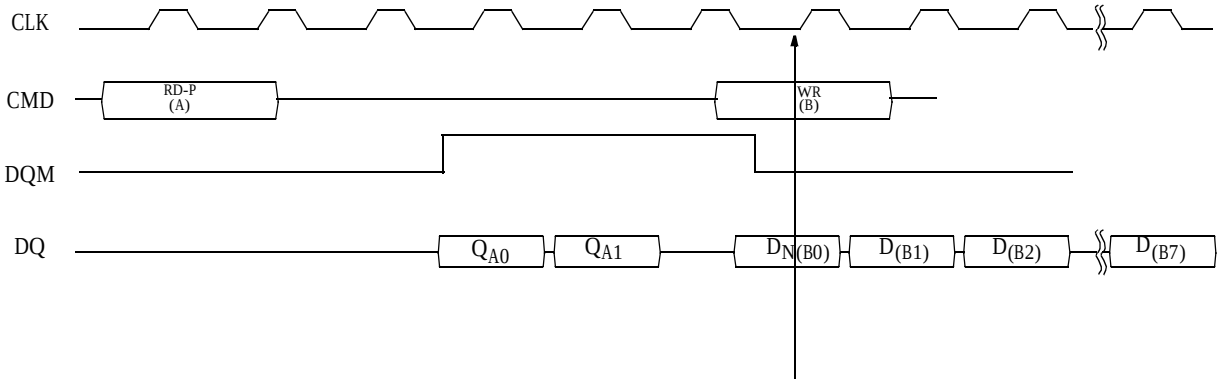
According to Intel™'s specification, auto-p burst interruption is allowed by another burst provided that the interrupting burst is in a different bank than the ongoing burst.

(A) RD-P interrupted by RD in another bank (CL = 3, BL = 4)



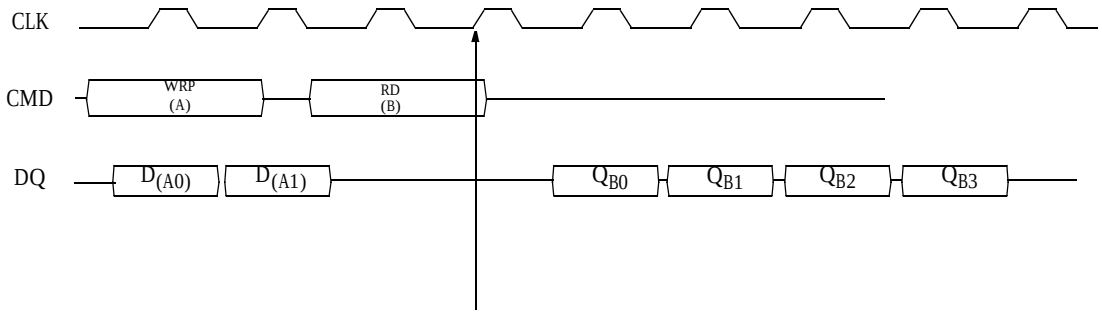
Bank A Precharge Starts *

(B) RD-P interrupted by WR in another bank (CL = 2, BL = 8)



Bank A Precharge Starts *

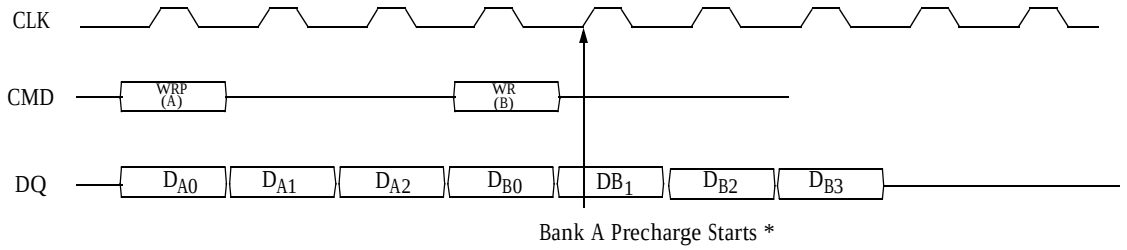
(C) WR-P interrupted by RD in another bank (CL = 2, BL = 4)



Bank A Precharge Starts *

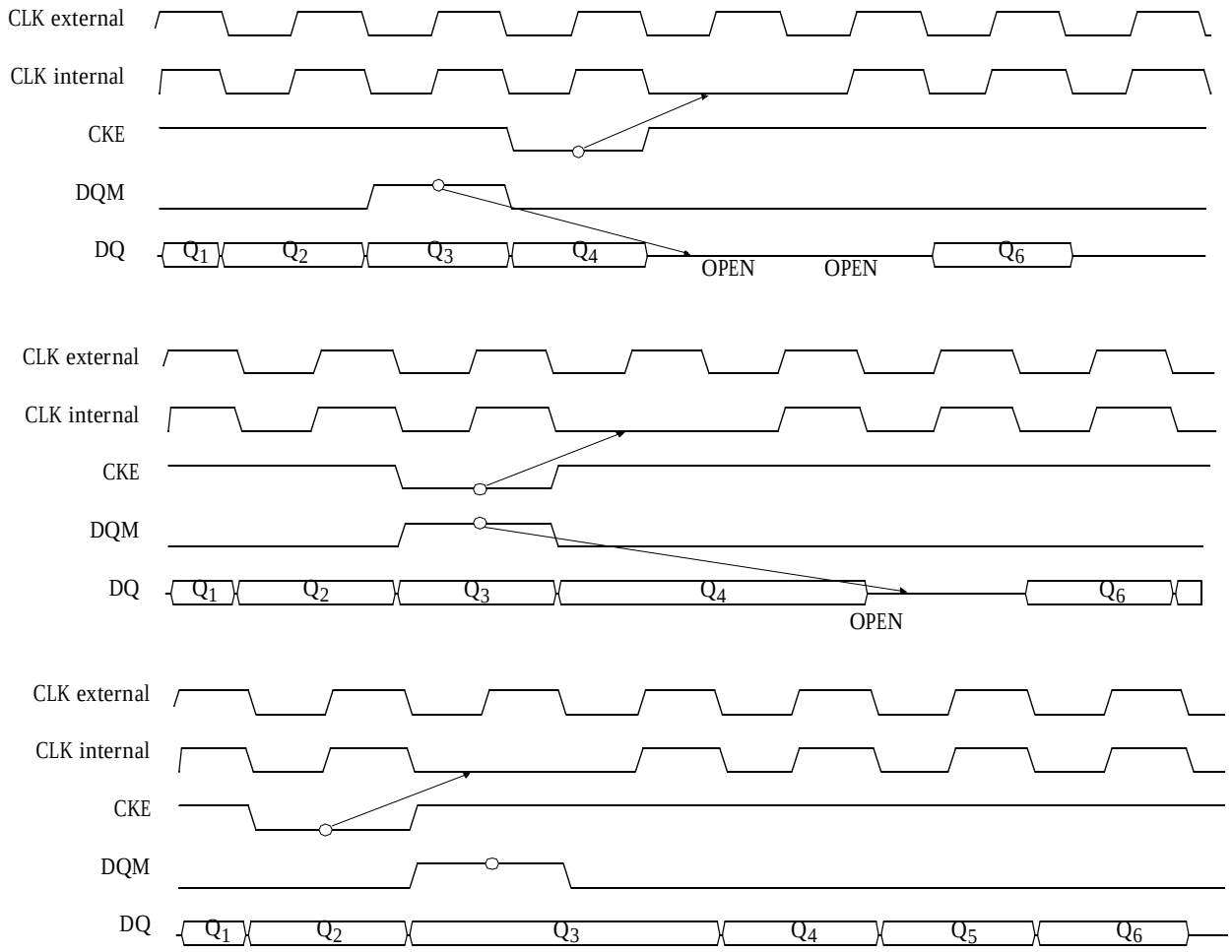
* The row active command of the precharge bank can be issued after t_{RP} from this point.

(D) WR-P Interrupted by WR in another bank (CL = 3, BL = 4)

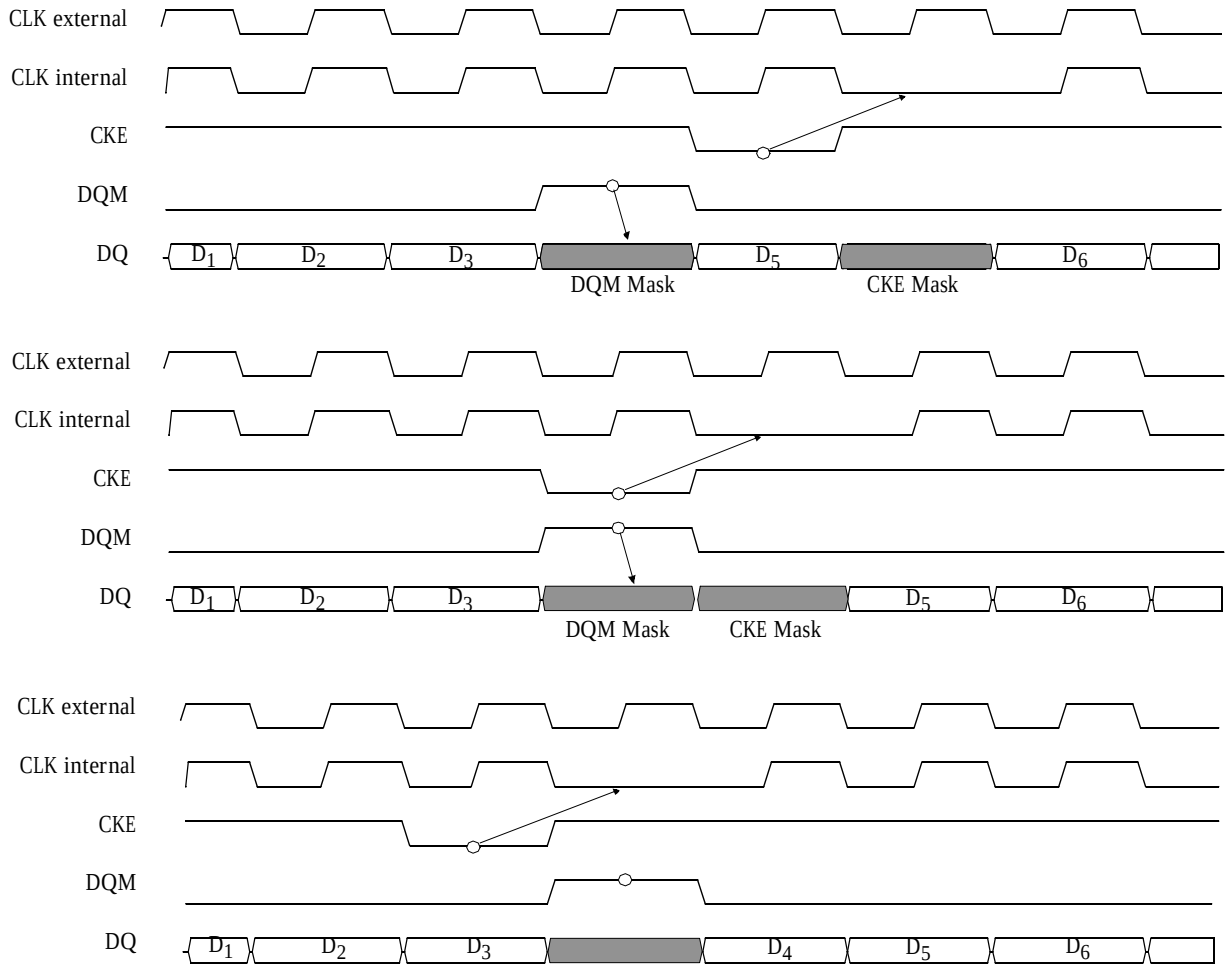


* The row active command of the precharged bank can be issued after t_{RP} from this point.

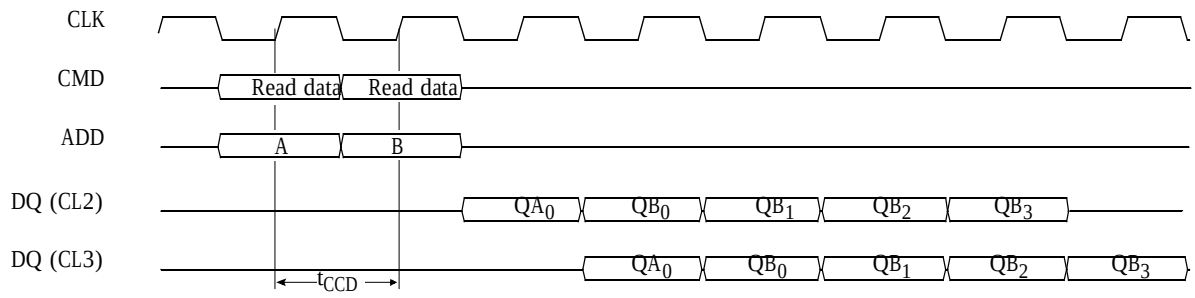
Clock suspension read waveforms (BL = 8)



Clock suspension write waveforms (BL = 8)

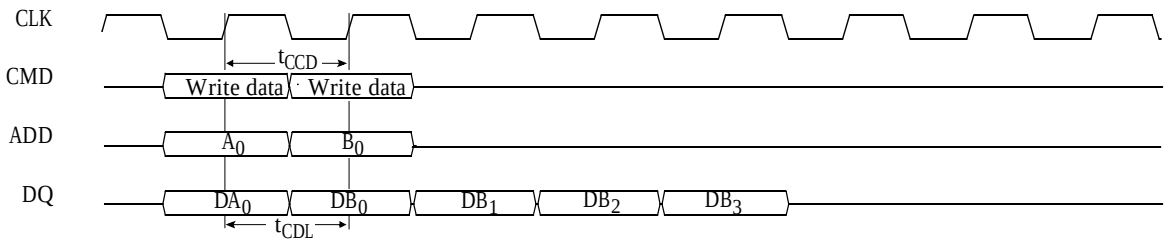


Read/write interrupt timing read interrupted by read (CL = 2, BL = 4)



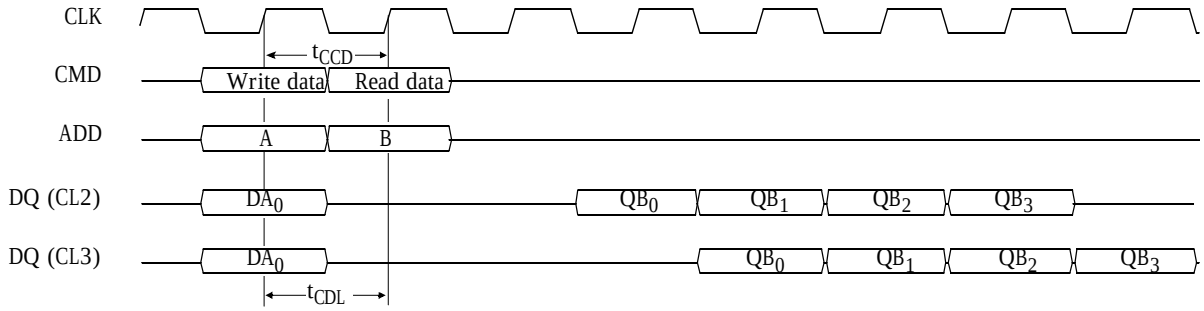
t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)

write interrupted by write (BL = 4)



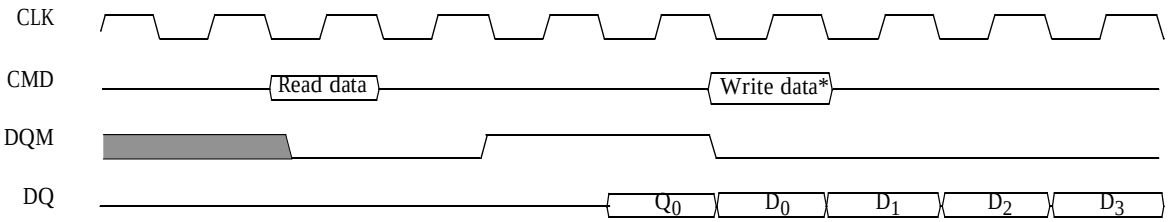
t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)
t_{CDL} = last address in to new column addres delay (= 1 CLK)

write interrupted by read (CL = 2, BL = 4)



t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)
t_{CDL} = last address in to new column addres delay (= 1 CLK)

read interrupted by write (CL = 3, BL = 4)

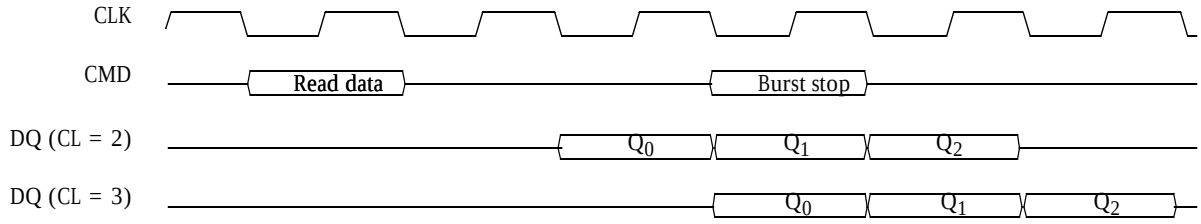


* To prevent bus contention, maintain a gap between data in and data out.

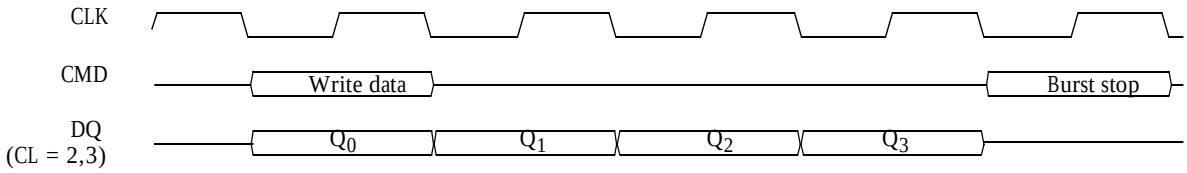
Burst termination

Burst operations may be terminated with a Read, Write, Burst Stop, or Precharge command. When Burst Stop is asserted during the read cycle, burst read data is terminated and the data bus goes to High Z after $\overline{CAS}$ latency. When Burst Stop is asserted during the write cycle, burst write data is terminated and the databus goes to High Z simultaneously.

Burst stop command waveform, read cycle (BL = 8)



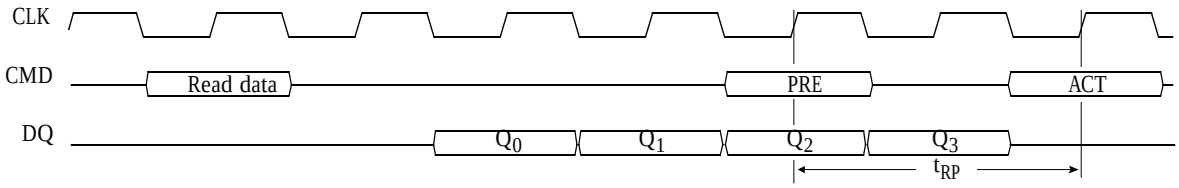
write cycle



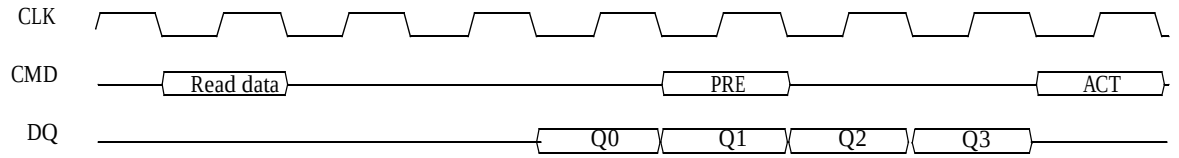
Precharge command

A Precharge command can be used to interrupt burst read/write operation during the read cycle. During RD, burst read is terminated and o/p goes to High Z after $\overline{CAS}$ latency. The same bank can be activated after t_{RP}. During write, burst write operation is terminated immediately. Data written two cycles prior to the precharge command will be correctly stored. Set DQM high one cycle before Precharge command and hold it high until Precharge command to mask and avoid writing invalid data.

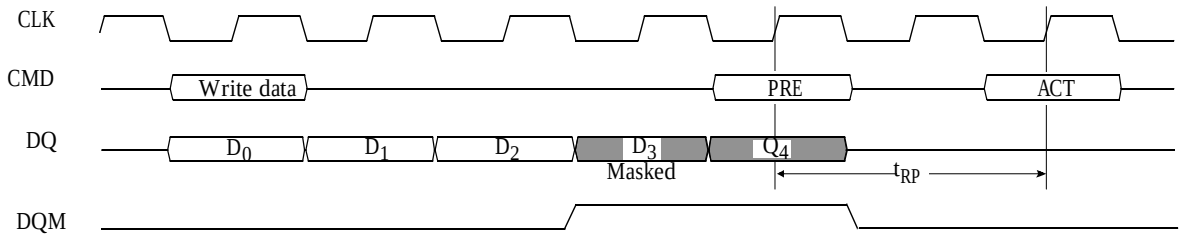
read cycle (CL = 2)



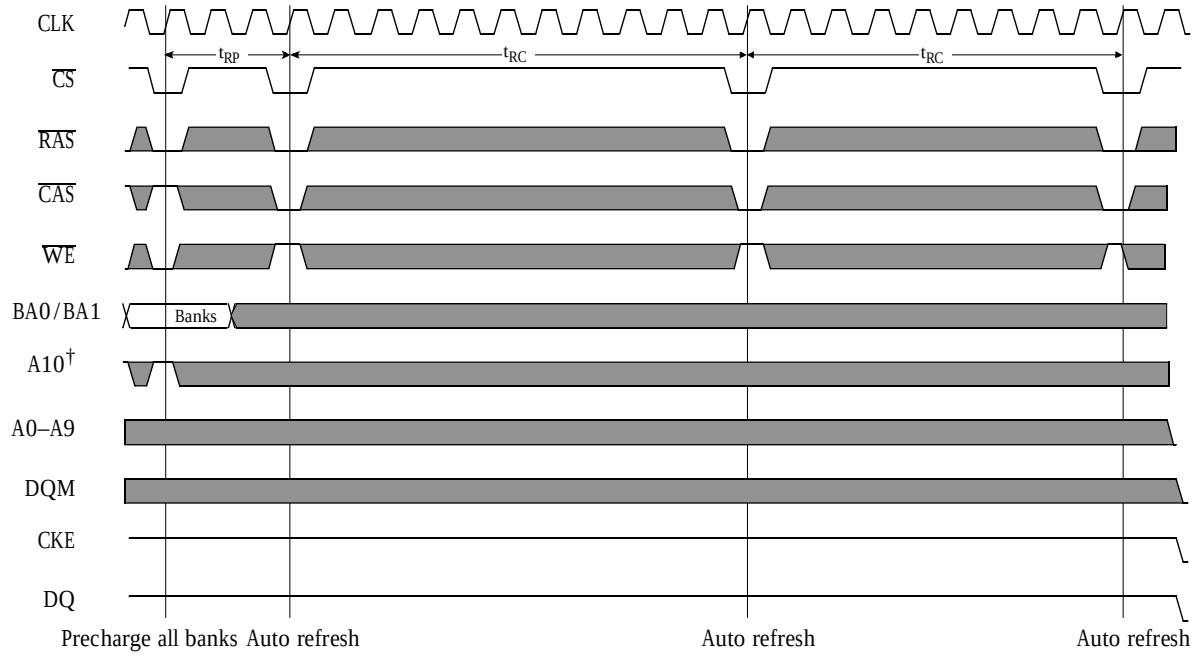
read cycle (CL = 3)



write cycle (BL = 8)

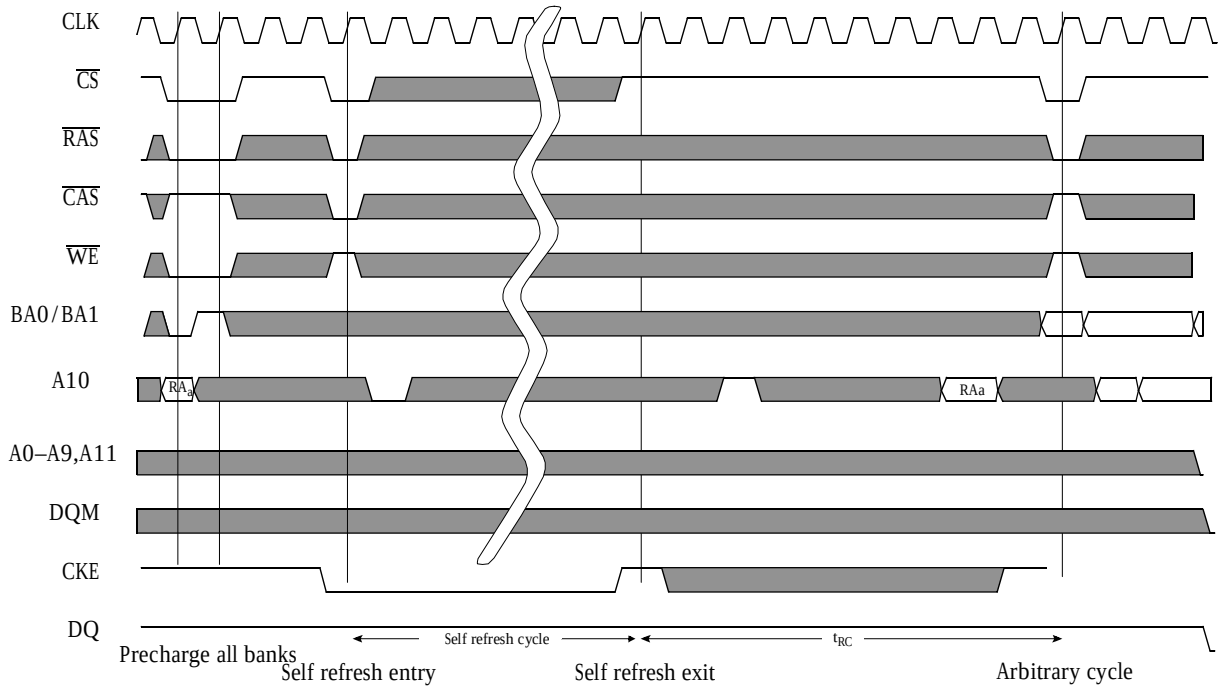


Auto refresh waveform

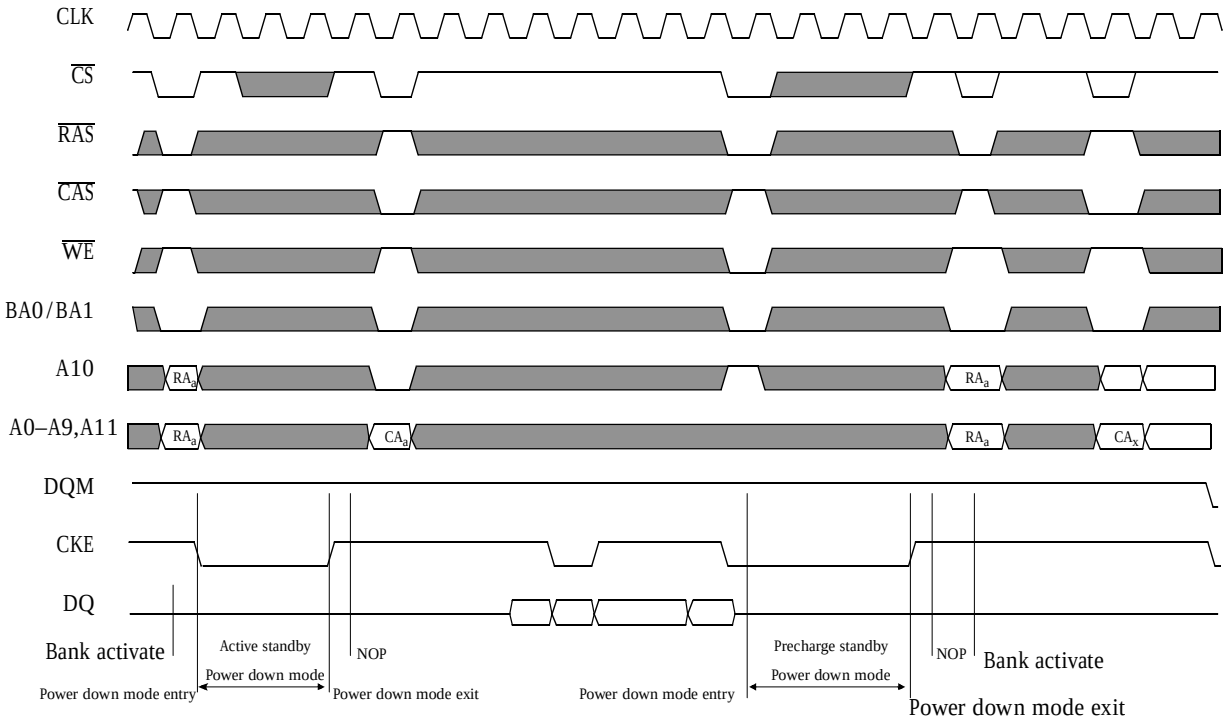


† If A10 = High, then BA0/BA1 = don't care; if A10 = low, then BA0/BA1 = bank select.

Self refresh waveform

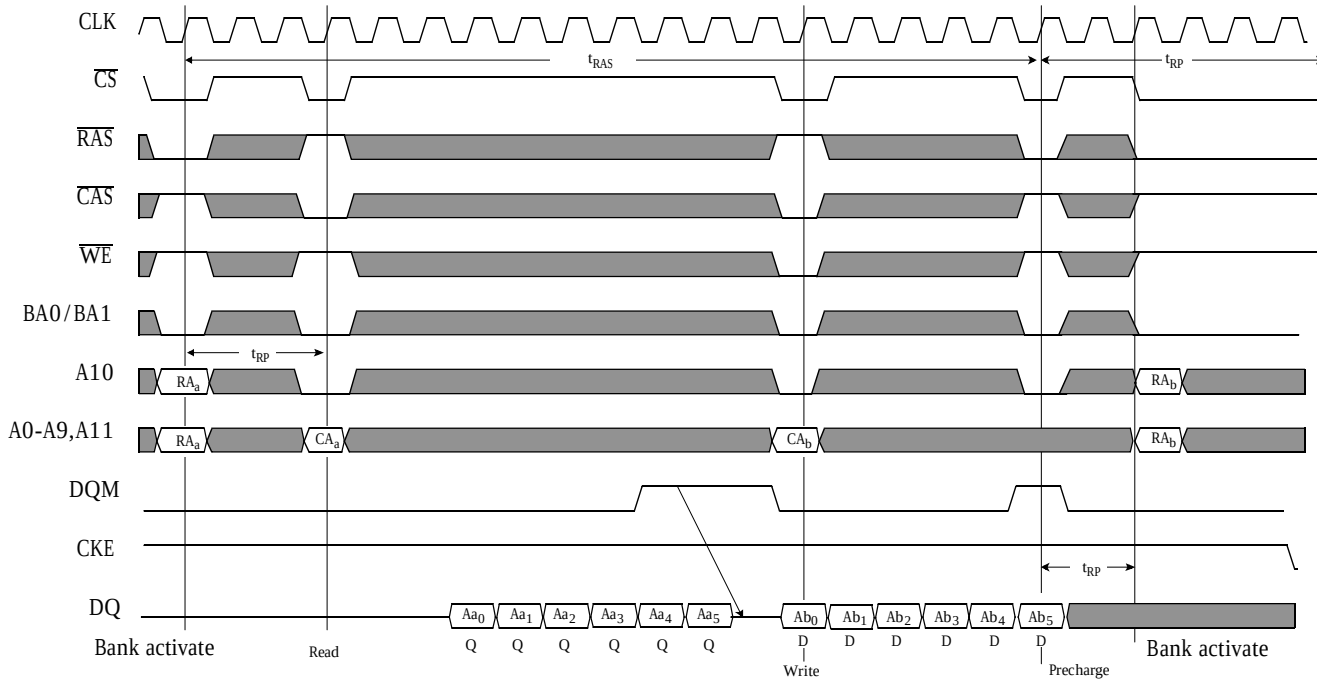


Power down mode waveform

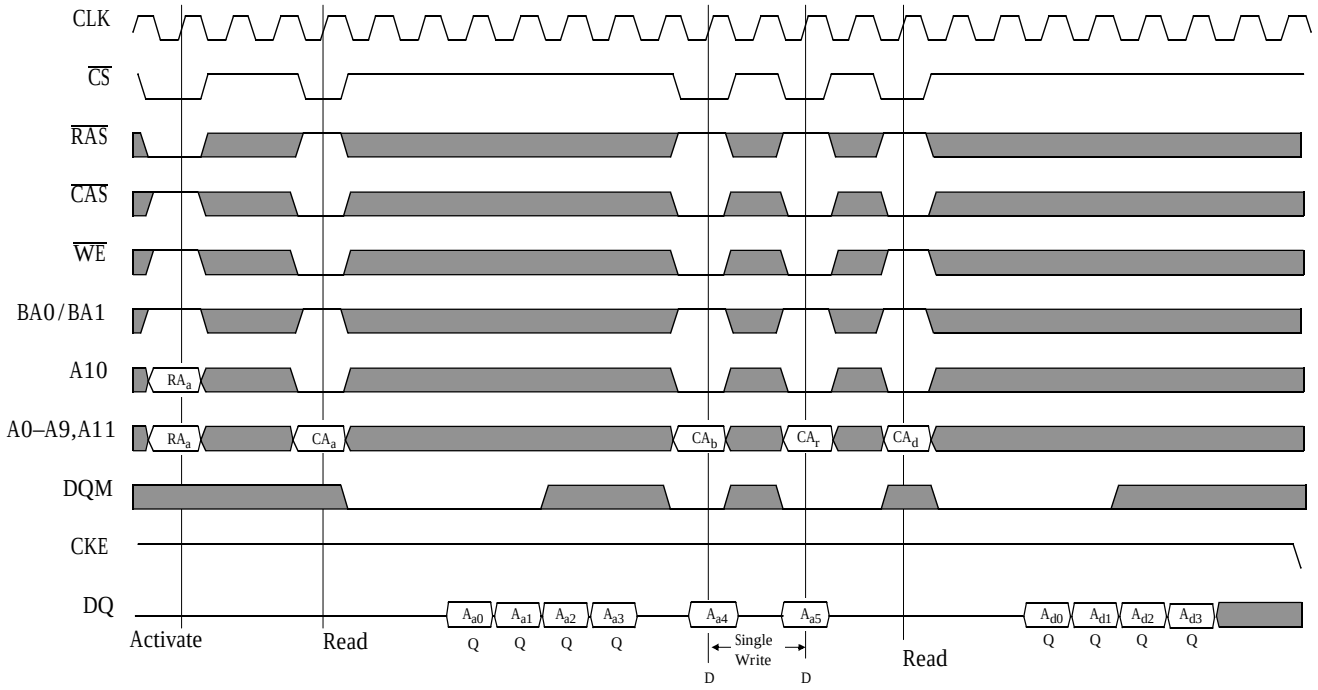


Enter power down mode by pulling CKE low.
All input/output buffers (except CKE buffer are turned off in power down mode.
When CKE goes high, command input must be equal to no operation at next CLK rising edge.

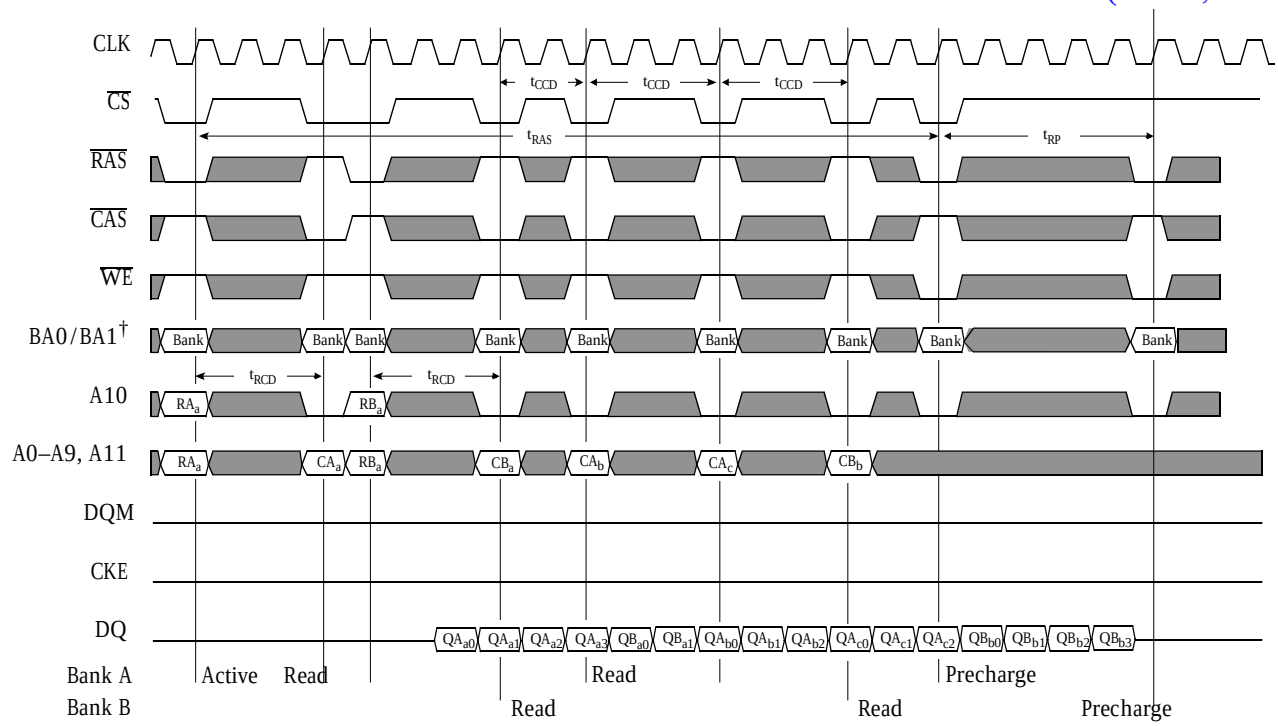
Read/write waveform (BL = 8, CL = 3)



Burst read/single write waveform (BL = 4, CL = 3)

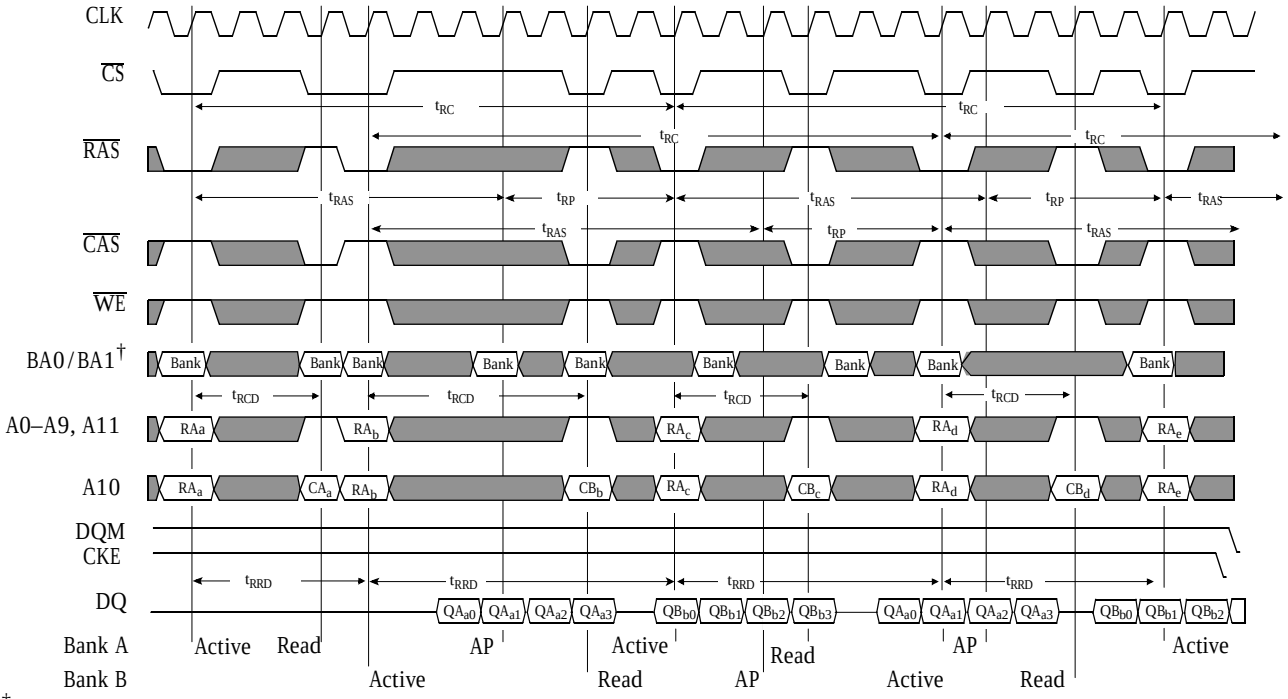


Interleaved bank read waveform (BL = 4, CL = 3)



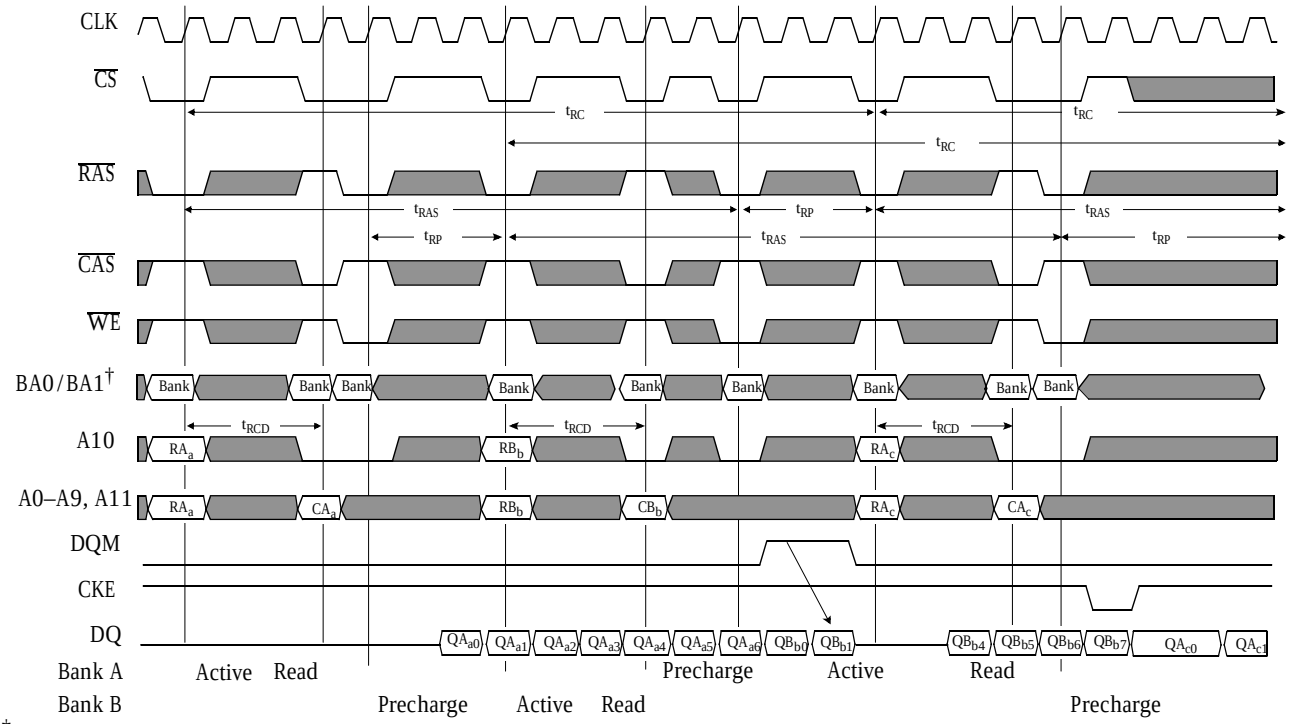
† BA0 and BA1 together determine which bank undergoes operations.

Interleaved bank read waveform (BL = 4, CL = 3, Autoprecharge)



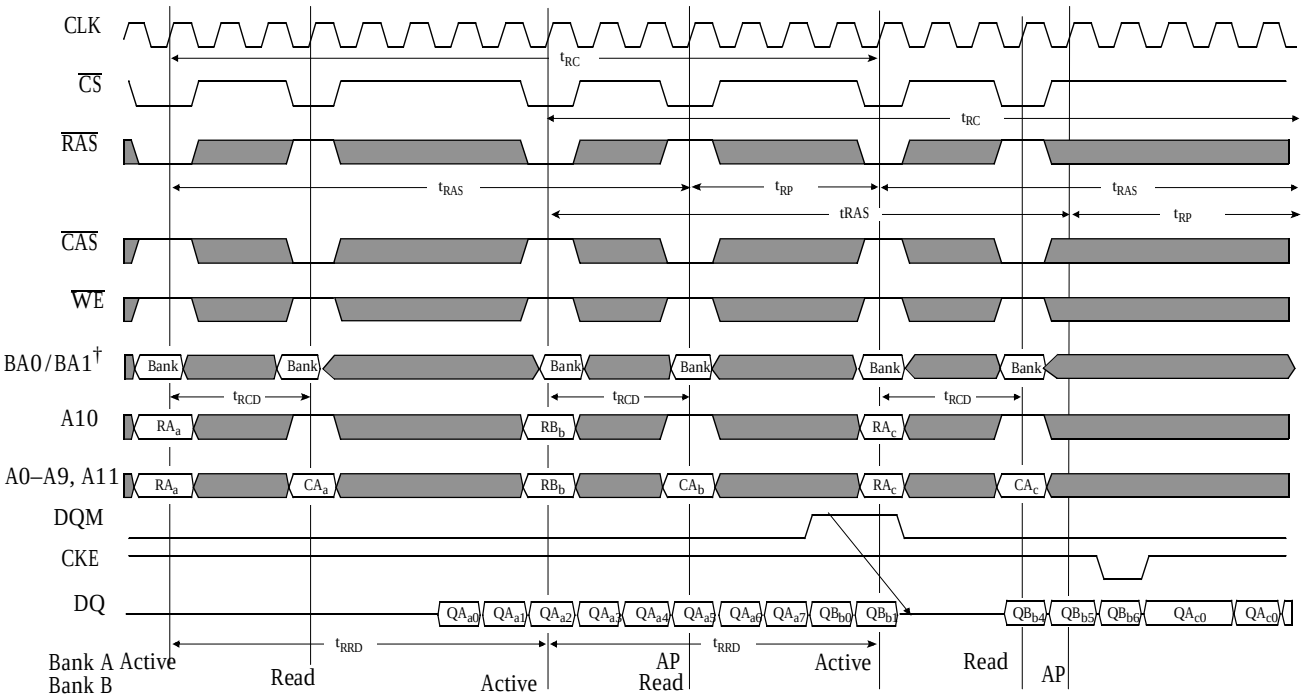
†BA0 and BA1 together determine which bank undergoes operations. AP = internal precharge begins.

Interleaved bank read waveform (BL = 8, CL = 3)



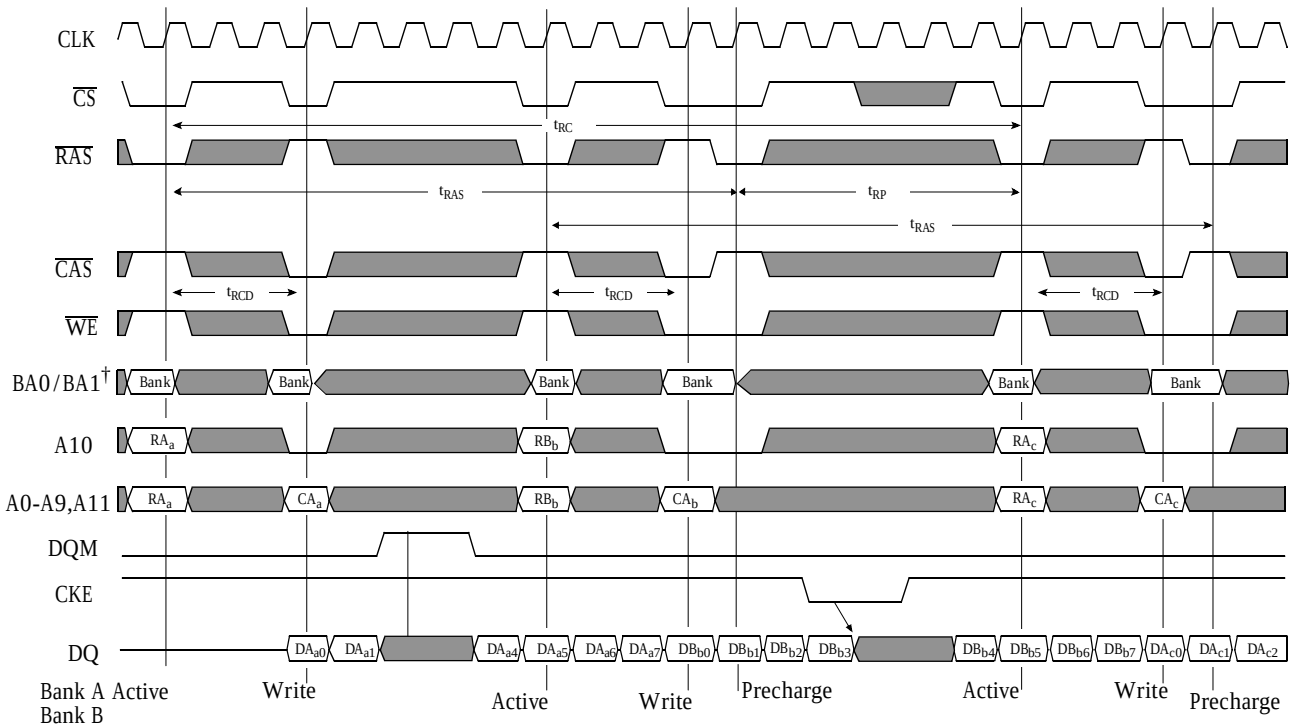
†BA0 and BA1 together determine which bank undergoes operations.

Interleaved bank read waveform (BL = 8, CL = 3, Autoprecharge)



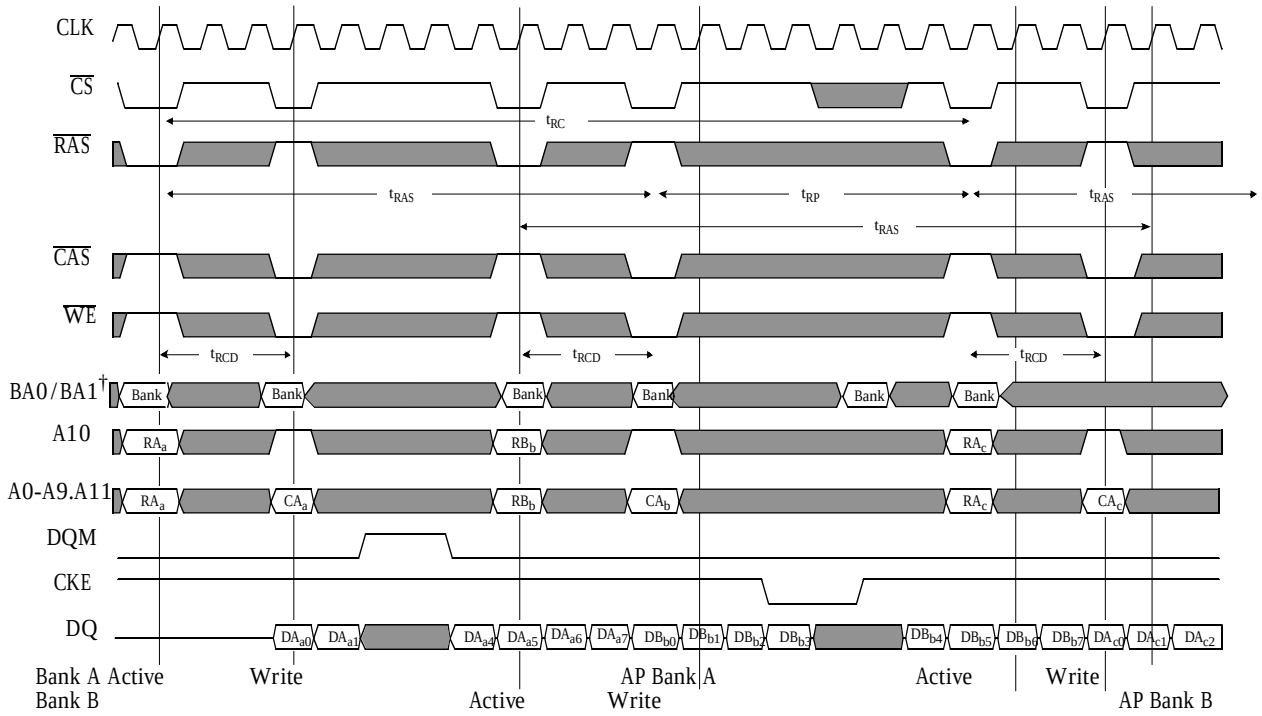
† BA0 and BA1 together determine which bank undergoes operations. AP = internal precharge begins.

Interleaved bank write waveform (BL = 8)



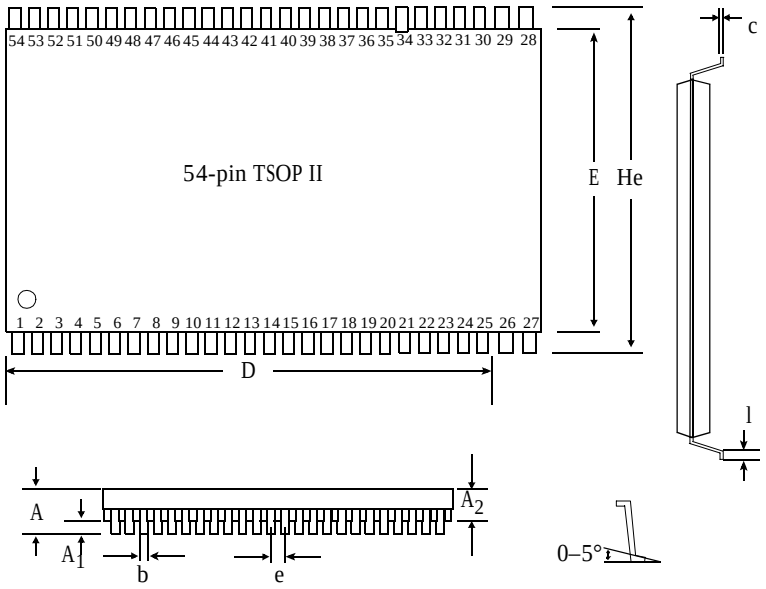
† BA0 and BA1 together determine which bank undergoes operations.

Interleaved bank write waveform (BL = 8, Autoprecharge)



† BA0 and BA1 together determine which bank undergoes operations. AP = internal precharge begins

Package dimensions



	54-pin TSOP II	
	Min (mm)	Max (mm)
A	–	1.2
A_1	0.05	–
A_2	0.95	1.05
b	0.30	0.45
c	0.12	0.21
D	22.12	22.32
E	10.03	10.29
e	0.80 (typical)	
H_e	11.56	11.96
l	0.40	0.60

AC test conditions

- Input reference levels of VIH = 2.0V and VIL = 0.8V
- Output reference levels = 1.4V
- Input rise and fall times: 2 ns

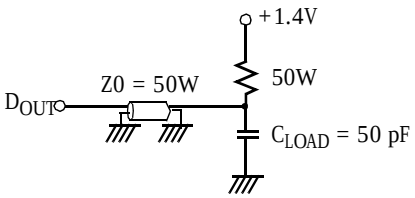


Figure A: Equivalent output load

Ordering information

Part	–75	–8	–10	–10F
TSOP II, 400 mil, 54-pin	AS4LC8M8S0-75TC	AS4LC8M8S0-8TC	AS4LC8M8S0-10TC	AS4LC8M8S0-10FTC
TSOP II, 400 mil, 54-pin	AS4LC4M16S0-75TC	AS4LC4M16S0-8TC	AS4LC4M16S0-10TC	AS4LC4M16S0-10FTC

Part numbering system

AS4	LC	XXXS0	–XX	T	C
DRAM prefix	LC = 3.3V CMOS	Device number for synchronous DRAM	1/frequency	Package (device dependent): TSOP II 400 mil, 54 pin	Commercial temperature range, 0° C to 70 ° C