

**STRUCTURE** Silicon Monolithic Integrated Circuit  
**PRODUCT SERIES** Dual Power Amp. for Stereo Radio Cassette Recorders  
**TYPE** BA5412  
**PACKAGE OUTLINES** Figure 1 (Plastic Mold)  
**BLOCK DIAGRAM** Figure 2  
**FUNCTION**

- High output power.
  - Pout= 5.4W (Vcc=12V, RL=3Ω, THD=10%)
  - Pout= 2.5W (Vcc= 9V, RL=4Ω, THD=10%)
- Excellent tone quality.
  - THD = 0.09% (f=1kHz, Po=0.5W)
  - VNO = 0.3mVrms (Rg=10kΩ)
  - RR = 60dB (fRR=100Hz)
- Wide supply voltage range.
  - Vcc = 5.0 ~ 18.0 V
- Minimal power-on/off pop noise.
- Built-in protective circuit against ripple of starting motor.
- Built-in thermal-shut-down.
- Built-in Stand-by switch.
- Unchanged starting time against supply voltage.
- Soft-clip.
- Useless heat sink. (Vcc=9V, RL≥4Ω)

### Absolute Maximum Ratings (Ta=25°C)

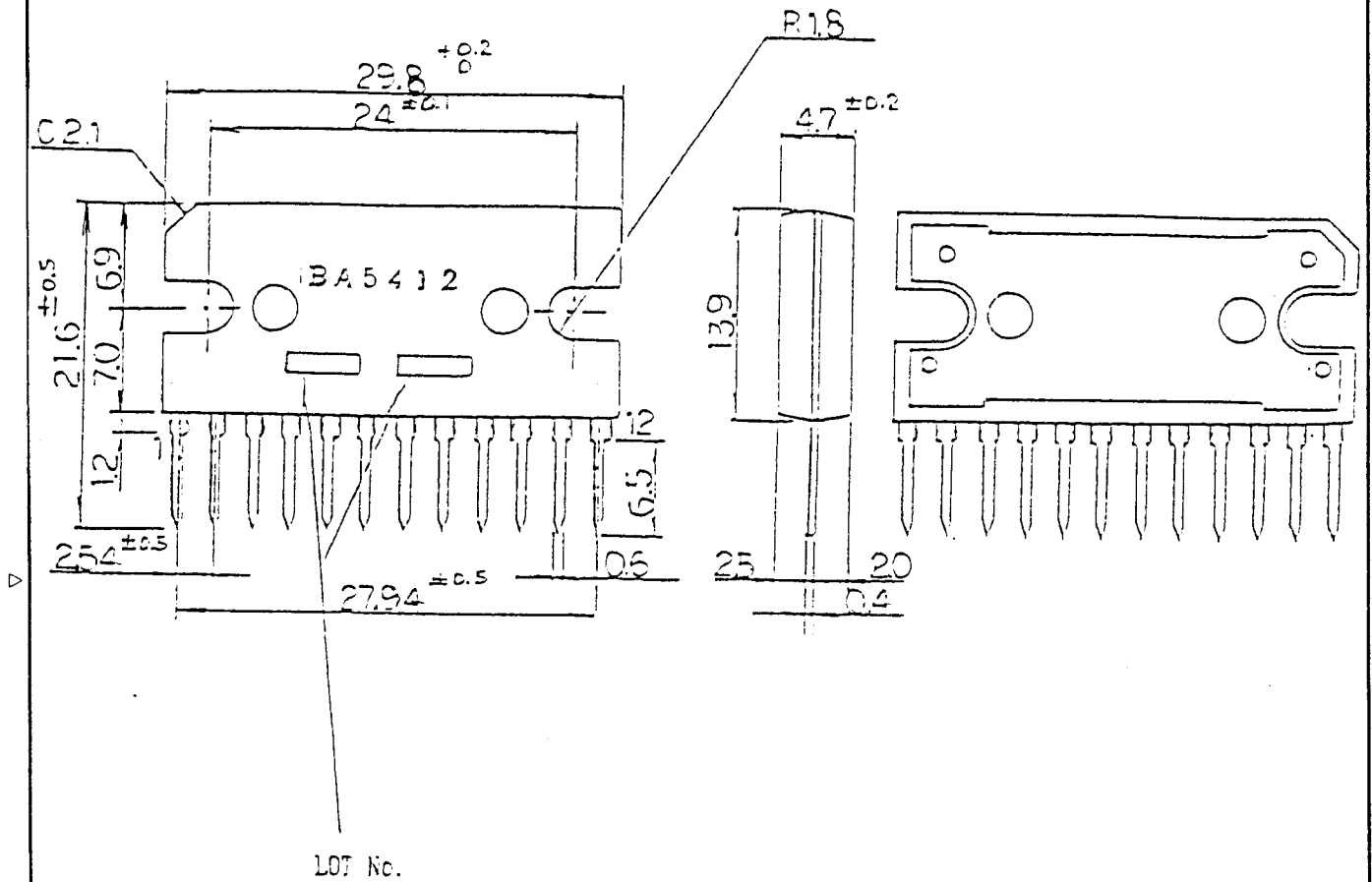
Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	※1 24	V
Power Dissipation	Pd	※2 20 ※3 4.0	W
Operating Temperature Range	Topr	-25 ~ +75	°C
Storage Temperature range	Tstg	-55 ~ +150	°C

- ※1 Inside of AS0. (Fig.10)
- ※2 Back-metal temperature 75°C. (Fig.12)
- ※3 Derating is done at 40mW/°C for operation above Ta=25°C. (Without heat sink.)

Recommended Operating Supply Voltage Range : Vcc = 5.0 ~ 18.0 V

ROHM assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

Design	Check	Approval	MAR / 16 / '90	Specification
<i>K. Nishitake</i>	<i>Y. Kimada</i>	<i>H. Kawakami</i>	Date	
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(Unit: mm)

Fig.1 Outline (Plastic Mold)

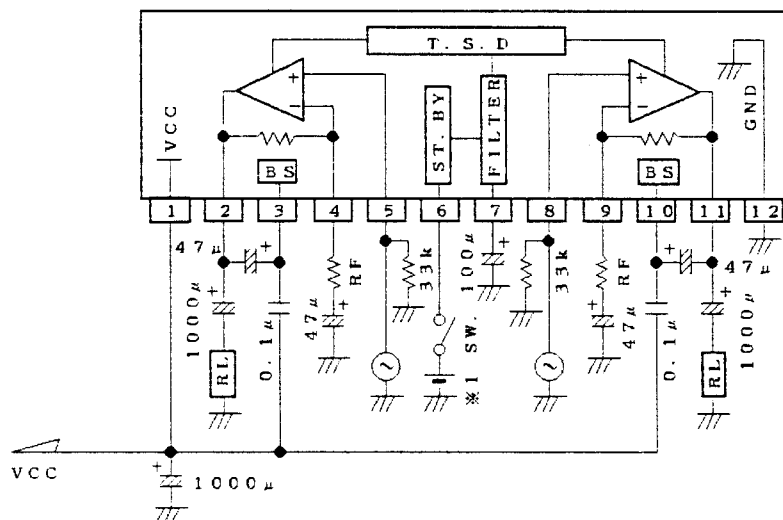
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## Electrical Characteristics

(Unless otherwise specified,  $T_a=25^\circ\text{C}$ ,  $V_{CC}=12\text{V}$ ,  $R_L=3\Omega$ ,  $R_F=240\Omega$ ,  $R_G=600\Omega$ ,  $f=1\text{kHz}$ , Test Cir.Fig.2)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Quiescent current	$I_Q$	—	28	45	mA	$V_{IN}=0\text{Vrms}$
Maximum output power	$P_{OM}$	—	8.3	—	W	$V_{IN}=-20\text{dBm}$
Rated output power 1	$P_{OUT1}$	4.5	5.4	—	W	THD=10%
Rated output power 2	$P_{OUT2}$	2.0	2.5	—	W	THD=10% $V_{CC}=9\text{V}$ $R_L=4\Omega$
Closed loop voltage gain	$G_{VC}$	43	45	47	dB	—
Output noise voltage	$V_{NO}$	—	0.3	1.0	mVrms	$R_G=10\text{k}\Omega$ DIN AUDIO
Total harmonic distortion	THD	—	0.09	1.0	%	$P_{OUT}=0.5\text{W}$
Ripple rejection ratio	RR	45	60	—	dB	$f_{RR}=100\text{kHz}$ $V_{RR}=-10\text{dBm}$
Crosstalk level	CT	45	60	—	dB	$V_O=0\text{dBm}$
Cir. current(ST.BY SW.off)	$I_{OFF}$	—	0	—	$\mu\text{A}$	—
ST.BY pin inflow current	$I_{SIN}$	—	0.3	—	mA	$V_{ST.BY}=V_{CC}$
Input bias current	$I_{BIN}$	—	0.1	0.5	$\mu\text{A}$	$R_G=0\Omega$

○ This product is not designed for protection against radioactive rays.



※1  $V_{ST.BY}=3\text{V}\sim V_{CC}$

Fig.2 Block Diagram & Test Circuit

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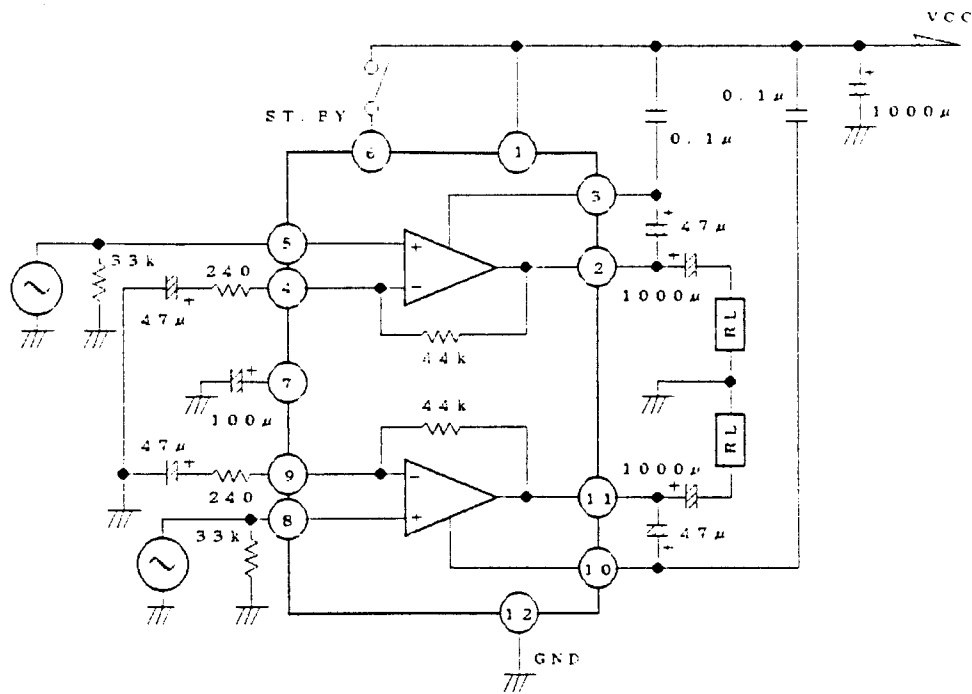


Fig.3 OTL Application Example

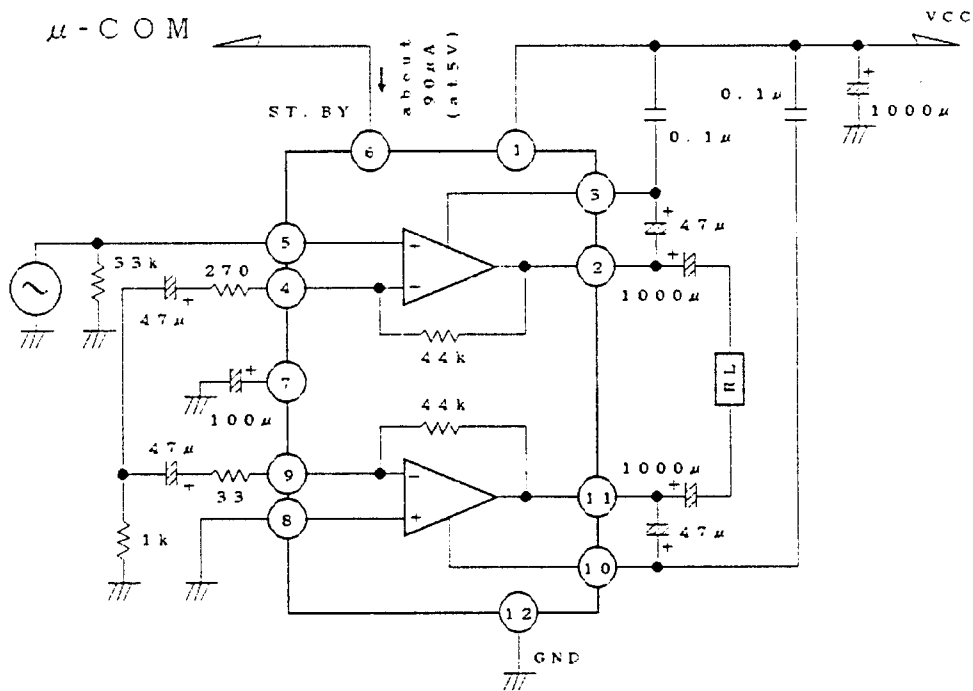


Fig.4 BTL Application Example

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## Notes for use

### 1. Input circuit

Fig.5 shows the input section circuit composition. No input coupling capacitor is required. But input coupling capacitor  $C_{IN}$  may be used to eliminate the noise from the volume due to up to  $0.5\mu A$  of bias current  $I_{BIN}$  generated from the input pin.

Input bias resistances are required. Therefore put input bias resistances ( $33k\Omega$  is recommended) between INPUT and GND.

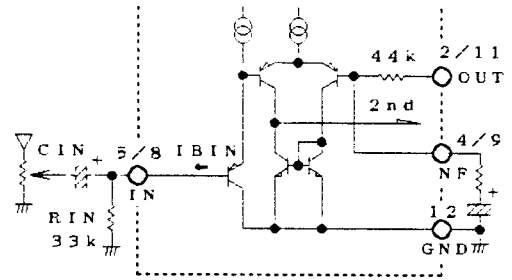


Fig.5

### 2. Gain adjustment

Gain  $G_V$  is obtained by the following equation.

$$G_V = 20 \text{ LOG } \frac{R_{NF} + R_F}{R_F}$$

$G_V$  can be reduced by increasing  $R_F$ . But  $G_V$  at 30 or more dB is recommendable since reduction in  $G_V$  increases the feedback facilitates oscillation.

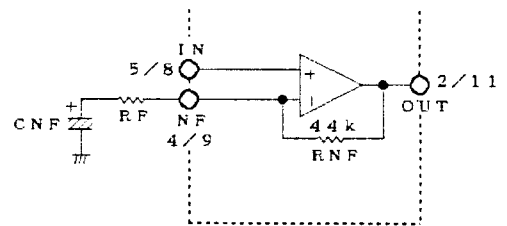


Fig.6

### 3. Oscillation preventive measures

It is recommendable to use a film capacitor with good temperature and high-frequency characteristics for oscillation preventive capacitor  $C_1$  between the B.S. pin and Vcc pin. Since ceramic capacitor temperature characteristics is not good, confirm that a sufficient amount of allowance for oscillation is provided before starting operation. Oscillation preventive capacitor  $C_2$  may be used between the OUTPUT and GND.

Since the amount of allowance for oscillation varies depending on the print pattern and capacitor position, design the system by referring to our application board patterns.

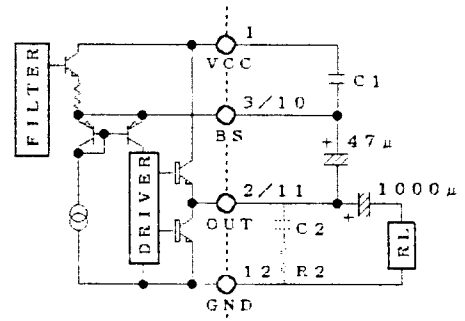


Fig.7

### 4. Vcc line and GND line

Since PIN12 is used for both Pre. GND and Pow. GND, some print patterns may cause worse crosstalk and distortion factor due to the common impedance of these GNDs. The power supply capacitor between Vcc and GND may also deteriorate ripple rejection and distortion factor due to the impedance common to the Vcc and GND of some print patterns. So design the system by referring to our application board patterns ( $1000\mu F$  or higher capacity power supply capacitors are recommendable).

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## 5. ST.BY SW. (Standby switch)

Since as ST.BY SW. is built in PIN6, power can be turned on and off with a small-capacity switch. ON-voltage  $V_1$  is available within the voltage range,  $3V \sim V_{cc}$ . So the ST.BY PIN voltage will deteriorate no characteristics as in the conventional systems, resulting in higher degree of freedom in designing.

Some switches installed outside generate a low popping sound when it is turned off. In such a case, install an approx.  $0.022 \mu F$  capacitor (C3).

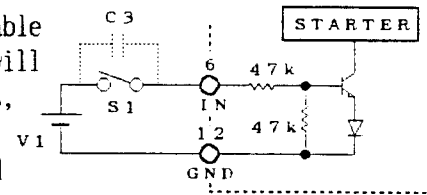


Fig.8

## 6. Filter pin

PIN7 is used for the ripple filter. Rejection becomes easier to some extent as the pin capacity increases. But since it influences the starting time,  $100 \sim 220 \mu F$  is recommended.

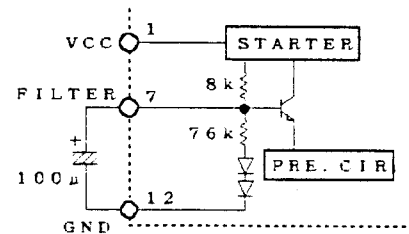


Fig.9

## 7. Supply voltage

When Power transistors are inside of ASO, the IC will not be in trouble up to the maximum absolute rating,  $V_{cc}=24.0V$ . When the IC is operating of ordinary,  $V_{cc}$  should be suppressed to inside of recommended operating supply voltage range.

After all, When ST.BY SW is turned off, The IC is compensated till Absolute Maximum Supply Voltage ( $V_{ccMax}=24.0V$ ). When ST.BY SW. is turned on, set the regulation characteristic of power supply such as  $V_{cc}$  should be suppressed to  $18.0V$  or lower, capacity of power supply capacitor considered. If this level is exceeded, the IC is damaged.

Installation of the IC in the reverse direction may instataneously damage the IC since PIN1 connects the  $V_{cc}$  and PIN12, the GND. So take sufficient care.

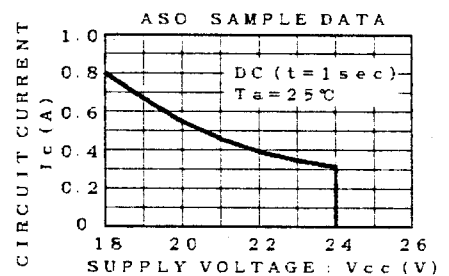


Fig.10

## 8. T.S.D. (Thermal shutdown)

When the IC temperature has extraordinarily increased due to the shortcircuit of loading or insufficient heat release, the heat cutting circuit operates to restrict the output voltage. The circuit is set to operate when the heat releasing plate is at approx.  $175^\circ C$ .

## 9. Others

Our application board patterns are recommendable but sufficiently check the required characteristics before operation to prevent careless mistakes. Before modifying the fixed number of outside installation, study not only the static characteristics but also the transient ones including the dispersion of the IC and other parts installed outside.

## 10. Standard DC electric potential of each pin ( $V_{cc}=12V$ , $T_a=25^\circ C$ , Circuit measured: Fig.2)

PIN No	1	2	3	4	5	6	7	8	9	10	11	12
DC (V)	$V_{cc}$	6.0	10.0	0.6	0.004	$V_{ST. BY}$	10.9	0.004	0.6	10.0	6.0	GND

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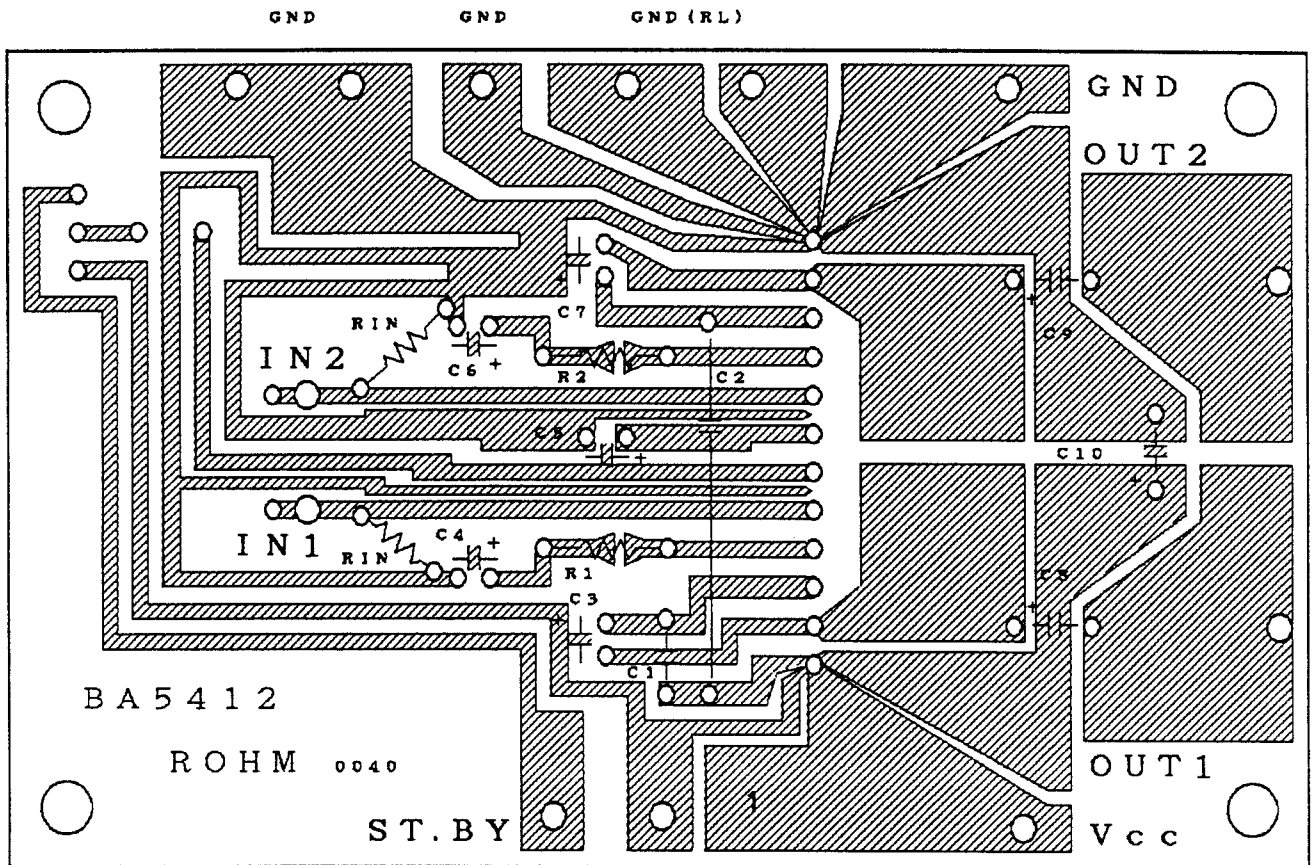
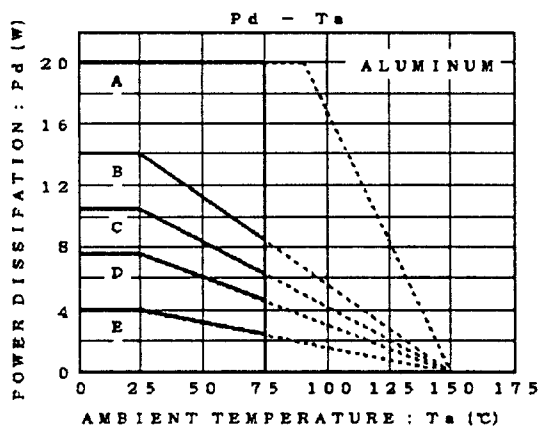


Fig.11



- A: INFINITE HEAT SINK  $\theta_{jc}=3\text{C/W}$   
 B:  $100\text{cm}^2 \times 1.6\text{mm}$   
 C:  $50\text{cm}^2 \times 1.6\text{mm}$   
 D:  $25\text{cm}^2 \times 1.6\text{mm}$   
 E: WITHOUT HEAT SINK  $\theta_{ja}=31\text{C/W}$

Fig.12

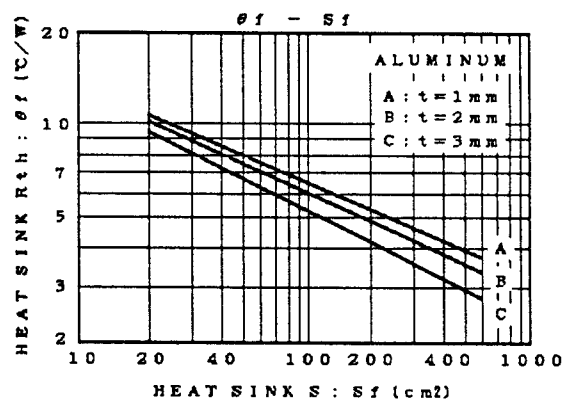
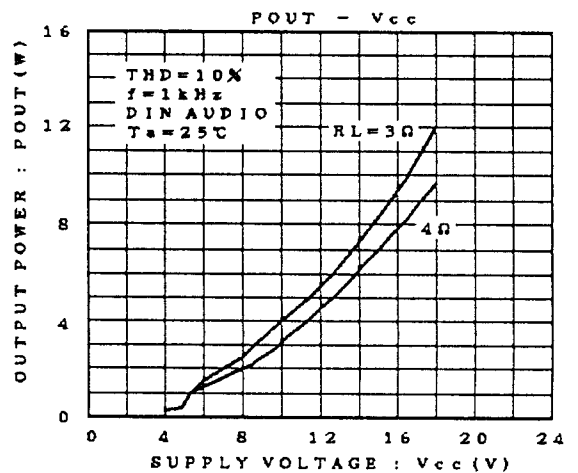
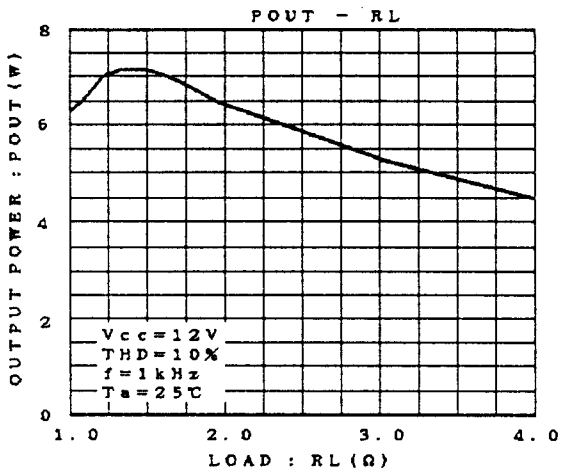
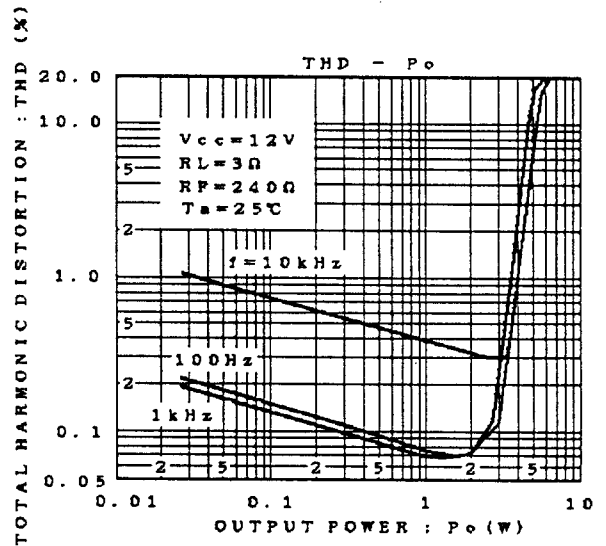
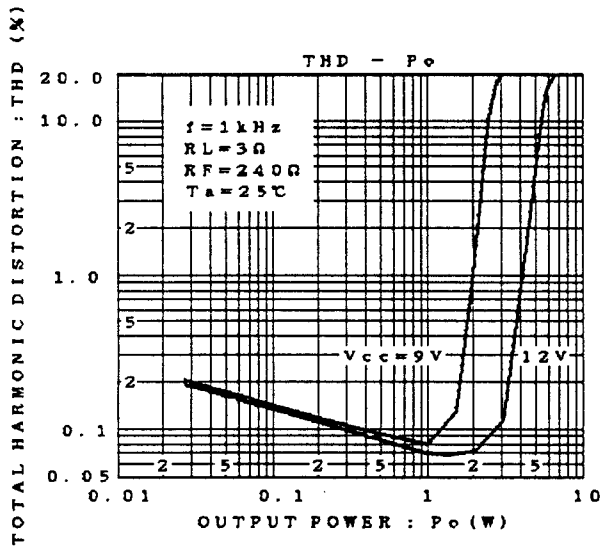
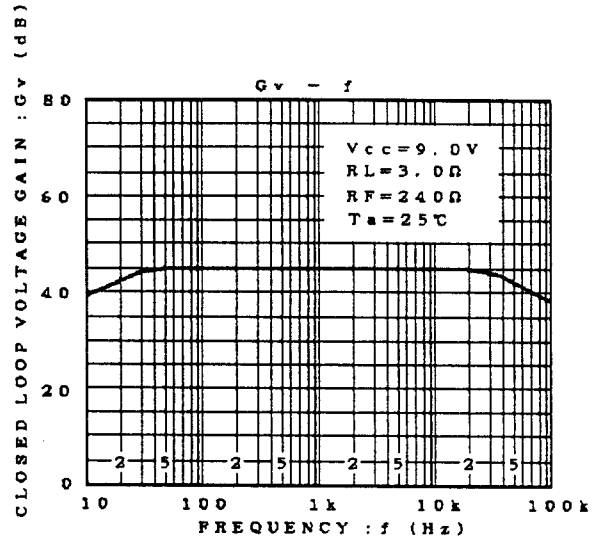
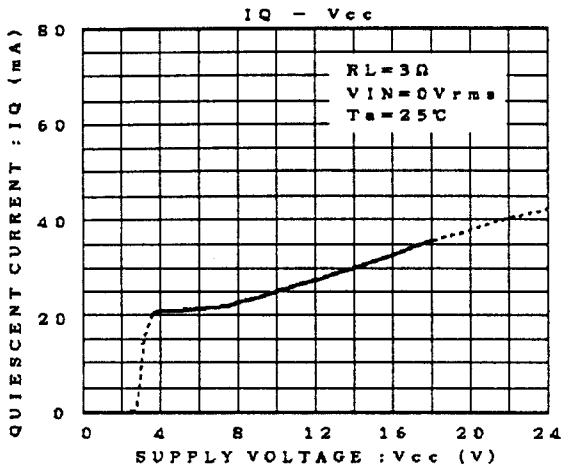


Fig.13

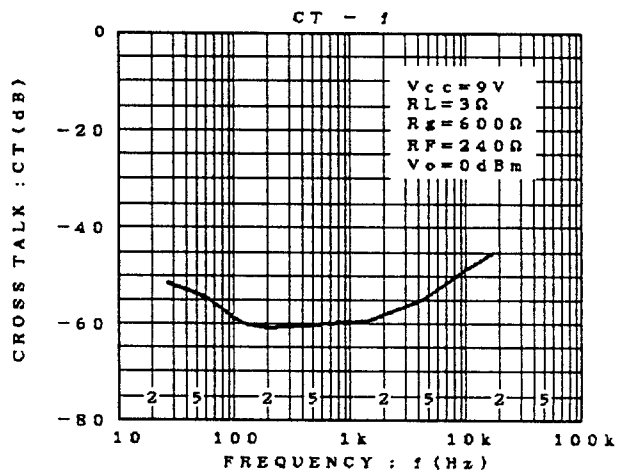
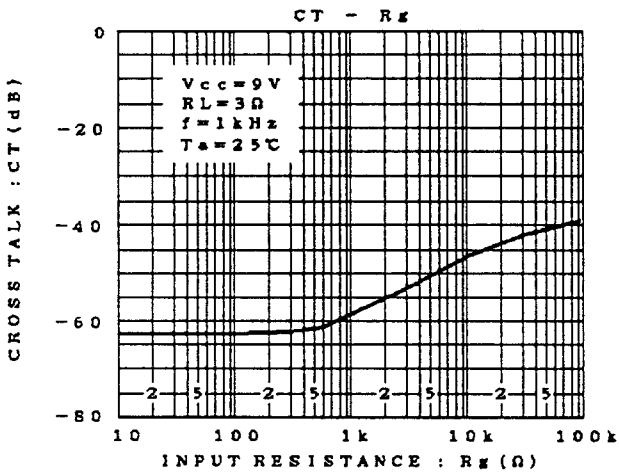
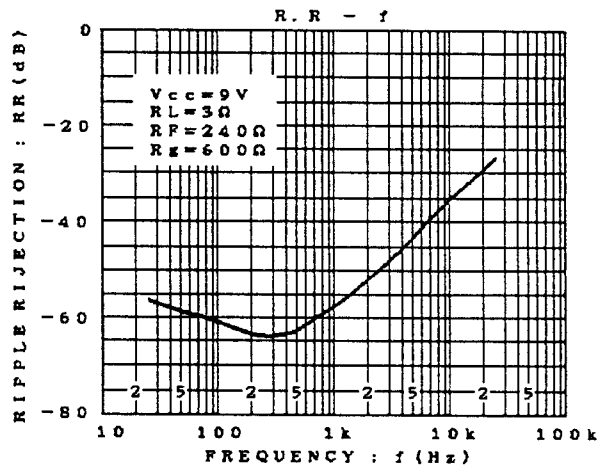
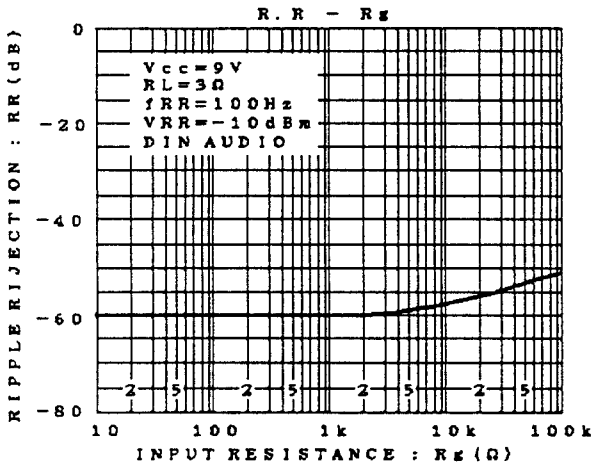
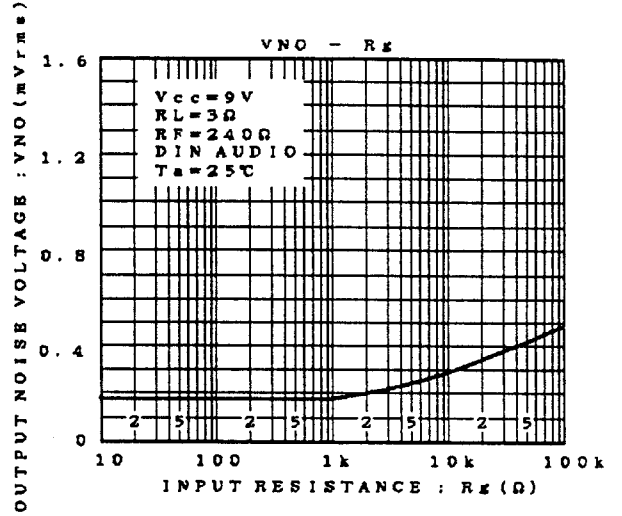
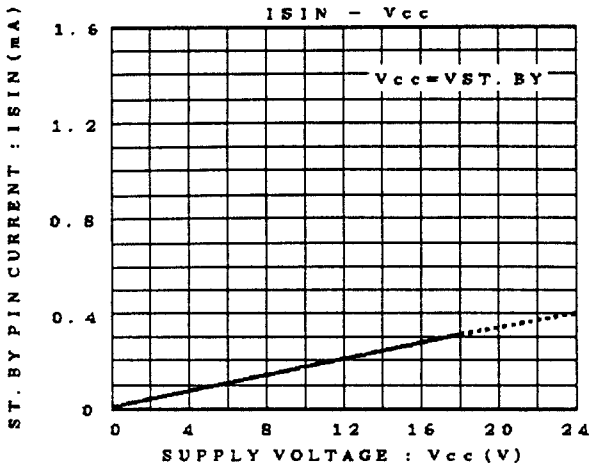
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## Electrical Characteristics Curves



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